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CY7B9973V RoboClock®

High-Speed Multi-Output PLL Clock Buffer

Features

- 10 MHz to 200 MHz output operation
- Output-to-output skews < 350 ps
- 13 LVTTL 50% duty cycle outputs capable of driving 50 Ω terminated lines
- Phase-locked loop (PLL) LOCK indicator
- 3.3V LVTTL/LV differential (LVPECL) hot insertable reference inputs
- Multiply/divide ratios of (4, 6, 8, 10, 12, 16, 20):(2, 4, 6, 8, 10, 12, 16, 20)
- Operation with outputs operating at up to 10x input frequency
- Low cycle-to-cycle jitter (< ±75 ps peak-peak)
- Single 3.3V ± 10% supply
- 52-pin TQFP package

Functional Description

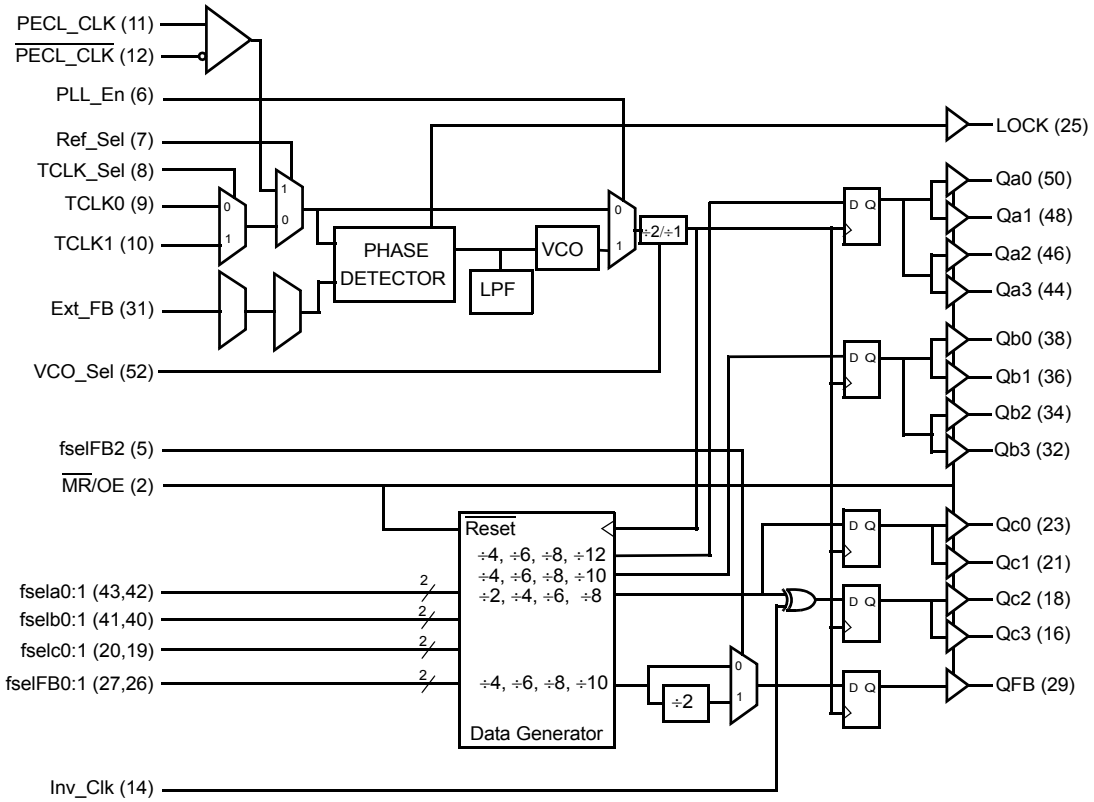
The CY7B9973V Low Voltage PLL Clock Buffer offers user-selectable frequency control over system clock functions. This twelve output clock driver provides the system integrator with selectable frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:3, 5:1, 5:2, 5:3, 6:1 and 6:5 between outputs. An additional output is dedicated to providing feedback information to allow the internal PLL to multiply an external reference frequency by 4, 6, 8, 10, 12, 16 or 20. The completely integrated PLL reduces jitter and simplifies board layout.

The thirteen configurable outputs can each drive terminated transmission lines with impedances as low as 50 Ω while delivering minimal and specified output skews at LVTTL levels.

The CY7B9973V has a flexible reference input scheme with three different hot-insertion capable inputs. These inputs allow the use of either differential LVPECL or single-ended LVTTL inputs, which can be dynamically selected to provide the reference frequency.

For a complete list of related documentation, click here.

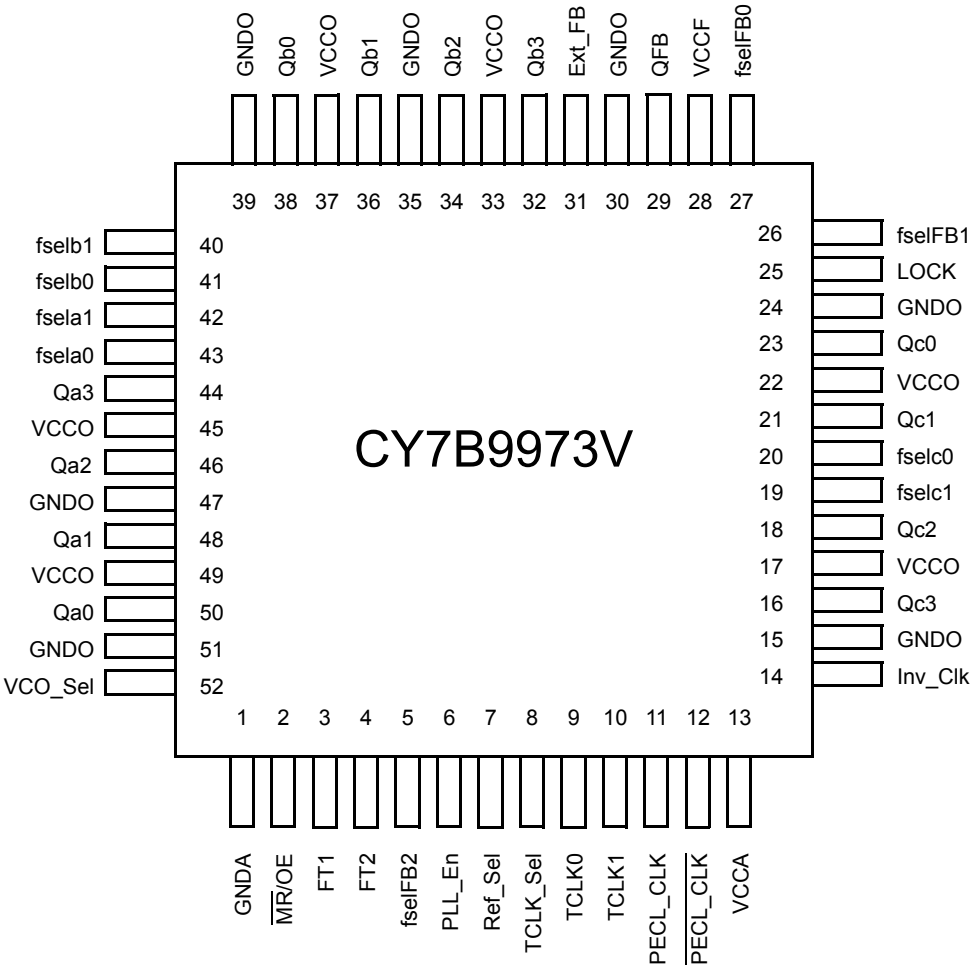
Logic Block Diagram



Contents

Pin Configurations

Figure 1. 52-pin TQFP pinout (Top View)



Selection Options

Table 1. Divider Function Selects for Qa, Qb, Qc

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

Table 2. Divider Function Select for QFB

fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

Table 3. Control Pin Function Selects

Control Pin	Logic ‘0’	Logic ‘1’
VCO_Sel	VCO/2	VCO
Ref_Sel	Controlled by TCLK_Sel	PECL
TCLK_Sel	TCLK0	TCLK1
PLL_En	Bypass PLL	Enable PLL
$\overline{\text{MR}}$/OE	Master Reset/Output Hi-Z	Enable Outputs
Inv_Clk	Noninverted Qc2, Qc3	Inverted Qc2, Qc3

Pin Definitions

Name	Pin No.	Type	Description
Q[a:c][0:3] QFB	50, 48, 46, 44, 38, 36, 34, 32, 23, 21, 18, 16, 29	LVTTL Output	**Clock Output**. These outputs provide numerous divide functions determined by the fsel[a:c][0:1] and the fselFB[0:2] inputs. See Table 1 and Table 2.
Ext_FB	31	LVTTL Input [1]	**PLL Feedback Input**. This input is used to connect one of the clock outputs (usually QFB) to the feedback input of the PLL.
Ref_Sel	7	LVTTL Input [1]	**Reference Select Input**. The Ref_Sel input controls the reference input to the PLL. When LOW, the input is selected by the TCLK_Sel input. When HIGH, the PECL_CLK is selected. This input has an internal pull up.
TCLK_Sel	8	LVTTL Input [1]	**TTL Clock Select Input**. The TCLK_Sel input controls which TCLK[0,1] input is used as the reference input if Ref_Sel is LOW. When TCLK_Sel is LOW TCLK0 is selected. When TCLK_Sel is HIGH TCLK1 is selected. This input has an internal pull up.
TCLK0, TCLK1	9, 10	LVTTL Input [1]	**LVTTL Reference Inputs**. These inputs provide the reference frequency for the internal PLL when selected by Ref_Sel and TCLK_Sel.
PECL_CLK, PECL_CLK	12,11	LV-Diff. PECL Input	**Differential Reference Inputs**. This LV-Differential PECL input provides the reference frequency for the internal PLL when selected by Ref_Sel.
fsel[a:c][0:1]	43, 42, 41, 40, 20,19	LVTTL Input [1]	**Output Divider Function Select**. Each pair controls the divider function of the respective bank of outputs. See Table 1.
fselFB[0:1] fselFB2	27,26, 5	LVTTL Input [1]	**Feedback Output Divider Function Select**. These inputs control the divider function of the feedback output QFB. See Table 2.
VCO_Sel	52	LVTTL Input [1]	**VCO Frequency Select Input**. This input selects the nominal operating range of the VCO used in the PLL. When VCO_Sel is HIGH, the VCO range is 200 to 480 MHz. When VCO_Sel is LOW, the VCO range is 100 to 240 MHz.
PLL_En	6	LVTTL Input [1]	**PLL Bypass Select**. When this input is HIGH, the internal Phase Locked Loop (PLL) provides the internal clocks to operate the part. When this input is LOW, the internal PLL is bypassed and the selected reference input provides the clocks to operate the part.
FT1, FT2	3, 4	LVTTL Input [1]	**PLL Bypass Mode Control Inputs**. When PLL_En is HIGH, these inputs are ignored and may be set to any logic level or left open. These inputs have an internal pull up.
Inv_Clk	14	LVTTL Input [1]	**Invert Mode**. This input only affects the Qc bank. When this input is HIGH, Qc2 and Qc3 are inverted from the “normal” phase of Qc0 and Qc1. When this input is LOW all outputs of the Qc bank are in the “normal” phase alignment.
$\overline{\text{MR}}$/OE	2	LVTTL Input [1]	**Master Reset (Active LOW) and Output Enable (Active HIGH) Input**. When $\overline{\text{MR}}$/OE is deasserted (set to HIGH), the PLL is disturbed and the outputs will be at an indeterminate frequency until it is relocked.
VCCA	13	Power	**PLL Power**.
VCCF	28	Power	**Feedback Buffer Power**.
VCCO	17, 22, 33, 37, 45, 49	Power	**Output Buffer Power**.
GNDA	1	Ground	**PLL Ground**.
GNDO	15, 24, 30, 35, 39, 47, 51	Ground	**Output Buffer Ground**.

Note
1. Includes internal pull up. If this pin is left unconnected, it assumes a HIGH level.

Pin Definitions (continued)

Name	Pin No.	Type	Description
LOCK	25	LVTTL Output	**PLL Lock Indicator**. When HIGH, this output indicates that the internal PLL is locked to the reference signal. When LOW, the PLL attempts to acquire lock. **Note** If there is no activity on the selected reference input, LOCK may not accurately reflect the state of the internal PLL. This pin drives logic, but not Thevenin terminated transmission lines. It is always active and does not go to a high impedance state. This output provides TEST MODE information when PLL_En is LOW.

Functional Overview

Phase Frequency Detector and Filter

These two blocks accept signals from the reference inputs (TCLK0, TCLK1, or PECL_CLK) and the FB input (Ext_FB). Correction information is then generated to control the frequency of the Voltage Controlled Oscillator (VCO). These two blocks, along with the VCO, form a (PLL) that tracks the incoming reference signal.

The CY789973V has a flexible reference input scheme. These inputs allow the use of either differential LVPECL or one of two single-ended LVTTL inputs. The reference inputs are tolerant to hot insertion and can be changed dynamically.

VCO, Control Logic, and Divider

The VCO accepts analog control inputs from the PLL filter block. The VCO_Sel control pin setting determines the nominal operational frequency range of the VCO (f_{NOM}). When VCO_Sel is HIGH, the VCO operating range is 200 to 480 MHz. For systems that need lower frequencies, VCO_Sel can be set LOW, which changes the VCO operating range to 100 to 240 MHz.

Data Generator

The Data Generator has four independent banks: three banks for clock outputs and one bank for feedback. Each clock output bank has four low-skew, high-fanout output buffers (Q[a:c][0:3]), controlled by two divide function select inputs (fsel[a:c][0:1]).

The feedback bank has one high fanout output buffer (QFB). This output is usually connected to the selected feedback input (Ext_FB). This feedback output has three divider function selects fselFB[0:2].

Inv_Clk Pin Function

The Qc bank has signal invert capability. The four outputs of the Qc bank acts as two pairs of complementary outputs when the Inv_Clk pin is driven HIGH. In complementary output mode, Qc0 and Qc1 are noninverting (in phase with the other banks), Qc2 and Qc3 are inverting outputs (inverted from the other banks). When the Inv_Clk pin is driven LOW, the outputs do not invert. Inversion of the outputs are independent of the divide functions. Therefore, clock outputs of Qc bank can be inverted and divided at the same time.

Lock Detect Output Description

The LOCK detect output indicates the lock condition of the integrated PLL. Lock detection is accomplished by comparing the phase difference between the reference and feedback inputs. An unacceptable phase error is declared when the phase difference between the two inputs is greater than about 700 ps.

When in the locked state, after four or more consecutive feedback clock cycles with phase-errors, the LOCK output is forced LOW to indicate out-of-lock state.

When in the out-of-lock state, 32 consecutive phase-errorless feedback clock cycles are required to allow the LOCK output to indicate lock condition (LOCK = HIGH).

If the feedback clock is removed after LOCK has gone HIGH, a Watchdog circuit is implemented to indicate the out-of-lock condition after a time-out period by deasserting LOCK LOW. This time-out period is based upon a divided down reference clock.

This assumes that there is activity on the selected reference input. If there is no activity on the selected reference input, then the LOCK detect pin may not accurately reflect the state of the internal PLL.

The LOCK pin is designed with an intentionally reduced output drive capability to minimize noise and power dissipation. This pin drives logic, but not Thevenin-terminated transmission lines. It is also unaffected by the MR/OE input and is always active.

PLL Bypass Mode Description

The device enters PLL bypass mode when the PLL_En is driven LOW. In factory PLL bypass mode, the device operates with its internal PLL disconnected; input signals supplied to the reference input are used in place of the PLL output. In PLL bypass mode the Ext_FB input is ignored. All functions of the device are still operational in PLL bypass mode.

Factory Test Reset

When in PLL bypass mode (PLL_En = LOW), the device can be reset to a deterministic state by driving the MR/OE input LOW. When the MR/OE input is driven LOW in PLL bypass mode, all clock outputs go to HI-Z; after the selected reference clock pin has five positive transitions, all the internal finite state machines (FSM) are set to a deterministic state. The deterministic state of the state machines depends on the configurations of the divide selects and frequency select input. All clock outputs stay in high impedance mode and all FSMs stay in the deterministic state until MR/OE is deasserted. When MR/OE is deasserted (with PLL_En still at LOW), the device reenters PLL bypass mode.

Safe Operating Zone

The device operates below its maximum allowable junction temperature (t_J < 150°C) in any configuration of multiply or divide with all outputs loaded to the data sheet maximum (with 25 pF load and 0-m/s air flow).

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –40 °C to +150 °C

Ambient Temperature with Power Applied ..... –40 °C to +125 °C

Supply Voltage to Ground Potential .....–0.5 V to +4.6 V

DC Input Voltage ..... –0.3 V to V_{CC} + 0.5 V

Output Current into Outputs (LOW) ..... 40 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2000V

Latch-up Current ..... ±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 10%

DC Characteristics

Over the Operating Range

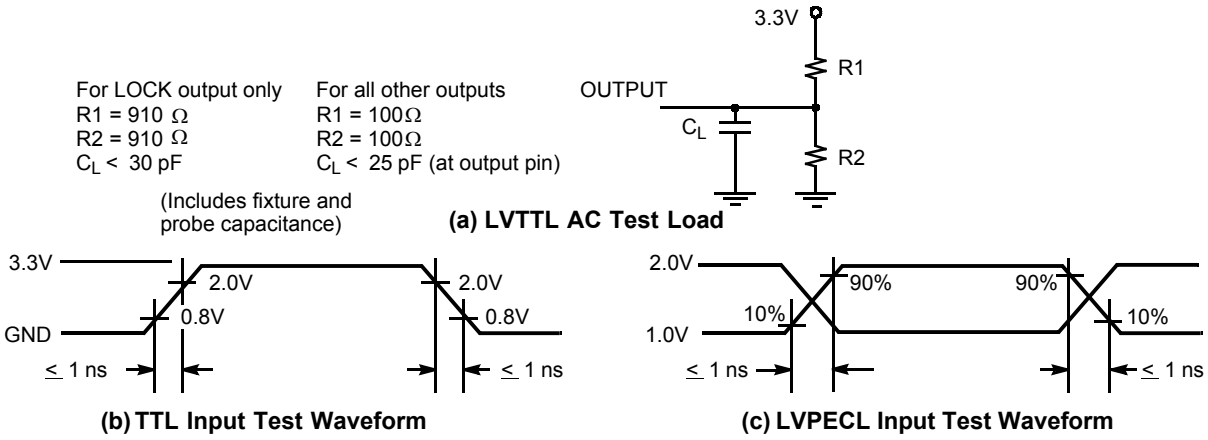
Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage		2.0	–	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–	–	0.8	V
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		400	–	V_{cc}	mV
V_{CMR}	Common Mode Range (Crossing) PECL_CLK	Note 2	0.8	–	V_{cc}	V
V_{OH}	Output HIGH Voltage All “Q” Outputs	I_{OH} = –20 mA[3]	2.4	–	–	V
	Output HIGH Voltage LOCK Output	I_{OH} = –2 mA[3]	2.4	–	–	V
V_{OL}	Output LOW Voltage “Q” Output	I_{OL} = +20 mA	–	–	0.5	V
	Output LOW Voltage LOCK Output	I_{OL} = +2 mA	–	–	0.5	V
I_{IN}	Input Current [4]	All control inputs GND < V_{IN} < V_{CC}	–	–	±150	µA
		PECL_CLK and TCLK[0:1] GND < V_{IN} < V_{CC}	–	–	±500	µA
I_I	Hot Insertion Input Current	PECL_CLK and TCLK[0:1] V_{IN} ≤ 3.63 V V_{CC} = GND	–	–	100	µA
I_{CCQ}	Maximum Quiescent Supply Current	Sum all V_{CC} pins PLL_En = LOW reference off	–	50	150	mA
I_{CCD}	Maximum Dynamic Supply Current (Neglecting Output Load Current)	Outputs unloaded fselFB = 010 (÷8) ref = 50 MHz	–	320	400	mA
C_{IN}	Input Capacitance	Note 5	–	–	4	pF

Notes

2. V_{CMR} is the measured at the point that both inputs achieve the same voltage.
3. The CY7B9973V clock outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge.
4. Inputs have pull up resistors which affect input current.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [6]



(a) LVTTL AC Test Load

(b) TTL Input Test Waveform

(c) LVPECL Input Test Waveform

Note
6. These figures are for illustrations only. The actual ATE loads may vary.

PLL Input Reference Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Max	Unit
t_r, t_f	TCLK Input Rise/Fall Time	Note 7	–	3.0	ns
f_{ref}	Reference Input Frequency		14	120	MHz
t_{refDC}	Reference Input Duty Cycle		25	75	%

AC Characteristics

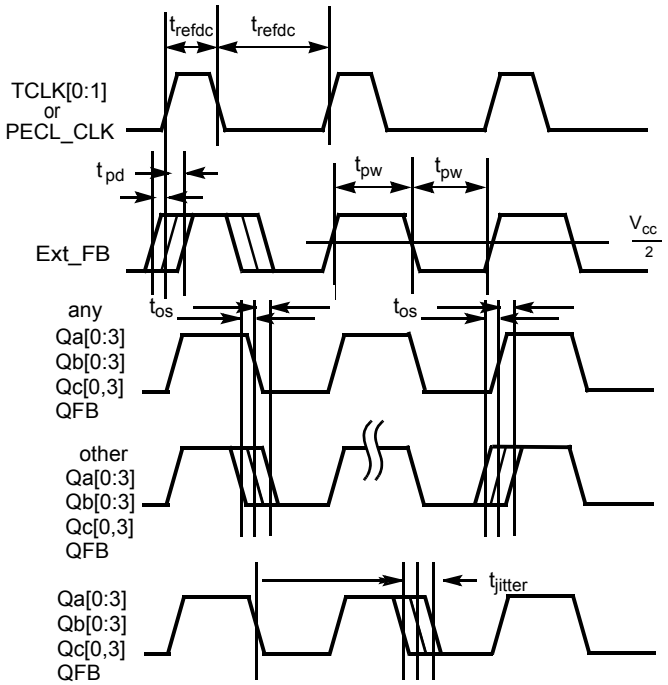
Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_r	Output Rise Time	0.8 to 2.0 V[8]	0.15	–	1.2	ns
t_f	Output Fall Time	2.0 to 0.8 V[8]	0.15	–	1.2	ns
t_{pw}	Output Duty Cycle	f_{max} < 125 MHz[9, 10]	(t_{CYCLE}/2) – 400	(t_{CYCLE}/2) ± 200	(t_{CYCLE}/2) + 400	ps
		f_{max} > 125 MHz[9, 10]	(t_{CYCLE}/2) – 450	(t_{CYCLE}/2) ± 225	(t_{CYCLE}/2) + 450	ps
t_{pd}	Propagation Delay (Selected Reference Input Rise to Ext_FB Rise) QFB = ÷ 8	Notes 10, 11	–350	–	+350	ps
t_{os}	Output to Output Skew	Notes 10, 12	–	–	±350	ps
f_{VCO}	VCO Lock Range		200	–	480	MHz
f_{max}	Maximum Output Frequency	Note 13	–	–	200	MHz
$t_{jitter\ (CC)}$	Cycle to Cycle Jitter (Peak-Peak), 10,000 clocks	Note 14	–	±50	±75	ps
$t_{jitter\ (PER)}$	Period Jitter (Peak-Peak), 10,000 clocks	Note 14	–	120	168	ps
	Period Jitter (Peak-Peak), RMS		–	12	15.5	ps
$t_{jitter\ (PHASE)}$	I/O Phase Jitter (Peak-Peak), 10,000 clocks, ÷ 4 feedback, VCO = 250 MHz	Note 14	–	175	280	ps
	I/O Phase Jitter (Peak-Peak), RMS		–	24	46	ps
t_{OLZ}, t_{OHZ}	Output Disable Time	Note 15	1	–	10	ns
t_{OZL}, t_{OZH}	Output Enable Time	Notes 16, 17	0.5	–	14	ns
t_{lock}	Maximum PLL Lock Time		–	–	10	ms
t_{TB}	Total Timing Budget Window	Note 18	–	–	775	ps

Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Measured with no load.
9. t_{PW} is measured at Vcc/2.
10. 50Ω transmission line terminated into V_{CC}/2.
11. t_{PD} is specified for a 50 MHz input reference. The t_{PD} does not include jitter.
12. All outputs operating at the same frequency.
13. f_{max} measured with CL = 25 pF.
14. Not a tested parameter. Guaranteed by characterization.
15. Measured at 0.5V deviation from starting voltage.
16. For t_{OZL} and t_{OZH} minimum, C_L = 0 pF, R_L = 1k (to V_{CC} for t_{OZL}, to GND for t_{OZH}). For t_{OZL} and t_{OZH} maximum, CL= 25 pF and RL = 100Ω (to V_{CC} for t_{OZL}, to GND for t_{OZH}).
17. t_{OZL} maximum is measured at 0.5V. t_{OZH} maximum is measured at 2.4V.
18. $t_{TB} = t_{pd} + t_{OS} + t_{jitter}$, this parameter is calculated and is the worst case between devices.

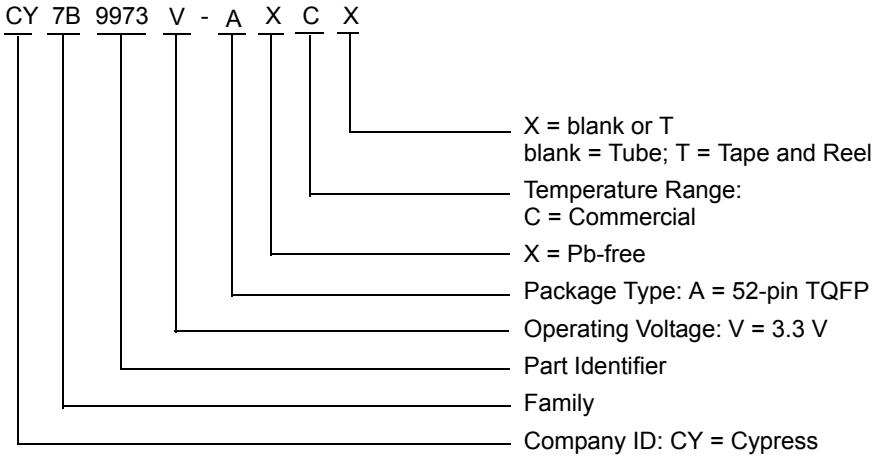
AC Timing Diagrams



Ordering Information

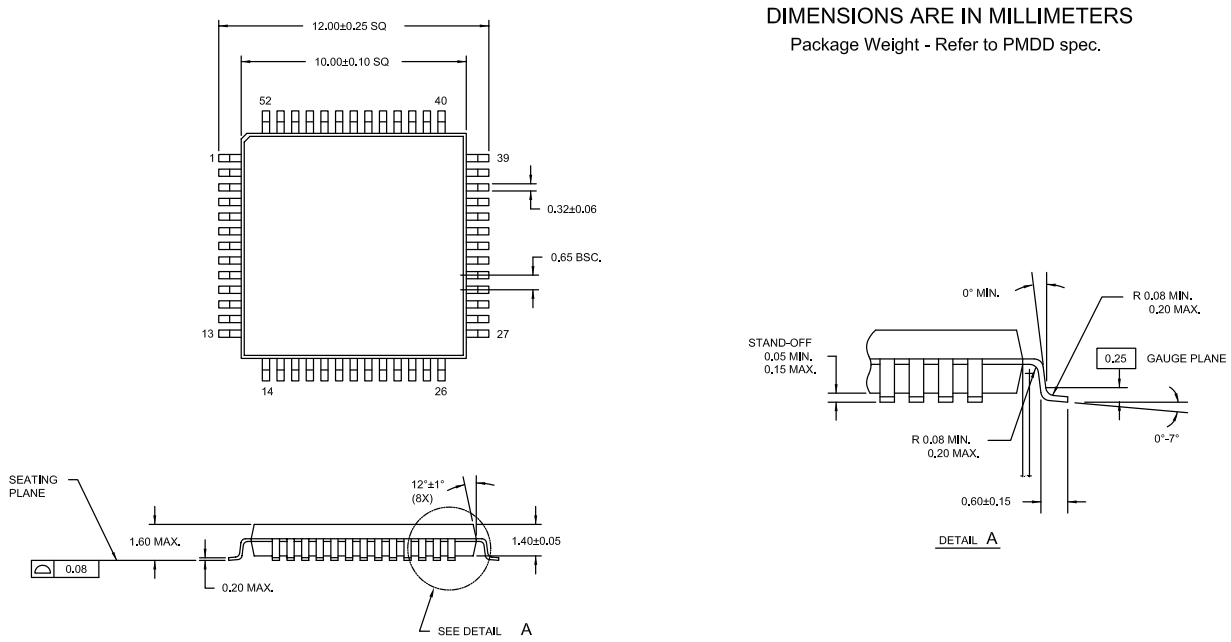
Ordering Code	Package Name	Package Type	Operating Range
Pb-Free			
CY7B9973V-AXC	AZ52	52-pin TQFP	Commercial, 0 °C to 70 °C
CY7B9973V-AXCT	AZ52	52-pin TQFP, Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Diagram

Figure 3. 52-pin TQFP (10 × 10 × 1.4 mm) A52SA Package Outline, 51-85131



Acronyms

Table 4. Acronyms Used in this Documnent

Acronym	Description
FSM	Finite State Machine
LVPECL	Low-Voltage Positive Emitter Coupled Logic
LVTTL	Low-Voltage Transistor-Transistor Logic
OE	Output Enable
RMS	Root Mean Square
PLL	Phase Locked Loop
TQFP	Thin Quad Flat Pack
VCO	Voltage Controlled Oscillator

Document Conventions

Units of Measure

Table 5. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	µVrms	microvolts root-mean-square
dB	decibel	µW	microwatt
dBc/Hz	decibels relative to the carrier per Hertz	mA	milliampere
fC	femtoCoulomb	mm	millimeter
fF	femtofarad	ms	millisecond
Hz	hertz	mV	millivolt
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolt	σ	sigma: one standard deviation

Document History Page

Document Title: CY7B9973V RoboClock®, High-Speed Multi-Output PLL Clock Buffer Document Number: 38-07430				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	115842	06/10/02	HWT	New data sheet.
*A	128182	09/15/03	RGL	Updated AC Characteristics: Removed t_{jitter} parameter and its details. Added $t_{jitter\ (CC)}$, $t_{jitter\ (PER)}$, $t_{jitter\ (PHASE)}$ parameters and their details. Updated AC Timing Diagrams: Tightened duty cycle spec and split duty cycle based on output frequency.
*B	506217	See ECN	RGL	Post to external web.
*C	2902940	04/01/10	KVM	Updated Features: Removed “Pin-compatible with Motorola MPC973”. Updated Ordering Information: Updated part numbers. Added operating temperature range in “Operating Range” column. Updated Package Diagram. Updated to new template.
*D	3057972	10/14/2010	BASH	Added Ordering Code Definitions under Ordering Information. Added Acronyms and Units of Measure.
*E	4176955	10/29/2013	CINM	Updated Package Diagram: spec 51-85131 – Changed revision from *A to *C. Updated to new template. Completing Sunset Review.
*F	4563192	11/17/2014	CINM	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Fixed formatting issues.
*G	5493962	10/25/2016	XHT	Updated to new template. Completing Sunset Review.
*H	5979440	11/29/2017	AESATMP9	Updated logo and copyright.

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