AN17006

High Speed Serial Simulation with HOTLink II™

Associated Project: No
Associated Part Family: HOTLink II™
Software Version: H-Spice version 2001.4 or later
Related Application Notes: None

AN17006 discusses the methodology for simulation of high speed links of the HOTLink II™ over the backplanes, using H-Spice.

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HOTLink II™ Background

The HOTLink II™ family of devices are point-to-point or point-to-multipoint communication building blocks, providing encoding, serialization, deserialization, and decoding at high speed and are compatible with many communication standards. A HOTLink II device is a frequency agile transceiver with the ability of the serial links to transport data at a rate between 0.2 and 1.5 Gigabits per second (Gbps) per channel.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting backplanes on switches, routers, servers, and video transmission systems.

The purpose of this document is to discuss the methodology for simulation of the high-speed serial links of the HOTLink II over the backplanes, using H-Spice and to enable the HOTLink II customers to simulate the performance of their designs.

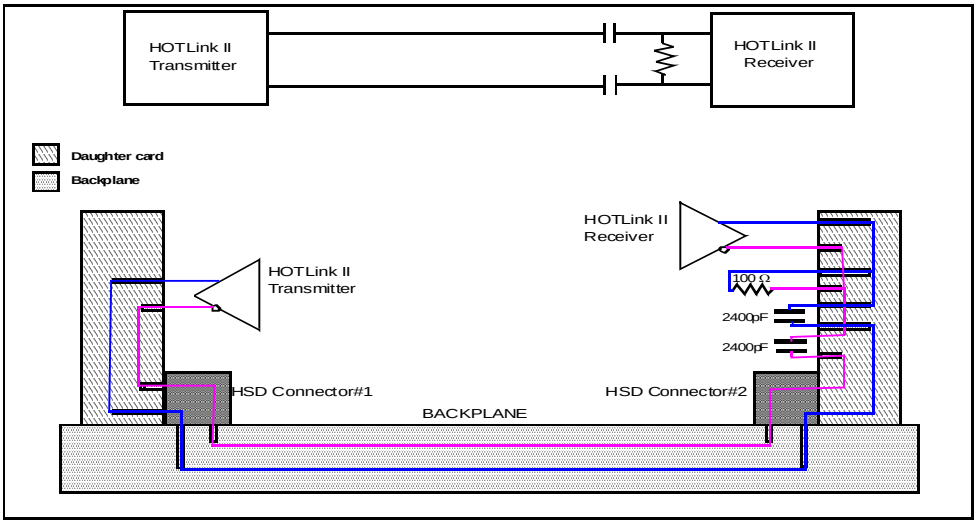
Simulation Methodology

Setup

This document discusses the serial link simulation of the HOTLink II using H-Spice for accurate modeling. A typical backplane implementation of the 1.5-Gbps serial link using two 8-row HSD connectors is simulated and analyzed with H-Spice. Teradyne (http://www.teradyne.com) supplied backplane and HSD connector simulation parameters are used.

The simulation is done for the setup as shown in Figure 1.

Figure 1. Basic Setup and Physical Setup



The HOTLink II Transmitter serial output is transmitted in the following way before it is input to the serial input of the HOTLink II Receiver.

1. The differential serial outputs of the HOTLink II Transmitter are traced into the daughter card through vias.
2. The traces travel in the daughter card for 4 inches before they are routed though the vias to the differential HSD connector#1 (for the transmitter).
3. The traces go to the backplane from the HSD connector#1 through the vias. These traces run 20 or 30 inches on the FR-4/Getek backplane before going into differential HSD connector#2 (for the receiver).
4. From the HSD connector#2, the traces traverse 4 inches through the daughter card before they reach the Receiver of the HOTLink II. The differential serial lines are AC-coupled with 2400 pF and are terminated with a 100 W resistor as shown in the Figure 1.

The simulation is done based on the following assumptions.

1. The traces in both of the daughter cards are 5 mils wide and 4 inches long. The trace width is assumed to be ±0.5 mil to account for etch process variation.
2. The traces in the backplane are 8 mils wide and 20 inches long. The trace width is assumed to be ±0.5 mil to account for etch process variation.
3. All traces are modeled assuming stripline construction.
4. The circuit traces included frequency dependent losses. This was modeled by converting the output from RLGC, a 2D field solver, to an H-Spice compatible ".RLC" file for-mat. The dielectric assumptions (ε_r and loss tangent δ) used, as the input to the RLGC field solver, are shown in Table 1. The dielectric values were obtained from vendor supplied data.

Table 1. Board Material Characteristics Used

Board Material	ε_r at 1.0 GHz	δ at 1.0GHz
FR-4	4.0	0.018
Getek	3.9	0.0093

5. Via and pad capacitances were characterized using a via model based on a 0.250-inch-thick backplane and 0.093-inch-thick daughter cards. Note that worst-case via effect was assumed such that the connections were on one end of the via leaving the rest of the via as an unterminated stub.
6. Rows G and H of the Teradyne HSD 8 row connector model were used to interconnect the daughter cards and the backplane.
7. The AC coupling capacitors are 402 in size and 2400 pF in value. These capacitors are 0.25 inches away from the terminating resistor. The terminating resistor is 0.25 inches away from the Receiver buffer of HOTLink II.
8. The simulation is done for 1.5-Gbps serial speed. The pulse pattern consists of a K28.5 with a single 1 and a single 0 embedded. The pattern used is "0101111100 1010000011 0000000010000000 1111111011111111". The single embedded bits will represent a PRBS 2^7.

9. The following conditions were assumed for weak, typical and strong cases.

Table 2. Parameters for Different Conditions

Silicon Corner	Temperature (°C)	Voltage (V_{CC})	Backplane and Daughter Card Impedance	Trace Widths
Worst	100	–5%	110 Ω	–0.5 mil
Typical	25	Nominal	100 Ω	Nominal
Best	0	+5%	90 Ω	+0.5 mil

H-Spice Simulation Code

The HOTLink II Transmitter serial outputs conform to the CML signaling standard. The HOTLink II Receiver input buffers are LVPECL-compatible CML input buffers. The CML output buffers and the input buffers have been referenced by the main simulation file (henceforth to be called SIM.CKT) as sub-circuits. Other simulation components shown later in the document is for the lossy transmission line (Sample.RLC), for the capacitors (CAP.TXT), and for the waveform (FF.TXT). The specific components that have not been shown in this document are for the vias (11X093VIAS.txt & Hsdvias.txt) and for the HSD connector (hsd1gh.cir) that can be obtained from Teradyne under nondisclosure agreement.

The following files are required in the simulation. Please note that the comments are written in red and will explain the code.

SIM.CKT

```
*** MODEL [sim.ckt]
**- Cypress CMLOUT & CMLIN (CYP15G0401DXB)
**- Bit pattern: PRBS @1.5Gbps
.prot
**- Cypress serial output & input spice
**- models. Must be used with permission
.include 'cmlout.ckt'
.include 'cmlin.ckt'
**- Cypress Corner files
.include 'trtc.cor'
.include 'trtclin.cor'
.include 'ss.cor'
.include 'npnc.cor'
**- Typical via files from Teradyne
**- Must be used with permission
.include '11X093VIAS.txt'
.include 'Hsdvias.txt'
**- Contains the test pattern
.include 'FF.txt'
**- Model for 0402 @6.3V @X7R Capacitor
.include 'Cap.txt'
**- Model for Teradyne 8 row Connector
**- Must be used with permission
.include 'hsd1gh.cir'
.unprot
```

Now the static parameters need to be declared.

```
Vvpwr vpwr 0 dc vccr
Vvgnd vgnd 0 dc vssr
**- This is for the best case situation
**- for worst case vccr='3.3*0.95'
**- for Typical case vccr='3.3'
.param vccr='3.3*1.05'
.param vssr=0v
```

The following code shows how the different elements in the design are modeled. Note that all components in the design as shown in Figure 2 have been simulated.

```
**- Cypress Serial Out Subckt
IBIS_9294_CMLOUT
XBUF a_n a_p vpwr vgnd DOUTP DOUTN
IBIS_9294_CMLOUT
**- OUTP(positive) & OUTN(negative) of
HOTLink II go through the vias to the
daughter card
X1 0000 DOUTP DOUTPI DCVIA1
X2 0000 DOUTN DOUTNI DCVIA1
**- Model for the stripline in the
daughter-card simulated. Length=4 inches,
Material=FR-4
**- Name of the file containing the model
is Sample.RLC
W2 N=1 DOUTPI 0000 DC1IIP 0000
RLGCFILE=Sample.RLC L='4/39.37'
W3 N=1 DOUTNI 0000 DC1IIN 0000
RLGCFILE=Sample.RLC L='4/39.37'
**- Vias again. Going to the G and H rows
of the HSD connector
X3 0000 DC1SIP DC1IIP DCVIA1
X4 0000 DC1SIN DC1IIN DCVIA1
**- Calling HSD8GH from the file hsd1gh.cir
X5 0000 DC1SIP DC1SIN DC1SOP DC1SON HSD8GH
**- Vias going to the Backplane.
X6 0000 DC1SOP DC1IOP HSDVIA1
X7 0000 DC1SON DC1ION HSDVIA1
**- 20 inches Backplane traces. the
parameters of the transmission line are
**- in Sample1.RLC file. The material used
here is FR4.
W7 N=1 DC1IOP 0000 DC2IOP 0000
RLGCFILE=Sample1.RLC L='20/39.37'
W8 N=1 DC1ION 0000 DC2ION 0000
RLGCFILE=Sample1.RLC L='20/39.37'
**- Vias going to the HSD connector
X8 0000 DC2SOP DC2IOP HSDVIA1
X9 0000 DC2SON DC2ION HSDVIA1
**- Calling HSD8GH from the file hsd1gh.cir
X10 0000 DC2SIP DC2SIN DC2SOP DC2SON HSD8GH
```

```
**- Vias going to the daughter card
X11 0000 DC2SIP DC2IIP DCVIA1
X12 0000 DC2SIN DC2IIN DCVIA1
**- transmission lines through the daughter
card. Length=3.5 inches. Material=FR-4
W12 N=1 DC2IIP 0000 CAPPI 0000
RLGCFILE=Sample.RLC L='3.5/39.37'
W13 N=1 DC2IIN 0000 CAPNI 0000
RLGCFILE=Sample.RLC L='3.5/39.37'
**- Vias going to the 2400pF caps.
X13 0000 CAPP CAPPI DCVIA1
X14 0000 CAPN CAPNI DCVIA1
**- Capacitor models. 0402 @ 6.3V @ X7R
Dielectric
X15 CAPP CAPPO CAP
X16 CAPN CAPNO CAP
**- Vias from the capacitors. Going to the
Daughter card
X17 0000 CAPPO CAPPOI DCVIA1
X18 0000 CAPNO CAPNOI DCVIA1
**- Traces for the 100 ohms resistor
termination on the daughter card.
length=0.25 inches
W18 N=1 CAPPOI 0000 RESPI 0000
RLGCFILE=Sample.RLC L='0.25/39.37'
W19 N=1 CAPNOI 0000 RESNI 0000
RLGCFILE=Sample.RLC L='0.25/39.37'
**- Vias to the resistor
X19 0000 RESP RESPI DCVIA1
X20 0000 RESN RESNI DCVIA1
RT RESP RESN 100
**- Traces to the serial differential CML
inputs of the HOTLink II Receiver on
daughter card
**- Length=0.25 inches. Material=FR4. RLGC
file referenced=Sample.RLC
W20 N=1 RESPI 0000 RINPI 0000
RLGCFILE=Sample.RLC L='0.25/39.37'
W21 N=1 RESNI 0000 RINNI 0000
RLGCFILE=Sample.RLC L='0.25/39.37'
**- Vias on the daughter card going to the
LVPECL compatible CML inputs of HOTLink II
RX
X21 0000 RINP RINPI DCVIA1
X22 0000 RINN RINNI DCVIA1
**- calls the subckt IBIS_9294_CMLIN, which
is the high level ckt in the CMLIN h-spice
model.
XRCV RINN RINP vpwr vgnd ROUTP ROUTN
IBIS_9294_CMLIN
```

The following code includes the input output instruction and the transient time.

SIM.CKT (continued)

```
.temp 0
**- Transient time. Simulation done for
170ns with 17ps steps
.tran 17p 170n
.OPTIONS INGOLD=2 METHOD=GEAR PROBE INTERP
.options post=2 tnom=27.0 accurate
.options brief
**- input/output instructions
**- input
.PRINT TRAN DRVROUTP=V(doutp)
DRVROUTN=V(doutn) DRVROUTD= V(doutp,doutn)
**- output
.PRINT TRAN RCVRINP=V(rinp) RCVRINN=V(rinn)
RCVRIND=V(rinp,rinn)
.PRINT TRAN RCVROUTP=V(routp)
RCVROUTN=V(routn) RCVROUTD=V(routp,routn)
```

The final required parameters and commands for plotting the eye are in the following code. Also mentioned in the code is the bit time for operation.

SIM.CKT (continued)

```
**- period of the waveform, no. of octets
and bit time
.param per = '4e-9/3'
.param noct = 2
.param tbit = 'per/2'
.param phase = 'noct*8*per/2'
** needed for eye plotting
.probe c1eye =
par('1*tbit*(((time/(1*tbit)+phase))-
(int(time/(1*tbit)+phase)))')
.probe c2eye =
par('2*tbit*(((time/(2*tbit)+phase))-
(int(time/(2*tbit)+phase)))')
.probe c3eye =
par('3*tbit*(((time/(3*tbit)+phase))-
(int(time/(3*tbit)+phase)))')
****
.END
****
```

This concludes the sim.ckt file.

The following pieces of code are modeled for the lossy transmission line and the capacitors. The sample RLGC file is called Sample.RLC.

Sample.RLC

```
**RLGC parameters for a SE stripline.
**5 mils wide,55 Ohms Worst,FR4 material
**dielectric constant=4.0
**loss tangent of 0.018
**Line is frequency dependent and lossy
****************************************
**- N (number of signal conductors)
1
**- Lo (DC inductance per meter)
3.6689E-07
**- Co (DC capacitance per meter)
1.2130E-10
**- Ro (DC resistance per meter)
1.0480E+01
```

```
**- Go (DC conductance per meter)
0.0000E+00
**- Rs (Skin resistance per meter)
1.5043E-03
**- Gd(Dielectric loss conductance/meter)
1.3720E-11
```

The capacitor model is as shown below. The sample capacitor model is called CAP.TXT.

CAP.TXT

```
.SUBCKT CAP IN OUT
* 0402 @ 6.3V @ X7R Dielectric
RC IN 1 0.642
LC 1 2 0.8NH
CC 2 OUT 2399.004pF IC=0V
.ENDS CAP
```

The input waveform to the HOTLink II Transmitter is defined in FF.txt. The contents of the FF.txt is shown below.

FF.txt

```
$ 0101111100 111111101111111 000000010000000 1010000011 $
** The 1st and 3rd columns indicate the time and the 2nd and 4th indicate voltage
va_p   a_p 0   pwl
+   0.0000E+00       3.10E+00           ,      1.0000E-10          2.90E+00
+   5.6667E-10       2.90E+00           ,      7.6667E-10          3.30E+00
+   1.2333E-09       3.30E+00           ,      1.4333E-09          2.90E+00
+   1.9000E-09       2.90E+00           ,      2.1000E-09          3.30E+00
+   5.2333E-09       3.30E+00           ,      5.4333E-09          2.90E+00
+   6.5667E-09       2.90E+00           ,      6.7667E-09          3.30E+00
+   1.1233E-08       3.30E+00           ,      1.1433E-08          2.90E+00
+   1.1900E-08       2.90E+00           ,      1.2100E-08          3.30E+00
+   1.6567E-08       3.30E+00           ,      1.6767E-08          2.90E+00
+   2.1233E-08       2.90E+00           ,      2.1433E-08          3.30E+00
+   2.1900E-08       3.30E+00           ,      2.2100E-08          2.90E+00
+   2.6567E-08       2.90E+00           ,      2.6767E-08          3.30E+00
+   2.7233E-08       3.30E+00           ,      2.7433E-08          2.90E+00
+   2.7900E-08       2.90E+00           ,      2.8100E-08          3.30E+00
+   2.8567E-08       3.30E+00           ,      2.8767E-08          2.90E+00
+   3.1900E-08       2.90E+00           ,      3.2100E-08          3.30E+00
+   3.3233E-08       3.30E+00           ,      3.3333E-08          3.10E+00
+   R= 0.00E+00
**- The statement with R= is required for generating a repeating pattern.
va_n   a_n 0   pwl
+   0.0000E+00       3.10E+00           ,      1.0000E-10          3.30E+00
+   5.6667E-10       3.30E+00           ,      7.6667E-10          2.90E+00
+   1.2333E-09       2.90E+00           ,      1.4333E-09          3.30E+00
+   1.9000E-09       3.30E+00           ,      2.1000E-09          2.90E+00
+   5.2333E-09       2.90E+00           ,      5.4333E-09          3.30E+00
+   6.5667E-09       3.30E+00           ,      6.7667E-09          2.90E+00
+   1.1233E-08       2.90E+00           ,      1.1433E-08          3.30E+00
+   1.1900E-08       3.30E+00           ,      1.2100E-08          2.90E+00
+   1.6567E-08       2.90E+00           ,      1.6767E-08          3.30E+00
+   2.1233E-08       3.30E+00           ,      2.1433E-08          2.90E+00
+   2.1900E-08       2.90E+00           ,      2.2100E-08          3.30E+00
+   2.6567E-08       3.30E+00           ,      2.6767E-08          2.90E+00
+   2.7233E-08       2.90E+00           ,      2.7433E-08          3.30E+00
+   2.7900E-08       3.30E+00           ,      2.8100E-08          2.90E+00
+   2.8567E-08       2.90E+00           ,      2.8767E-08          3.30E+00
+   3.1900E-08       3.30E+00           ,      3.2100E-08          2.90E+00
+   3.3233E-08       2.90E+00                  3.3333E-08          3.10E+00
+   R= 0.000E+00
```

Simulation Result

The simulation requires H-Spice version 2001.4 or later. The simulation will produce a SIM.tr0 file, which can be plotted on AVANWAVES plotter.

Shown below are the simulated eye diagrams for the following settings.

Table 3. Settings for Simulated Eye Diagrams

Figure No.	Material	Backplane Trace Length	Simulation Condition
Figure 3	FR-4	20 inches	Weak
Figure 4, Figure 5	FR-4	20 inches	Typical
Figure 6, Figure 7	FR-4	20 inches	Strong
Figure 8, Figure 9	FR-4	30 inches	Typical

Figure 2. Simulated Eye for TX Output (20” FR-4 Weak Condition)

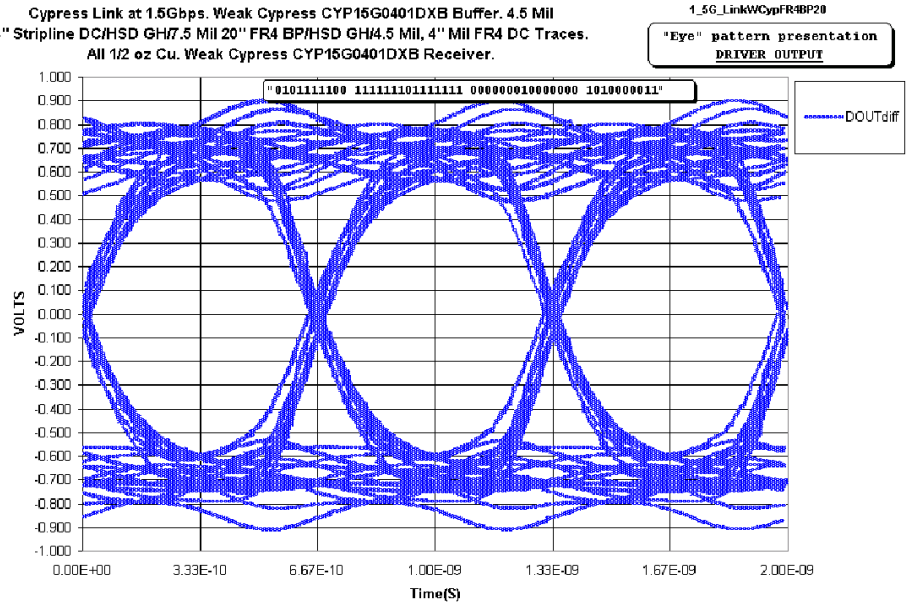


Figure 3. Simulated Eye for RX Input (20” FR-4 Weak Condition)

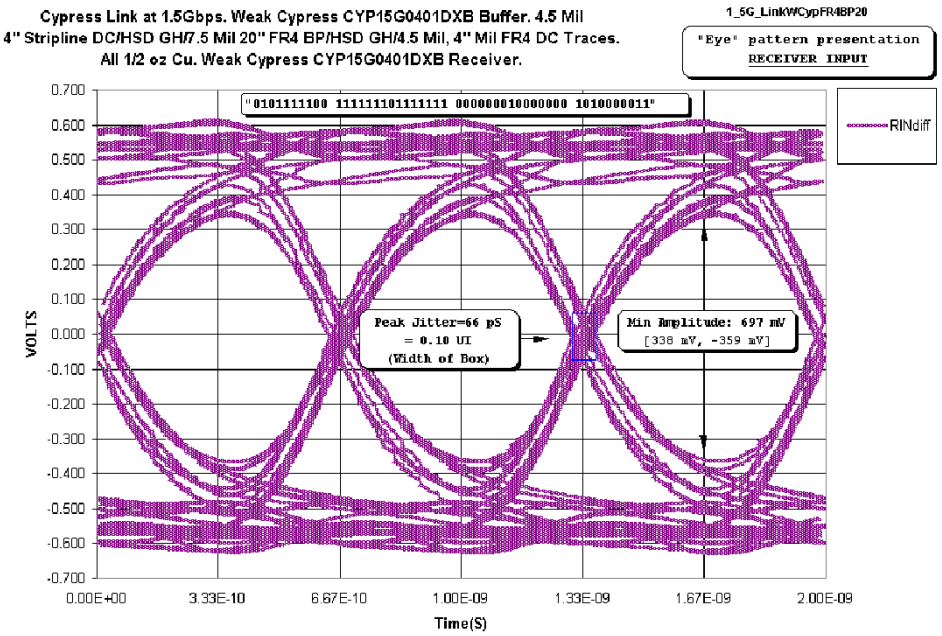


Figure 4. Simulated Eye for TX Output (20” FR-4 Typical Condition)

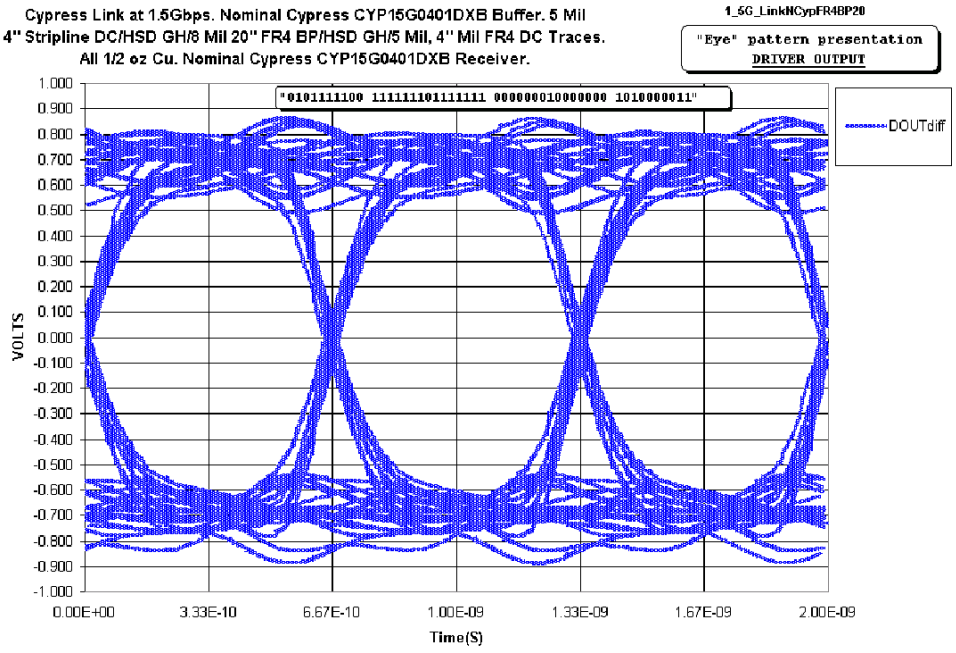


Figure 5. Simulated Eye for RX Input (20” FR-4 Typical Condition)

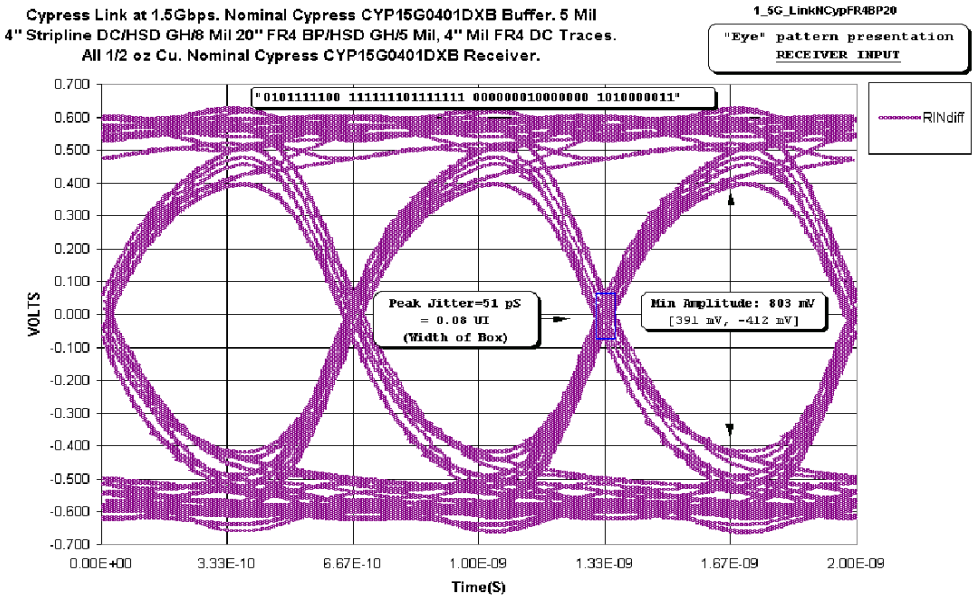


Figure 6. Simulated Eye for TX Output (20” FR-4 Strong Condition)

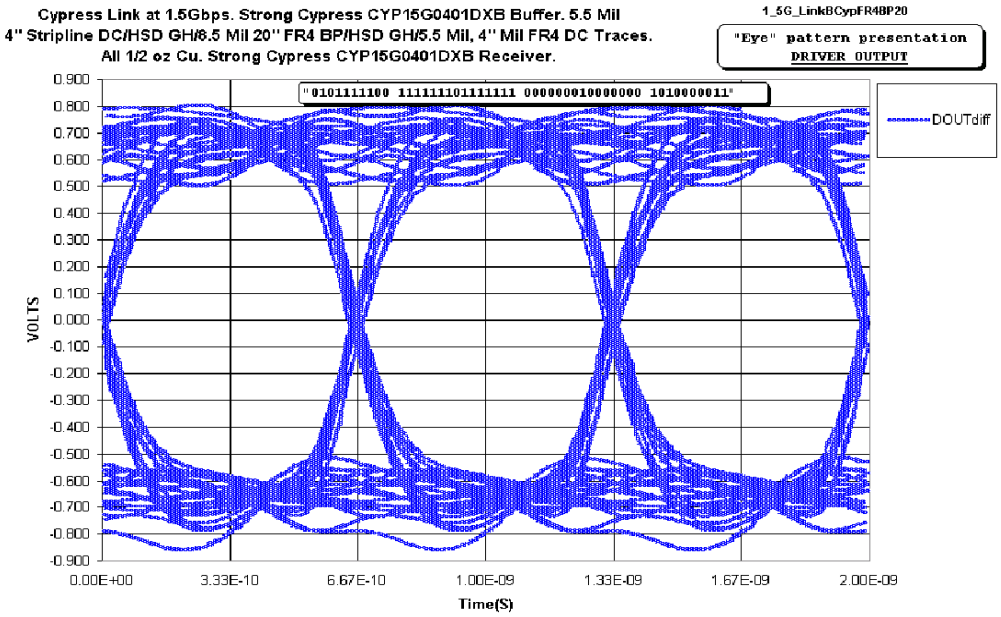


Figure 7. Simulated Eye for RX Input (20” FR-4 Strong Condition

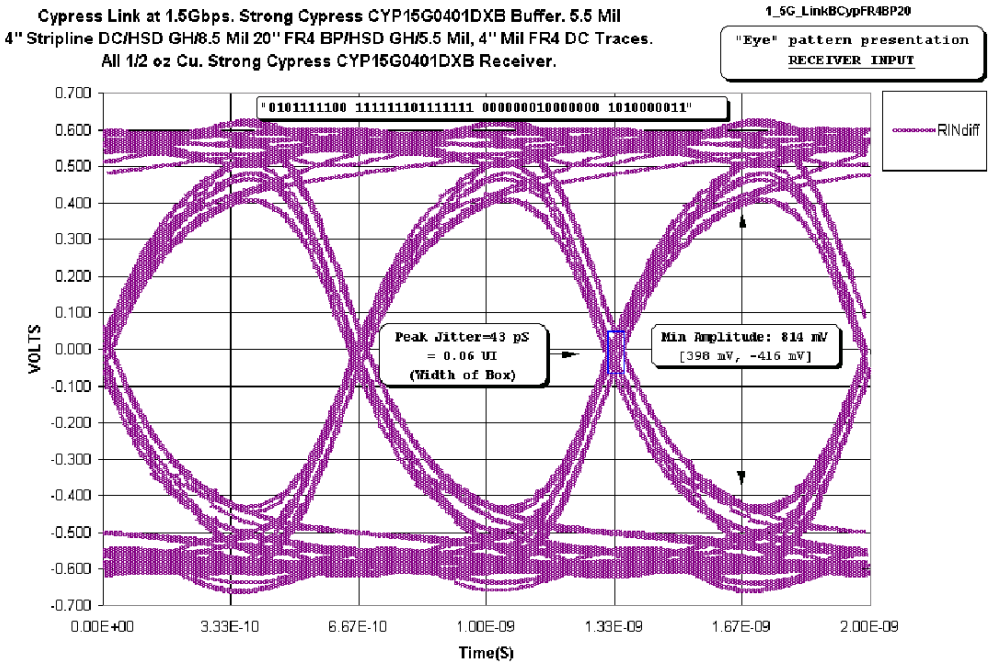


Figure 8. Simulated Eye for TX Output (30” FR-4 Typical Condition)

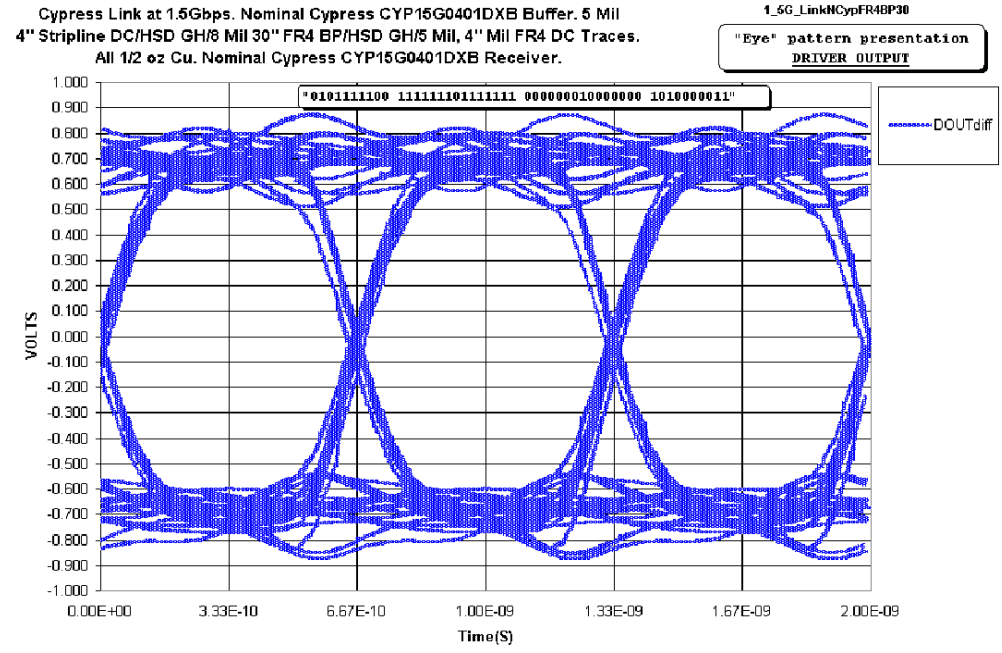
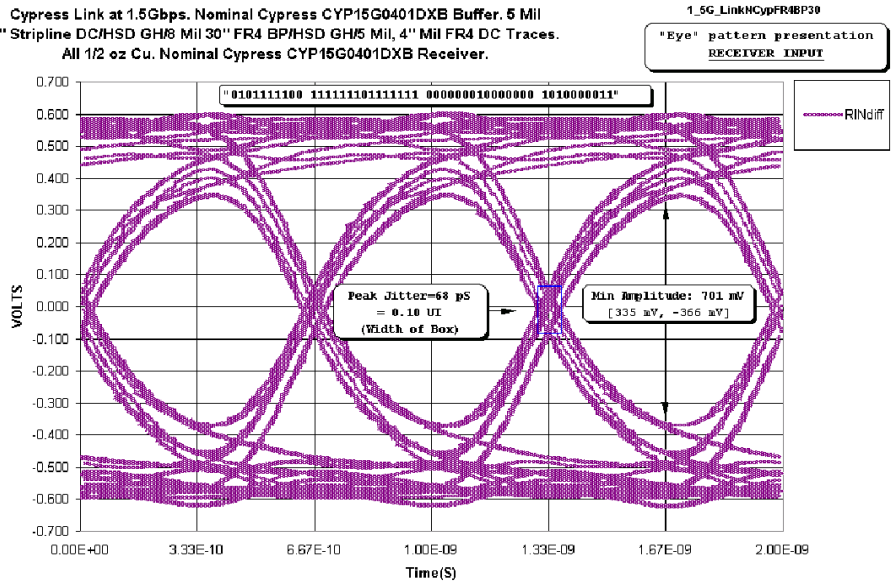


Figure 9. Simulated Eye for RX Input (30” FR-4 Typical Condition)



Summary

The simulations under different conditions demonstrate the performance of the HOTLink II serial output and input drivers. From the simulation results, it can be verified that the peak deterministic jitter is low enough and the minimum eye width is high enough for the HOTLink II to drive 30 inches or more of the serial traces on the backplane with ease. Remember that the simulations show only the deterministic jitter and do not include effects of power supply noise, connector cross talk, reference clock jitter, and so on. However, there is plenty of margin even in the worst-case, to accommodate these effects.

The simulations also demonstrate that the backplane made of Getek material improves the performance, which is specifically useful for the longer backplanes. The improvements include larger eye amplitude, less peak deterministic jitter, and wider eye width. However, with differential signaling, inexpensive FR4 backplanes over 30-inch lengths can easily be used with careful design.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1345503	SAAC	08/07/2007	New spec
*A	3380182	SAAC	09/22/2011	Updated to new template.
*B	4574278	YLIU	11/19/2014	Updated to new template. Completing Sunset Review.
*C	5823094	AESATMP9	07/18/2017	Updated logo and copyright.

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