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AN60305

Using PSoC® 3 and PSoC 5LP IDACs to Build a Better VDAC

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This application note describes how to configure the PSoC® 3 and PSoC 5LP IDACs as a flexible analog source. It presents different approaches for using the IDACs in applications, and discusses the advantages and disadvantages of the topologies presented. This application note will: help you to understand compliance voltage and why it is important; explain how to generate an “any range” or “any ground” VDAC; describe an implementation for a multiplying VDAC; give details on how to build a rail-to-rail low-output impedance 9-bit VDAC from a single IDAC, an opamp, and a resistor; and provide information on how to build a current scaling circuit with an opamp and two resistors.

Voltage DACs Are Great, Current DACs Are Great; PSoC 3 and PSoC 5LP Have Both

Generating an analog signal from digital systems is often a vital part of system design. The generated analog signal can be used to control any number of aspects in a system. Digital-to-analog converter (DAC) requirements are as varied as the applications of which they are a part. Voltage DACs (VDACs) can be used to bias field effect transistors, provide sensor excitation signals, apply a known calibration voltage, generate waveforms, and control voltage operated circuits. Current DACs (IDACs) can be used to bias transistors, perform open circuit detection on long sensor loops, level shift signals, provide precise continuous LED brightness control, and charge or discharge capacitors in a controlled manner (super capacitors), to name a few applications.

Having an IDAC or VDAC provides great flexibility in your designs, but having both makes it possible to address specific design requirements with minimum extra hardware.

1 Know the Limitations of your IDAC

Let us say for your specific design you need a voltage output range of 0 to 200 mV. PSoC 3 and PSoC 5LP VDACs have two built-in ranges of 0 to 1.020 V and 0 to 4.080 V. Neither range is ideal because you want to have the full resolution over your 200 mV range. What do you do? Use an IDAC.

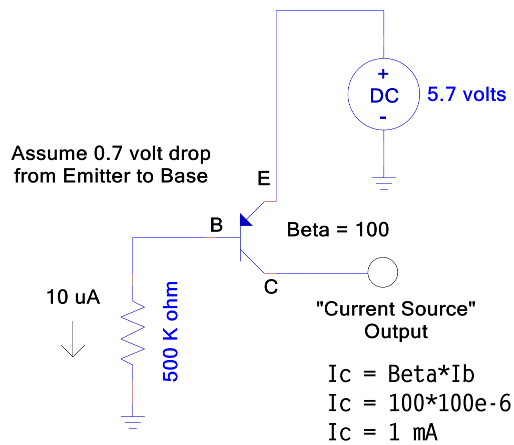
An IDAC and a resistor can generate any desired voltage range as long as you do not violate the compliance voltage of the IDAC. The compliance voltage describes the maximum/minimum voltage a practical current source can reach when attempting to source current and the minimum voltage it can reach when attempting to sink current.

In an ideal current source, the voltage at the output can vary from negative infinity to positive infinity ensuring the specified current flows through the load. This is difficult to achieve in reality, so there are limits on what can be accomplished. Figure 1 shows a simple current source. The voltage at the transistor’s base is kept one diode drop below the voltage at the emitter. The current flowing out of the base is kept at a fixed 10 µA because the base voltage is fixed. The transistors beta (current gain) amplifies the base current by a factor of 100, producing 1 mA at the collector, ignoring the negligible base current contribution.

The circuit shown in Figure 1 tries to source 1 mA from the collector into a load connected to the output, but there are limitations. Let us say that the voltage from the emitter to the collector must be greater than or equal to 0.7 V to maintain the current through the transistor. All other non-idealities of real transistors are ignored. As long as the load does not require more than 5 volts on the collector to consume 1 mA, this circuit will act as a current source. The collector voltage can move “up and down” as needed to source 1 mA. The compliance voltage of this current source is 0.7 V. If the load requires greater than 5 volts to consume 1 mA, (5.7 minus the compliance voltage of 0.7) the current source cannot provide 1 mA.

The compliance voltage for the PSoC 3 and PSoC 5LP devices are available in the device datasheet.

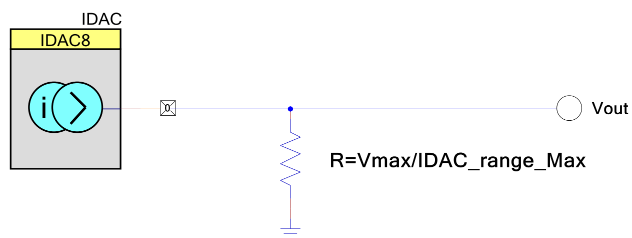
Figure 1. Simple Current Source



2 “Any Range” VDAC from IDAC and Resistor

To generate the 0 to 200 mV range with an IDAC, implement the circuit shown in Figure 2.

Figure 2. Simple VDAC from IDAC



The resistor is selected based on the maximum output voltage desired and the maximum current that can be sourced by the IDAC in its selected mode (see Equation 1). For example, if the 32 µA range is selected, you need a 200 mV/32 µA = 6.25 kΩ resistor.

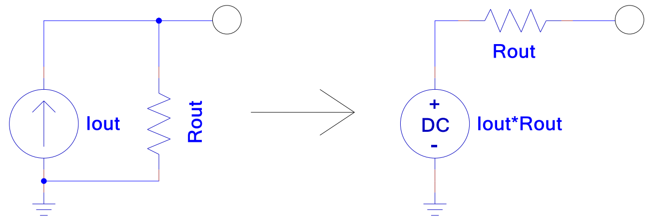
$$R = \frac{V_{max}}{IDAC_{range\max}} \quad \text{Equation 1}$$

If you do not want your desired voltage to be affected by the load connected, make your drive circuit’s output impedance very low compared to the input impedance of the load. How low the output impedance needs to be is up to you, the circuit designer.

The Norton and Thevenin equivalent circuits are useful tools to determine the output impedance of a circuit. Using an IDAC as a VDAC lends itself well to analysis as a Norton circuit.

You can change the Norton equivalent circuit (current source in parallel with a resistor) into a Thevenin equivalent circuit (voltage source in series with a resistor) using the conversion in Figure 3. This allows to easily see the effective output impedance of the circuit.

Figure 3. Norton to Thevenin Conversion



This means that the “VDAC” has an equivalent output impedance of 6.25 kΩ. In some cases, this output impedance may be too high. If you increase the IDAC output range from 32 µA to 2.040 mA, the same 0 to 200 mV range will require a 98-Ω resistor, which reduces the output impedance by a factor of 64 (6.25 kΩ to 98 Ω).

Using this method to generate a voltage you can:

- Generate a voltage referenced to ground by sourcing current into a resistor connected to ground. *Do not forget the compliance voltage.*
- Generate a voltage referenced to the power rail (≤ Vdda) by sinking current from a resistor connected to the power rail. *Do not forget the compliance voltage.*
- Select any of the current ranges to suit your applications specific needs depending on:
  - Desired output impedance: a higher current means a lower output impedance for a given voltage range.
  - Desired power consumption: lower current ranges use less power for the same generated voltage.

3 Dynamic Voltage Range Adjustments

The ability to change the generated voltage range dynamically is valuable. If you set your midrange voltage from 0 to 500 mV by selecting the 255 µA current range and selecting a 1.96 kΩ conversion resistor, you can:

- Change the current range to 32 µA using the API and the output range changes to 0 to 62 mV
- Change the current range to 2.048 mA using the API and the output range changes to 0 to 4 V

A dynamic voltage range adjustment provides the ability to change the range of the voltage generated by factors of eight without changing the external hardware.

4 Multiplying VDAC

Tying an ‘open drain drives low’ GPIO pin to the IDAC output gives you the ability to pulse width modulate the output current through a resistor. See Figure 4 and Figure 5 for an example. If the modulated output is then buffered and low pass filtered, the output approximates a multiplying VDAC where the duty cycle of the PWM is one (input1) input and the IDAC is the other input (input2). The output will be input1 × input2.

Figure 4. Multiplying VDAC

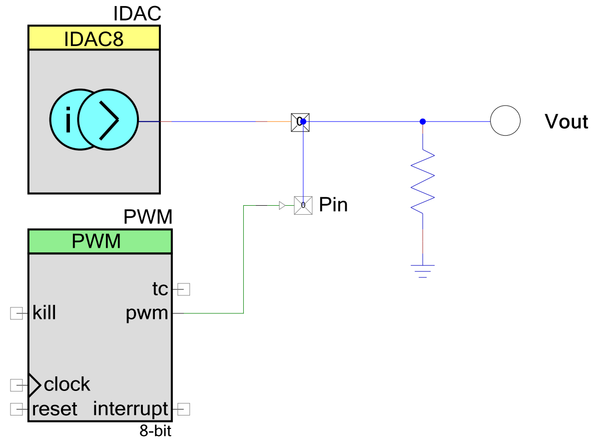
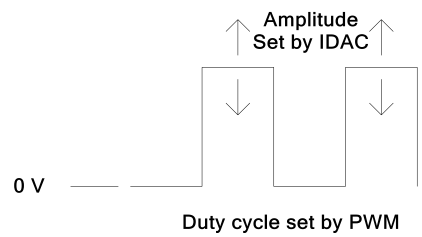


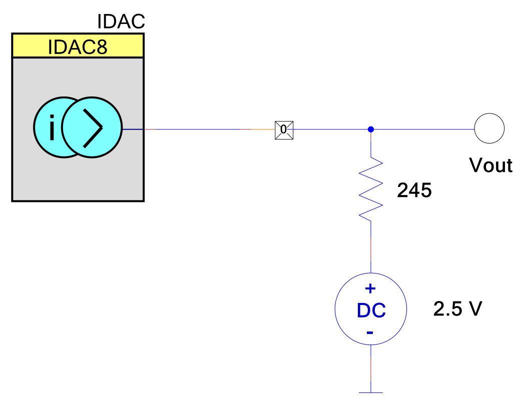
Figure 5. Output Waveform of Mixed Signal Multiplying VDAC



5 "Any Range and Any Ground" VDAC from an IDAC, Resistor and Buffer

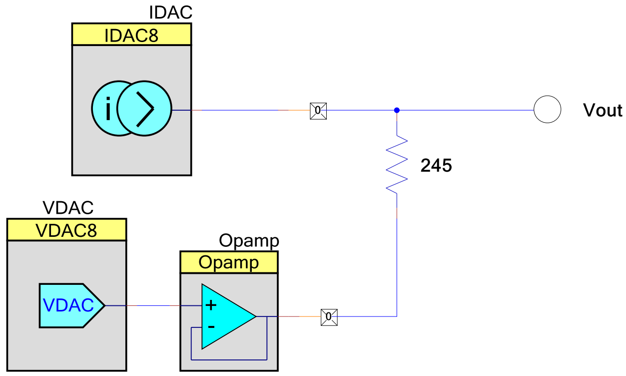
Perhaps you need a 65 mV range signal, but it needs to be referenced at 2.5 volts. Your 4 volt VDAC only gives you 16 mV per step, so your sensitive signal range only gets four steps around the 2.5 V range. A clever solution to this problem is to use an IDAC and resistor to generate the 65 mV voltage range, and then place the low side of the resistor to 2.5 volts. Figure 6 illustrates this using the 255 µA range and a 245-Ω resistor.

Figure 6. Any Range and Any Ground VDAC



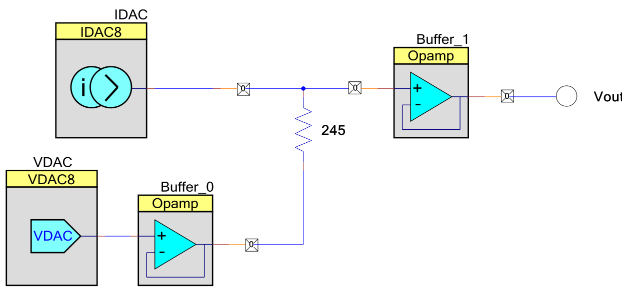
The easiest way to generate 2.5 volts is to use a VDAC, but be aware, the VDAC output resistance is not 0Ω, and the circuit will not behave as desired. Refer to the datasheet for equivalent output resistance for the different VDAC modes. To solve this problem, buffer the new "VDAC ground" signal as shown in Figure 7.

Figure 7. Any Range and Any Ground Implementation



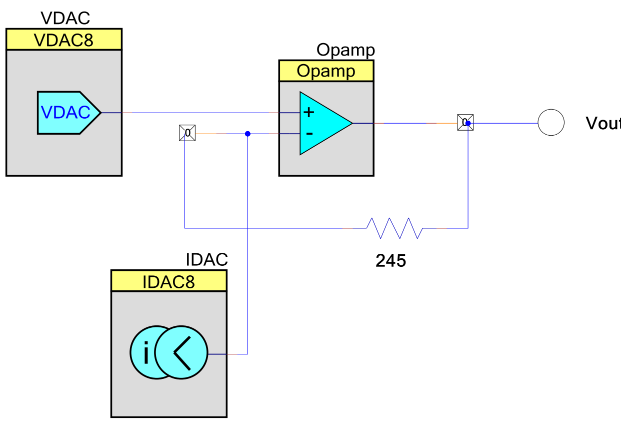
Furthermore, to ensure that the output signal has sufficiently low output impedance, buffer the output voltage as shown in Figure 8.

Figure 8. Any Range and Any Ground Implementation with Output Buffer



You can rearrange a few things, eliminate an opamp, and gain a few extra features in the process. Refer to Figure 9 for the updated topology.

Figure 9. Transimpedance Amplifier Implementation



The circuit in Figure 9 performs the same as the previous topology (any range, any ground, low output impedance). It saves an opamp, and the compliance voltage of the IDAC no longer has a significant impact on the output range. The IDAC sources current into the “negative input” of the opamp, which is kept at the same voltage as the output of the “ground” VDAC. Thus the desired output voltage no longer affects the IDACs ability to source current by cutting into its compliance range (as long as the ground voltage set by the VDAC does not violate the compliance voltage of the IDAC).

Remember that there is finite (non-zero) switch resistance from the IDAC output to the opamp input, which causes a minor voltage drop. However, the IDAC output can be kept within a few hundred millivolts of the VDAC setting (using proper IDAC current selection).

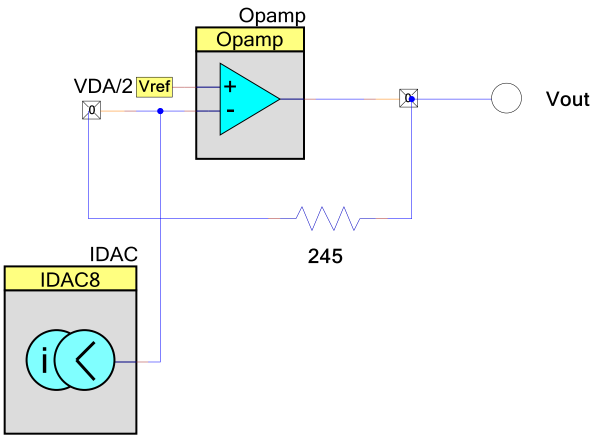
The polarity of the voltage will be opposite from the previous topologies, but that is easily solved by setting the direction of the IDAC to sourcing or sinking. There is no significant downside to choosing a smaller IDAC range in this topology, so internal voltage drop can be eliminated by using the 32 µA range. The output equation is shown in Equation 2. Voltage increases (+) on Vout if the IDAC direction is "sinking" and voltage decreases (–) on Vout if the IDAC direction is “sourcing”.

$$V_{OUT} = V_{DAC} \pm I_{DAC} * 245\Omega \qquad \text{Equation 2}$$

The output impedance of the circuit will be zero and the output voltage range can go as close to the rails as the opamp will allow.

If a non-standard analog ground is not required (a ground that needs to be generated by a VDAC), then the internal reference voltages can be used to set an analog ground. To see the circuit, refer to Figure 10. Because the voltage reference is driven into the high-impedance input of an opamp, it is not necessary to buffer the relatively weak reference voltages.

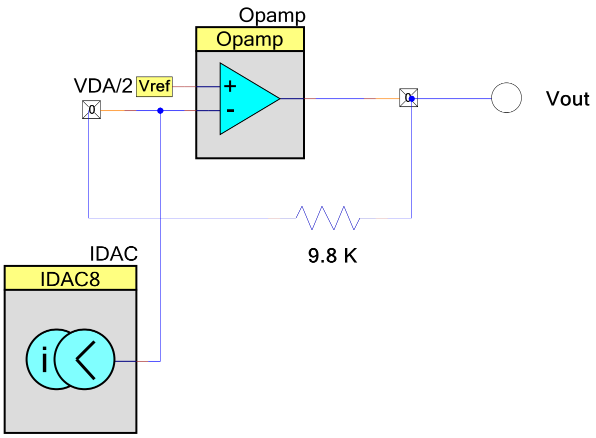
Figure 10. Transimpedance Amplifier VDAC Biased at VDDA/2



6 Rail-to-Rail 9-Bit VDAC with Low Output Impedance

The topology of the circuit in Figure 10 allows to turn an 8-bit IDAC, a resistor, and an opamp into a rail-to-rail, low-output impedance 9-bit VDAC. With a 5-V system as an example, use VDDA/2 as the voltage into the non-inverting terminal of the opamp shown in Figure 10. You can then select the 255 µA current range and choose a resistor that gave us half of our range (2.5 volts) at full scale on the IDAC (2.5 V / 255 µA = 9.8 kΩ). See Figure 11 for more information. Check the relevant datasheet specification to determine how close to the rails the opamp can go.

Figure 11. 9-Bit Voltage DAC Hardware



When the components are connected as shown in Figure 11, you can generate voltages from 0 to 5 volts by changing the direction of the IDAC. The direction can be changed through software or hardware, depending on the configuration. Table 1 gives a few examples to show how to reach the entire voltage range with this topology.

Table 1. Voltage Output With Sinking and Sourcing IDAC into a VDDA/2 Biased TIA

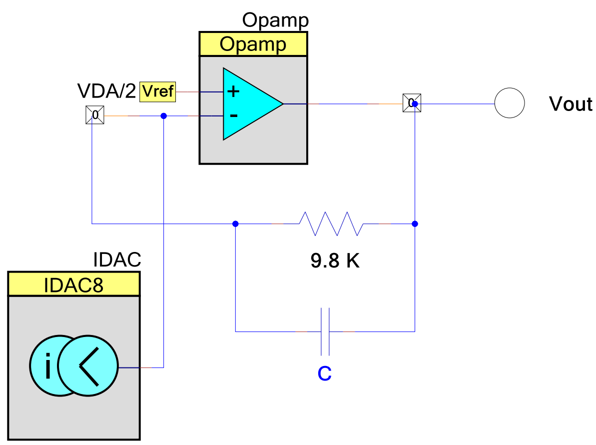
IDAC Current Setting	IDAC Direction	Output Voltage
255 µA	Sourcing	0
192 µA	Sourcing	0.618
128 µA	Sourcing	1.245
64 µA	Sourcing	1.872
0 µA	Sourcing/Sinking	2.5
64 µA	Sinking	3.127
128 µA	Sinking	3.754
192 µA	Sinking	4.382
255 µA	Sinking	5

Changing the IDAC direction allows you to turn an 8-bit IDAC into a 9-bit VDAC (255 steps above VDDA/2 and 255 steps below VDDA/2), with just an opamp and a resistor. Adding a capacitor in parallel with the resistor, as shown in Figure 12, provides a low pass filter on the output with a cutoff frequency set by Equation 3.

$$f_c = \frac{1}{2\pi RC}$$ Equation 3

To ensure the best accuracy, load the proper calibration values when the IDAC direction or range is switched. This can be done with software or DMA.

Figure 12. 9 Bit VDAC with Integrated Low Pass Filter

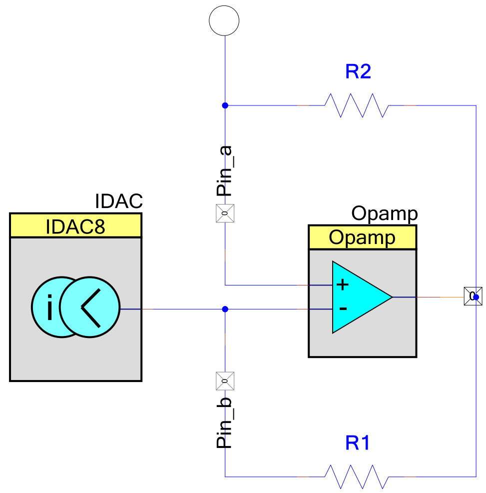


7 IDAC Current Multiplier

If you need a special IDAC range that the PSoC 3 and PSoC 5LP cannot reach with its three modes, then using an opamp and two resistors, make the current scaling circuit shown in Figure 13. Equation 4 governs the output current.

$$I_{out} = I_{DAC} * \frac{R_1}{R_2}$$ Equation 4

Figure 13. Current Multiplier Circuit



In this circuit, the output current has the opposite polarity of the IDAC. Remember these design considerations:

- The ratio of the resistors sets the current scale. For example, if R1 = 10 kΩ and R2 = 20 kΩ, the circuit will behave the same if R1 = 1 Ω and R2 = 2 Ω.
  - If the resistors are large (greater than 1 kΩ), then there is a significant voltage drop across them. Take care to ensure that the opamp has sufficient headroom to operate. However, large resistors are more tolerant of input offset voltage introducing error (as an offset current) into the current ratio.
  - If the resistors are small (less than 100 Ω), then there is more headroom to operate, because the voltage drop across the resistors are small. However, the error introduced by the input offset voltage of the opamp will be more significant.
- The load connected to the output node determines the voltage that the circuit will operate at. Take care to ensure that the IDAC compliance voltage is not violated and that the opamp has sufficient headroom to operate.

8 Summary

This application note presents few of the many possible ways you can use the highly flexible IDACs in PSoC 3 and PSoC 5LP. With these versatile tools, you can create unique applications and uses that are simply not possible otherwise. PSoC Rocks!

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2897540	KEES	03/22/2010	New application note
*A	3095638	SDUR	11/26/2010	Changed title from ‘PSoC® 3 and 5 IDAC Tips and Tricks’ to ‘Using IDACs to Build a Better VDAC’.
*B	3182216	KEES	02/25/2011	Updated title to AN60305 - Using PSoC® 3 and PSoC 5 IDACS to Build a Better VDAC
*C	3936338	KEES	03/19/2013	Updated document title to read as “Using PSoC® 3 and PSoC 5LP IDACs to Build a Better VDAC - AN60305”. Replaced “PSoC 5” with “PSoC 5LP” in all instances across the document. Updated the document template.
*D	4328303	KEES	03/31/2014	Sunset ECN, no change
*E	4521050	KEES	10/08/2014	Fixed the template. Removed the About the Author section.
*F	5232333	SJLE	04/20/2016	Sunset ECN, no change for application note contents. Removed an obsolete e-mail link and then added a proper Cypress supporting web page. Updated the product related links – Added PSoC 4 and ARM® Cortex®
*G	5700131	AESATP12	04/20/2017	Updated logo and copyright.

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