AN13652

Schematic Review Checklist for West Bridge® Antioch™

Associated Project: No
Associated Part Family: West Bridge
Software Version: Antioch SDK 1.0, 1.1, 1.2, 1.3
Related Application Notes: None

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/AN13652.

West Bridge® Antioch™ is a USB mass storage control device that contains three main ports: processor interface (P-port), mass storage support (S-port), and USB Interface (U-port). This application note discusses the hardware recommendations and guidelines for designing a system using Antioch.

Introduction

The West Bridge® Antioch™ device (CYWB0124AB) is a peripheral controller that supports high-speed USB and mass storage access. This controller provides access from both a processor interface and a high-speed USB (HS-USB) interface to peripherals including SD, MMC/MMC+, CE-ATA, and NAND. It supports interleaving accesses between the processor interface, the HS-USB, and the peripherals. This enables both an external processor and an external USB host to transfer data simultaneously to each other, and to the mass storage peripherals.

Following are the hardware considerations for designing Antioch into a system.

P-Port

1. If operating in the asynchronous mode, CLK is tied LOW through a 10 k resistor. If operating in synchronous mode, CLK is connected to the incoming CLK signal from the processor interface.
2. ADV# is tied to a signal on the processor interface that conforms to the timing in the datasheet West Bridge: Antioch USB/Mass Storage Peripheral Controller. If this signal is not available, tie ADV# to the CE# signal of the processor interface as described in the application note, *AN13553 - Using Processor Chip Enable as Address Valid Input to Antioch™*.
3. All unused inputs and I/O pins on the P-port are tied to a valid logic level (HIGH for lowest leakage) through a 10 k resistor. You can use a single resistor for multiple unused pins. When pulling HIGH, the unused pins are tied to the appropriate power domain: in this case, PVDDQ.
4. The DRQ Status Register and DRQ Mask Register indicate the available endpoints for transfer. They must be accessed even if a DMA or burst operation is not being implemented on the P-port interface. Use the DRQ# or the INT signal to indicate to the processor that at least one of the bits in the DRQ Status Register is set. If INT is used, an extra read of the P-Port interrupt register must be done before the DRQ Status Register is read.
5. DACK# is used in conjunction with DRQ#. If INT is used to indicate that at least one bit is set in the DRQ Status Register, then DACK# remains unused. DACK# is not required for Antioch to function.
6. The INT and DRQ# signals float when Antioch is in Standby state. These signals are active low. As a result, a pull-up resistor must be connected to these signals to prevent the P-port processor from receiving any false interrupts.
7. The WAKEUP pin should be connected to an externally controllable output (processor GPIO) with a pull-up resistor attached.

S-Port

1. You can use SD_D[3] or GPIO[0] to detect cards on Antioch. A 470 kΩ pull-down resistor is required for SD_D[3].
2. Do not leave any floating unused input-only or I/O pins. Tie all unused pins HIGH through a single 10 k resistor to the appropriate SSVDDQ or SNVDDQ supply. The CMD pin and DATA lines require a 10 k pull-up resistor when used.
3. You can treat the SD_CLK signal as a high-speed signal switching at 48 MHz to determine the appropriate signal integrity precautions.

4. The SD_POW signal floats when Antioch is in standby. If this signal is used to control power to the SD card through an external switch, a pull-up or pull-down resistor must be connected on SD_POW. This ensures that the switch remains on and power to the card is retained during Antioch's standby condition.
5. If you are designing for an application supporting SD/MMC and CE-ATA, follow the trace length restrictions.

Table 1 lists the acceptable frequencies for Antioch and the maximum trace lengths corresponding to the frequencies for SD cards that cannot operate in high-speed mode.

Table 1. Frequency vs. Trace Length (SD Default Mode)

SDFREQ (MHz)	Maximum Trace Length (in)
24.00	1.94
21.82	7.55
20.00	13.17
18.46	18.78
17.14	24.4

Table 2 lists the acceptable frequencies for Antioch, the perspective, and the corresponding maximum trace lengths for SD cards that are capable of operating in high-speed mode.

Table 2. Frequency vs. Trace Length (SD High-speed Mode)

SDFREQ (MHz)	Maximum Trace Length (in)
48.00	8.18
40.00	20.66
34.29	33.13
30.00	45.61
26.67	58.08

U-Port

1. To avoid an impedance mismatch, lay out the USB differential signals with constant spacing and on one plane. Avoid vias and stubs. It is prudent to lay out the signals before laying out the rest of the board.
2. Minimize the trace lengths between the D+ and D- pins on Antioch and the USB connector. For CYWB0124ABX-FDXI, a trace length of less than two inches is required to pass USB certification.
3. The UVALID signal mirrors the value of a register bit in Antioch. The register bit is written to using firmware. The main processor in the system can use UVALID to control the external power management ICs or USB switches. Its behavior during reset and low power modes is documented in the datasheet. UVALID is not required for Antioch to function.
4. If you plan to use an USB switch, contact your local sales representative or use the Cypress Connection Center to determine the best option. Further information can be found in the application note, AN42961 - Using a USB Switch with West Bridge® Antioch™.
5. For further information, see application note, *AN1168 - High Speed USB PCB Layout Recommendations*.

Clocks

1. Ensure that the XTALSLC[1:0] pin levels correspond to the frequency of the signal at XTALIN and XTALOUT.
2. Leave the XTALOUT floating if an external clock source is used.
3. Clock or crystal characteristics must conform to the requirements specified in the datasheet.
4. Further information about clock requirements can be found in this application note, AN49081 - Requirements for Input Clock to West Bridge Devices.
5. You must adhere to the power supply noise specifications for the PLL specified in the datasheet.
6. XVDDQ is the select pin for crystal and clock. XVDDQ must be 3.3 V when using a crystal. XVDDQ must be 1.8 V when using a clock source as an input.

Table 3 lists the various clock selection input settings.

Table 3. Clock Selection Input Settings

XTALSLC[1]	XTALSLC[0]	Clock Frequency	Crystal Support
0	0	19.2 MHz	Yes
0	1	24 MHz	Yes
1	0	48 MHz	No
1	1	26 MHz	Yes

Decoupling for Power Supplies

1. V_{DD} requires 2.2 µF and 0.1 µF decoupling.
2. Although AVDDQ is tied to the same supply as VDD, route it separately with 0.01 µF and 0.1 µF capacitors.
3. UVDDQ requires 2.2 µF and 0.1 µF decoupling.
4. GVDDQ, PVDDQ, SSVDDQ, SNVDDQ, and XVDDQ do not have any specific decoupling requirements; combine them with decoupling for other supplies at the same level. If in doubt, use 2.2 µF and 0.1 µF.
5. Ensure that in the Core power down mode, when the VDD power supply is turned down, there is a 1 kΩ resistance between the V_{DD} and ground.

Miscellaneous

You may leave all the unused output-only pins floating, but do not leave unused input-only and I/O pins floating. Tie the input-only and I/O to a valid logic level using a single 10 k pull-up resistor. There is a negligible difference if the unused input-only pins are tied HIGH or LOW. For lowest leakage, tie unused I/O pins HIGH.

An easy solution is to tie all unused inputs and I/O HIGH through a single 10 k pull-up resistor. Ensure that all unused pins handled this way are tied to their corresponding power domain. For example, an unused GPIO[1] is tied HIGH to GVDDQ through a 10 k pull-up which is shared with other unused signals in the GVDDQ domain.

If standby mode is not used in your design, WAKEUP should be tied high through its own 10 k resistor or through a 10 k resistor shared only with input-only pins. Tying this pin high through a resistor shared with I/O pins can lead to unstable operation.

To prevent floating GPIO input from resetting the West Bridge inadvertently, we recommend placing a pull-up on the RESET input line.

Additional Resources

- West Bridge® Antioch™ Advance Datasheet
- AN13553 - Using Processor Chip Enable as Address Valid Input to Antioch™
- AN42961 - Using a USB Switch with West Bridge® Antioch™
- AN49081 - Requirements for Input Clock to West Bridge® Devices
- AN1168 - High-Speed USB PCB Layout Recommendations

Summary

This application note began with the explanation on three interfaces available in Antioch peripheral controller namely P-Port, S-Port and U-Port.

Then, it discusses the hardware recommendations and guidelines for designing a system using Antioch.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	851520	DSG	03/22/2007	New application note.
*A	1733043	OSG	11/12/2007	Updated to new template.
*B	2620808	OSG / AESA	12/12/2008	Changed title to “Schematic Review Checklist for West Bridge® Antioch™”. Updated P-port and S-port sections.
*C	2650159	ODC	01/30/09	Added clarification on the USB trace length in the U-Port section.
*D	2742382	ODC	07/22/09	Added information on Wakeup pin in the P-Port section.
*E	3183375	ANOP	02/27/2011	Added Table 3 under Clocks. Added Additional Resources. Other minor updates across the document.
*F	3417871	AASI	10/21/2011	Updated to new template. Completing Sunset Review.
*G	4566134	PRJI	11/10/2014	Updated to new template. Completing Sunset Review.
*H	5840663	GNKK	08/01/2017	Updated the Cypress logo and copyright information

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