AN89371

Power Saving with Cypress's 65-nm Asynchronous PowerSnooze™ SRAM

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This application note explains the PowerSnooze™ feature of Cypress's 65-nm asynchronous fast SRAM devices (CY7S10xxG family). PowerSnooze allows the SRAM to enter a low-power mode during long chip disable periods. A user-controlled pin ($\overline{DS}$) enables a seamless transition between high-speed mode and low-power mode. This application note also describes critical timing parameters for the mode transitions as well as a sample SRAM interface configuration to use the PowerSnooze feature in application systems.

Introduction

With the advent of mobile technology and portable battery-backed devices, power consumption has become one of the key factors in system design. System designers face the dilemma of selecting between faster operating speeds and lower power consumption for the microcontrollers/ASICs, peripherals, and memory devices in their systems.

Microcontrollers from Texas Instruments and NXP Semiconductors have special low-power modes such as deep power-down and deep sleep. Applications running on these controllers can use these features to save power. The controller can run at full speed during normal operation but go into low-power mode afterwards, saving power. During this low-power mode, peripherals and memory devices are also expected to save power, which is a challenge to memory devices interfaced to such systems. Asynchronous SRAMs are typically used as off-chip cache memories, scratch pad memory, or other similar scenarios that need faster access times on the order of tens of nanoseconds.

Fast SRAMs offer access times between 10 ns and 20 ns but consume significant power during both active and standby modes. The low-power SRAMs, on the other hand, have slower access times of about 45 ns to 70 ns. Traditionally, system designers have used low-power SRAMs in low-power applications, but today, they need both: fast access times for their memory interface as well as low power consumption when their system is idle.

Cypress's 65-nm asynchronous SRAMs with the PowerSnooze™ feature offer the best of both worlds to make a true high-speed, low-power device.

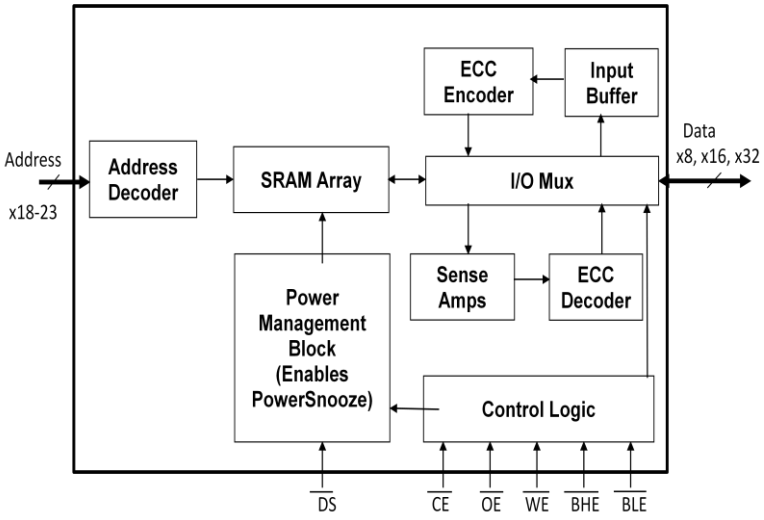
A True Fast, Low-Power Asynchronous SRAM

Cypress's 65-nm asynchronous SRAM with the PowerSnooze feature allows system designers to enjoy the benefits of fast access time and low-power consumption in the same chip. Cypress SRAMs with the letter "S" in their ordering code (for example, CY7S1061G30), which stands for 16-Mb asynchronous fast PowerSnooze SRAM, have an additional input pin, called $\overline{DS}$, that is apart from the conventional asynchronous SRAM interface. This pin is user controlled, which allows users to change the operating modes of SRAM on the fly.

During normal operation, the controller/ASIC/FPGA[1] can access SRAM data at a full speed of 100 MHz (access time of 10 ns). However, when the controller enters low-power modes, it can control the $\overline{DS}$ pin to put the SRAM in deep-sleep mode. In deep-sleep mode, these SRAMs consume a current of 22 µA at 85 ºC for a 16-Mb SRAM, making this device a true high-speed, low-power device. Figure 1 shows a simplified architecture of a PowerSnooze SRAM.

[1] The terms "controller," "ASIC," "microcontroller," and "FPGA" are used interchangeably in this document.

Figure 1: Asynchronous PowerSnooze SRAM Architecture



Modes of Operation

As shown in Figure 1, PowerSnooze SRAMs have an additional power management block that allows users to operate the SRAM in the following three modes:

- Active mode
- Standby mode
- Deep-sleep mode

Active Mode

When the $\overline{DS}$ pin is in a logic HIGH state and SRAM is enabled ($\overline{CE}$ is logic LOW[2]), then it is in active mode. In this mode, the device can operate with an access time of 10 ns, and it will consume active current I_{CC} (typically in the order of milliamps). Refer to the SRAM datasheet for the timing and DC parameters.

Standby Mode

When the $\overline{DS}$ pin is in a logic HIGH state and SRAM is disabled ($\overline{CE}$ is logic HIGH[2]), the SRAM is in standby mode, also referred to as "chip disable mode." In this mode, no access is allowed to the SRAM; it will consume standby current I_{SB2} (typically in milliamps, but an order less than active current). Data stored in SRAM prior to entering this mode will be retained while it is in the standby mode. Refer to the SRAM datasheet for standby mode conditions.

Deep-Sleep Mode

Cypress offers the PowerSnooze feature in both 4-Mb and 16-Mb asynchronous SRAMs. These two densities involve a minor difference in the way deep-sleep mode is entered and exited. Systems designed with 4-Mb PowerSnooze SRAMs will need minor firmware changes when upgrading to 16-Mb PowerSnooze SRAMs. Systems designed with 16-Mb PowerSnooze SRAM can use 4-Mb PowerSnooze SRAMs with no firmware changes. The following sections explain the deep-sleep mode for 16-Mb and 4-Mb SRAMs in detail.

[2] For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE2 is LOW, $\overline{CE}$ is HIGH.

Deep-Sleep Mode for 16-Mb SRAM

The 16-Mb PowerSnooze SRAM can enter the deep-sleep mode only from standby mode ($\overline{CE}$ is logic HIGH[2]). After the chip is disabled for at least t_{CEDS} time, the $\overline{DS}$ pin must be asserted (to logic LOW) to enter deep-sleep mode. Refer to Figure 2 for the timing requirements. On assertion of the $\overline{DS}$ pin (to logic LOW), the SRAM enters deep-sleep mode after t_{DS} time. During deep-sleep mode, $\overline{DS}$ must remain asserted and the SRAM must remain in standby mode ($\overline{CE}$ is logic HIGH). While entering deep-sleep mode (t_{CEDS} + t_{DS} time), SRAM will consume standby current I_{SB2}; once in deep-sleep mode, it will consume the deep-sleep current I_{DS}.

To exit the deep-sleep mode, the $\overline{DS}$ pin must be deasserted (to logic HIGH[2]) while SRAM is still disabled. SRAM will take t_{DSCE} time to return to standby mode. After t_{DSCE} time, SRAM can be enabled ($\overline{CE}$ to logic LOW[2]) to enter active mode.

It must be noted that any violations of these timing parameters do not guarantee successful entry to or exit from deep-sleep mode. Refer to Table 1 for a summary of the timing requirements.

Deep-Sleep Mode for 4-Mb SRAM

The 4-Mb PowerSnooze SRAM can enter the deep-sleep mode either from standby mode ($\overline{CE}$ is logic HIGH[2]) or active mode. On assertion of the $\overline{DS}$ signal (to logic LOW[2]), the SRAM starts its transition to deep-sleep mode. If $\overline{DS}$ continues to be asserted for at least t_{DS} time, the SRAM enters deep-sleep mode and consumes deep-sleep current I_{DS}. Refer to Figure 3 for the timing requirements. During deep-sleep mode, $\overline{DS}$ must remain asserted. While entering deep-sleep mode (t_{DS} time), SRAM will consume standby current I_{SB2}; once in deep-sleep mode, it will consume the deep-sleep current I_{DS}. If the $\overline{DS}$ signal gets asserted during a write operation, then the SRAM cannot guarantee successful operation, as the device starts transitioning to deep-sleep mode.

To exit the deep-sleep mode, the $\overline{DS}$ pin must be deasserted (to logic HIGH). If $\overline{DS}$ is asserted for at least t_{PDS} time, then SRAM will be disabled internally for t_{DSCD} time. This time (t_{DSCD}) allows the external controller to access $\overline{CE}$ and disable it externally. The device must continue to be disabled until t_{DSCA} time. After t_{DSCA} time from the deassertion of $\overline{DS}$, SRAM can be accessed by enabling it ($\overline{CE}$ to logic LOW) to enter active mode. If t_{PDS} is not met by the system, then t_{DSCD} is not guaranteed by the SRAM. During this period (when t_{PDS} < $t_{PDS(min)}$), SRAM must be disabled externally until t_{DSCA} time to avoid corruption of the SRAM data. Refer to Table 2 for a summary of these timing requirements.

Figure 2. Deep-Sleep Mode for 16-Mb SRAM – Entry and Exit Sequence

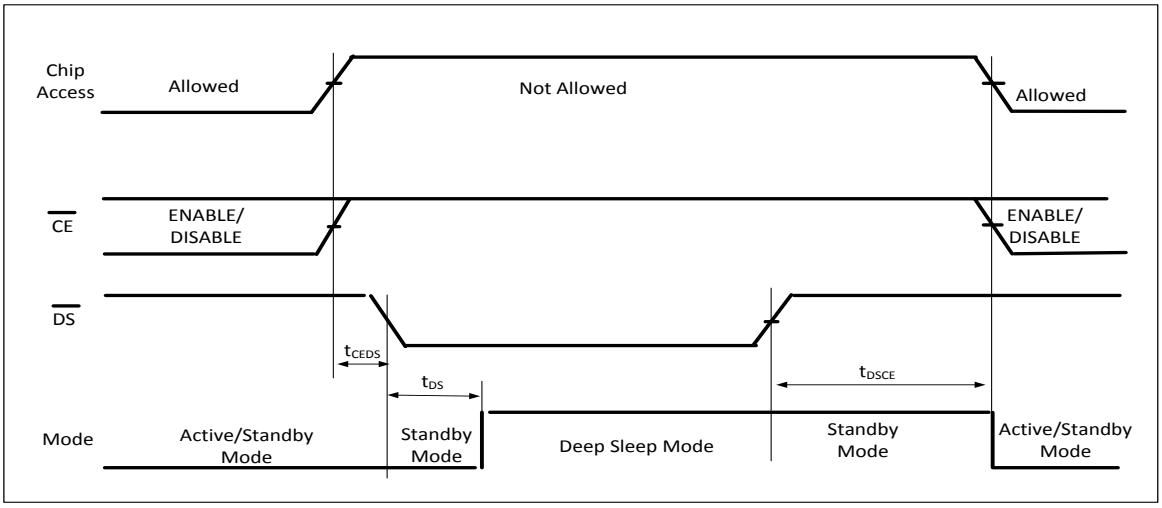


Table 1. Key Timing Parameters for 16-Mb PowerSnooze SRAM

Parameters	Description	Timing	
		Min	Max
t_{CEDS}	Time between deassertion of $\overline{CE}$ and assertion of $\overline{DS}$	100 ns	–
t_{DS}	$\overline{DS}$ assertion to deep-sleep mode transition time	–	1 ms
t_{DSCE}	Time between deassertion of $\overline{DS}$ and assertion of $\overline{CE}$	1 ms	–

Figure 3. Deep-Sleep Mode for 4-Mb SRAM– Entry and Exit Sequence

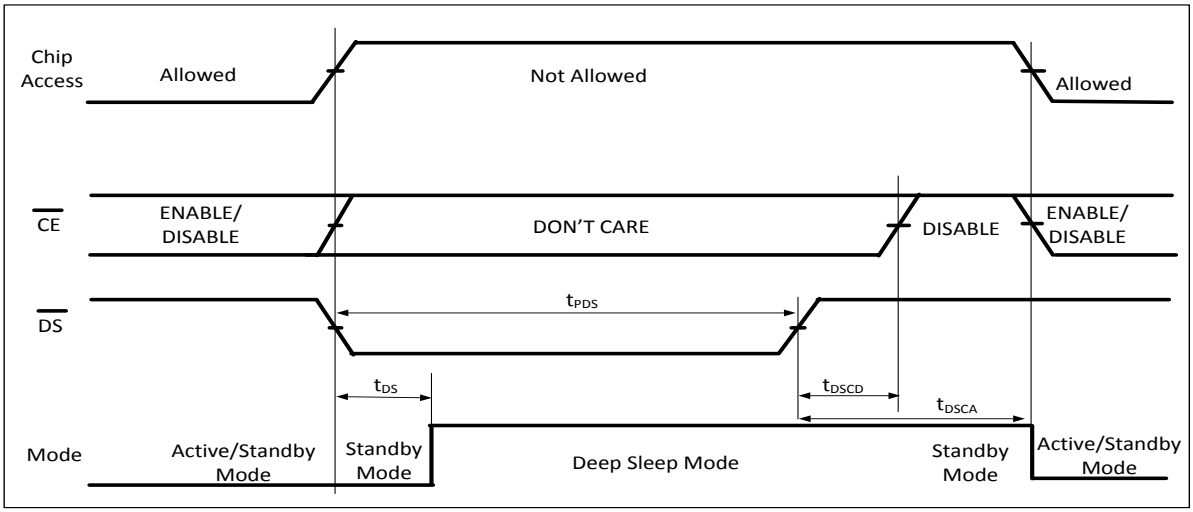


Table 2. Key Timing Parameters for 4-Mb PowerSnooze SRAM

Parameters	Description	Timing	
		Min	Max
t_{PDS}	Minimum time for $\overline{DS}$ to be LOW for part to successfully exit deep-sleep mode	100 ns	–
t_{DS}	$\overline{DS}$ assertion to deep-sleep mode transition time	–	1 ms
t_{DSCD}	Time between deassertion of $\overline{DS}$ and chip disable (if $t_{PDS} \geq t_{PDS(Min)}$)	–	100 µs
	Time between deassertion of $\overline{DS}$ and chip disable (if $t_{PDS} < t_{PDS(Min)}$)	–	0 µs
t_{DSCA}	DS# deassertion to chip access (active/standby) (if $t_{PDS} \geq t_{PDS(Min)}$)	300 µs	
	DS# deassertion to chip access (active/standby) (if $t_{PDS} < t_{PDS(Min)}$)		

As the SRAM is disabled for the entire period when it is in deep-sleep mode, data stored in SRAM prior to entering this mode is retained. Refer to the SRAM datasheet for the deep sleep-mode conditions. Table 1 and Table 2 summarize the key timing parameters that must be followed for PowerSnooze SRAMs.

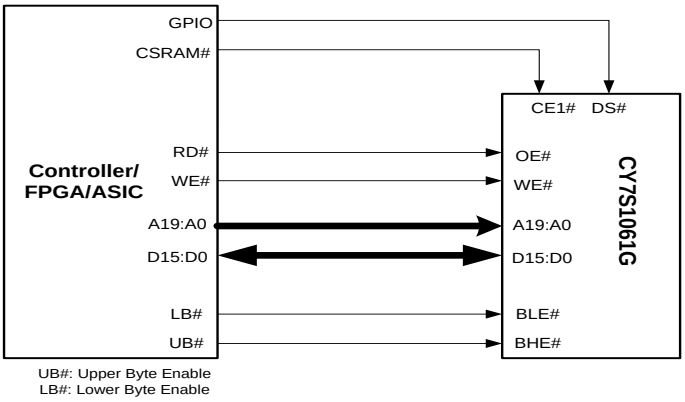
Interfacing PowerSnooze SRAM in Systems

High-end microcontrollers like AM18XX series from TI or LPC 177X/LPC178X series from NXP have special deep-sleep modes that the controller can enter to save power consumption. TI's AM18XX series controllers have an input signal, called $\overline{\text{DEEPSLEEP}}$, which can put the controller in low-power mode. This signal can be interfaced with the $\overline{\text{DS}}$ pin of PowerSnooze SRAMs. The LPC177x/178x series controller can enter low-power mode though a software configuration, which sequentially disables the peripherals and memory devices connected to it. This sequence can be used to generate an extra signal apart from normal SRAM interface signals to control the $\overline{\text{DS}}$ pin of PowerSnooze SRAMs.

In situations where system designers intend to use PowerSnooze SRAMs in existing applications or want to interface to an ASIC or microcontroller without a special low-power mode, the $\overline{\text{DS}}$ pin can be controlled with a normal GPIO. Figure 4 illustrates an interfacing scenario where a GPIO is interfaced to the $\overline{\text{DS}}$ pin of the PowerSnooze SRAM. During active and standby modes, the $\overline{\text{DS}}$ pin should always be at logic HIGH.

To enter deep-sleep mode, the microcontroller must follow the timing sequences explained in the previous section for $\overline{\text{CE}}$ and $\overline{\text{DS}}$. Thus, by performing minor modifications in the software and hardware, system designers can use the PowerSnooze SRAM in existing applications.

Figure 4. Interfacing PowerSnooze SRAM



Summary

Cypress's asynchronous PowerSnooze SRAM offers the best of both worlds—a fast and low-power SRAM. PowerSnooze SRAMs are available in multiple options and packages. Table 3 summarizes the 16-Mb and 4-Mb PowerSnooze SRAM product portfolio. Refer to the datasheet for information on choosing the right configuration and ordering.

Table 3. PowerSnooze SRAM Product Portfolio

Parameters	PowerSnooze SRAMs (High-Speed Low-Power)	
	16 Mb	4 Mb
Temperature range	–40 °C to +85 °C	–40 °C to +85 °C
Technology	65 nm	65 nm
Operating current I_{CC} (max)	110 mA	45 mA
Standby current I_{SB2} (max)	30 mA	8 mA
Deep-sleep current I_{DS} (max)	22 µA	15 µA
Packages	48-pin TSOP I , 54-pin TSOP II, 48-ball VFBGA	44-pin TSOP I, 44-pin SOJ, 36-pin SOJ, 48-ball VFBGA
Speed	10 ns	10 ns
Copper lead frame	Yes	Yes
Pb free and leaded	RoHS	RoHS
Availability	Production	Sampling

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Background Nilesh Badodekar has a Master's degree in Visual Information Processing and Embedded Systems from I.I.T. Kharagpur, India.

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4364981	NILE	04/29/2014	New Application Note.
*A	4623709	NILE	03/30/3015	Added details about Cypress's 4-Mb PowerSnooze SRAMs. Added Table 1 and Table 2 Updated Table 3 for specifications of 4-Mb PowerSnooze SRAMs. Updated template

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