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AN5044

EZ-USB Hubs (CY7C656XX) PCB Design Recommendations

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To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/AN5044.

AN5044 presents recommendations for designing with the Cypress Semiconductor CY7C65640A, CY7C65630, and CY7C65620 components. Techniques for high-speed design must be applied to circuits using these components. Due to the packaging and high performance characteristics of the hub chips, it is recommended that applications consider the PCB thermal design.

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Introduction

Cypress's TetraHub™ is a high-performance universal serial bus (USB) 2.0 Hub. The Cypress architecture provides three configurations of this chip.

Cypress Semiconductor's CY7C65640A TetraHub™ Component

Figure 1. TetraHub

The Cypress architecture provides three configurations of this chip. The first is the CY7C65640A with four downstream USB ports, with a transaction translator for each port, making it the highest performance hub possible. This single-chip device incorporates one upstream and four downstream USB transceivers, a Serial interface engine (SIE), USB Hub controller and repeater, and four transaction translators (TT). The second version of the hub chip (CY7C65630) utilizes a single transaction translator for all four downstream ports. The third version is a 2-port version for bus-powered applications. All of these are suitable for standalone hubs, motherboard hubs, and monitor hub applications.

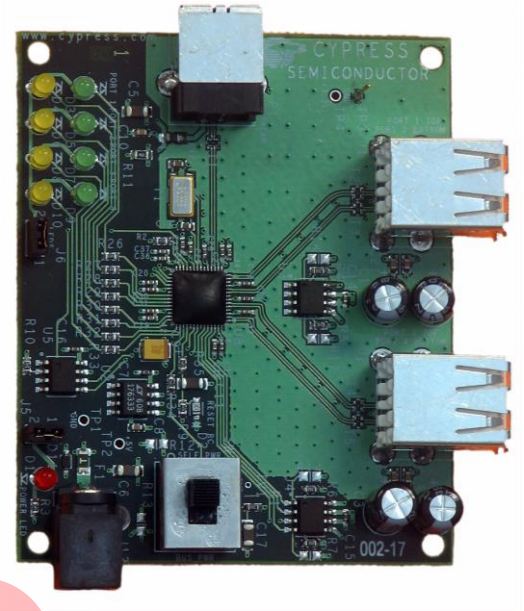
This family of hubs integrates many passive components, previously external to hub silicon. USB data line impedance matching resistors, downstream pull-down resistors, upstream speed signaling resistors, and phase-locked loop support circuits are integrated within the TetraHub family of components. This integration eases PCB layout.

For systems with large numbers of full-speed data transfers, optimum performance is achieved using the four transaction translators (TT), which are part of the Cypress CY7C65640A architecture. The USB specification requires a minimum of one TT. However, when a single TT hub operates with a mix of full-speed and low-speed devices, the sum of usable bandwidth is limited to that of a single full-speed port. When these are devices like keyboards or mice, the data is a low portion of the total bandwidth and a single TT versus a multiple TT makes little difference. When the full speed devices are near the maximum full-speed bandwidth, the multi-TT hub is optimum for performance. With the single TT all full-speed devices would share the bandwidth allotted a single full-speed device. With the multiple TT of the Cypress CY7C65640A architecture, each full-speed device may transfer data at rated full-speed.

CY4602A, CY4605, and CY4606 TetraHub Reference Designs

A complete design using the Cypress Semiconductor CY7C65640A TetraHub, the CY7C65630, and the CY7C65620 are available. The designs implement the recommendations of this application note. It may be useful for the reader to download the CY4602A, CY4605, or the CY4606 Reference Design Files from the Cypress Support page for Reference Designs.

Figure 2. Four-Port Hub



Cypress offers the TetraHub reference designs as an evaluation platform for developers wishing to integrate a USB 2.0 hub into their application. The designs are examples of a self-powered, 4-port USB 2.0 hub or a bus powered, 2-port hub. The kits includes the hub evaluation board, USB cable, power supply, schematics, bill of material, PCB Gerber files, and other documentation.

Package Description

The component is packaged as a 56-pad, 8-mm by 8-mm, 1-mm high, QFN (Quad Flatpack No leads), lead-free package. Refer to the latest CY7C656XX TetraHub high-speed USB hub controller data sheets for the detailed package drawing. The data sheets are Cypress specification 38-08037 and 38-08019.

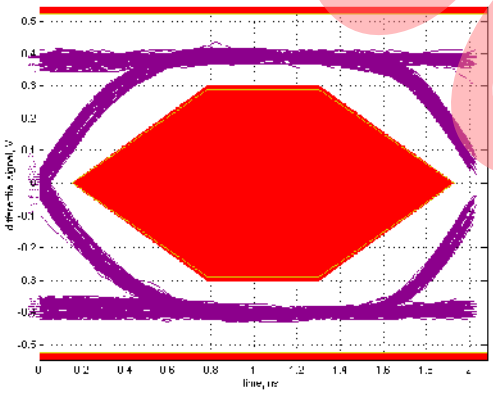
This package is, or is comparable to, the Amkor MicroLeadFrame™ package. It is a plastic encapsulated, near-chip scale package using solder lands instead of leads or balls. It uses a copper leadframe substrate that provides for short die to frame lead length giving good high-frequency performance. It has an exposed die paddle that enables good thermal transfer out of the package. For further details about this package and methods and processes associated with its assembly to a printed circuit board, refer to the manufacturer's application note identified in the References section of this document.

Electrical Design Recommendations

USB 2.0 high-speed signaling is used to transfer data at 480 Mbps. This rate is 40 times faster than the fastest speed of the USB 1.1 specification, full-speed signaling that operates at a 12-Mbps rate. High-speed signaling requires a greater level of attention to electrical design than previously required for USB designs. Careful attention to component selection, supply decoupling, signal line impedance, and noise are important considerations when designing for high-speed USB. Much of this is influenced by the PCB design; those physical issues are discussed in the PCB design recommendations section.

One key measurement of USB data signal quality is the eye pattern. The eye pattern is a representation of USB signaling that provides minimum and maximum voltage levels as well as signal jitter. Section 7.1 in the USB 2.0 Specification provides detailed explanation and requirements for a compliant eye pattern. Figure 3 is an eye diagram of high-speed signaling as measured on the CY7C656XX component.

Figure 3. CY7C656XX Eye Diagram of High-Speed Signaling



In the diagram, notice how no signal traces overlap the central, six-sided, shaded area. Also, no trace overlaps the extremes of permissible voltage as shown in the shaded lines at the very top and very bottom of the figure. Overlap of signal trace over the shaded areas would be a violation of the USB 2.0 specification. Overlap can be caused by excessive data jitter, mismatched impedance, and improper EMI filtering.

The Cypress Semiconductor application note titled *High-Speed USB PCB Layout Recommendations* treats the electrical design concerns applicable to high-speed USB 2.0 circuits. There are numerous textbooks that treat the subject of high-speed design in general. One such book is listed in the References section of this document.

Some areas of special note concerning design with high-speed hubs are discussed in the following sections.

CY7C656XX Device Supply Decoupling

Decoupling capacitors must be ceramic type of a stable dielectric. For lower value capacitance, it is appropriate to use Class 1 dielectric capacitors, C0G (also referred to as NPO). Class 2 X7R must be used for the larger values. Due to the quantity of high-speed USB data signal pairs on the TetraHub, is it recommended that a mix of 0.01-mF and 0.001-mF capacitors be used to decouple supply pins, nearest the five pairs of USB transceiver circuits. The 0.001-mF must be C0G dielectric. This will help decouple the power supply at the frequency range of high-speed USB switching. The other power supply pins must be decoupled with 0.1-mF X7R capacitors. It is important to have short trace runs for the power and ground connections from the TetraHub component to solid power and ground planes.

The specific recommendation for the ceramic capacitor nearest each CY7C656XX power pin is given in Table 1 below.

Table 1. Capacitor Recommendation

TetraHub Pin Number	Capacitor Value	TetraHub Pin Number	Capacitor Value
3	0.001 µF	23	0.01 µF
7	0.01 µF	27	0.1 µF
11	0.001 µF	33	0.1 µF
15	0.01 µF	39	0.1 µF
19	0.001 µF	55	0.1 µF
Addition bypass for CY7C65640A			
45	0.1 µF		

EMI and ESD Considerations

EMI and ESD need to be considered on a case by case basis relative to the product enclosure, deployed environment, and regulatory statutes. This application note does not give specific recommendations regarding EMI.

The CY7C656XX requires an external 24-MHz crystal. The component includes circuitry to step up that frequency to support the 480-MHz bit rate of high-speed USB signaling. Solid ground planes and short connections can help keep emissions low. Common mode chokes on the USB data pair will reduce emissions at the expense of signal quality. Other forms of EMI filtering such as ferrite beads in-line with USB data lines and adding capacitance to the data lines are strongly discouraged due to significant corruption of signal quality.

The TetraHub Reference Designs give examples of ESD consideration in the coupling between signal and

safety/shield ground. The two grounds are coupled together with the parallel connection of a 4.7-nF, 250 VAC capacitor and a 10M-ohm resistor. Review the CY7C656XX data sheet regarding ESD susceptibility (the maximum static discharge voltage) for the component pins.

When USB type A and type B connectors are used, they must be USB 2.0 compliant. These are shielded connectors appropriate to both EMI and ESD concerns. The connectors include separate connections for safety/shield ground and signal ground. These should be connected as stated in the previous paragraph.

PCB Design Recommendation

Printed circuit board (PCB) design for high-speed signaling requires careful attention to component placement, signal routing, layer stackup, and selection of board material. These characteristics impact electrical signal quality of the USB data pairs and the efficient dissipation of heat from the TetraHub component.

The Cypress Semiconductor application note titled *High-Speed USB PCB Layout Recommendations* treats the PCB design concerns applicable to high-speed USB circuits. There are numerous textbooks that treat the subject of high-speed design in general. One such book is listed in the References section.

Some areas of special note concerning design with high-speed hubs are addressed in this section.

Maintain PCB Trace Impedance

Designing the PCB traces for particular characteristic impedance is very important to signal quality. The USB specification requires controlled impedance among all elements in the USB data path. The differential impedance of each USB data pair must be 90 ohms with a 10% tolerance to match the differential output impedance of high-speed capable drivers.

A common way to implement a differential pair is to use an edge-coupled, surface microstrip line. The pair is on the board surface layer and is directly over a ground plane layer. This is the scenario used in the design of the CY4602. The following 5 parameters set the value for the differential impedance.

Table 2. Parameters For Setting Impedance

Term	Description
h	Height of signal traces above ground plane
εr	Material dielectric constant
t	Trace thickness
w	Trace width
s	Spacing between each trace of a differential pair, inside edge-to-edge

Parameters h, t, w, and s may be any unit but must be consistent. For example, the CY4602 design referenced in this application note shows these units in mil, (an English unit, 1/1000th of an inch). εr is a parameter with no units; it is dimensionless.

For an edge-coupled, surface microstrip, these 5 parameters (h, e, t, w, and s) set the value for the differential impedance (Zdiff). The differential pair impedance, (Zdiff), is given in terms of the impedance of each line of the pair, (Zo). The equations approximating impedance are:

$$Zdiff = 2 \cdot Z_0 \cdot \left(1 - 0.48 \cdot e^{-0.96 \cdot \frac{s}{h}}\right) ohms$$

Equation 1

$$Z_0 = \left(\frac{87}{\sqrt{\varepsilon_r + 1.41}}\right) \cdot \ln\left(\frac{5.98 \cdot h}{0.8 \cdot w + t}\right) ohms$$

Equation 2

The above equations are a good estimate when the following conditions are true:

$$\left(\frac{w}{h}\right) \leq 2.0$$

Equation 3

$$0.20 \leq \left(\frac{s}{h}\right) \leq 3.0$$

Equation 4

Books and calculators for impedance estimation for this and other topologies are available. One book and one spreadsheet for free download are cited in the References section.

Taken from the CY4602 TetraHub Reference Design drawings, Table 3 shows the dimensions impacting impedance for the USB data traces. The dimensions must satisfy the required characteristic impedance but must also result in a practical physical design. For instance, different fabrication processes may have limited choices for material dielectric constant and material thickness between the signal layer and the ground layer. These two parameters impacted the trace dimensions for this design. The PCB manufacturer's material for the PCB was taken from their standard supply. The vendor provided the tolerance values shown in Table 3. The values are all finished dimensions.

Table 3. Tolerance Values

Parameter	Tolerances	Min.	Nominal	Max.
Material thickness (mils)	±0.2	4.3	4.5	4.7
Material dielectric	±0.2	3.8	4.0	4.2
Trace thickness, 1 oz. (mils)	±0.1	1.1	1.2	1.3
Width (mils)	±0.5	6.5	7.0	7.5
Spacing (mils)	±1.0	6.0	7.0	8.0

Using the dimensions from the table, the Zdiff for the USB data pairs of the CY4602 TetraHub Reference Design is 90 ohms +10%, –10%.

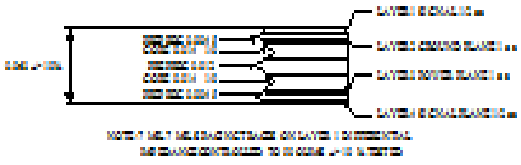
The designer should take advantage of any help available from the PCB manufacturer. The key dimensions and tolerances should be available from the manufacturer. Some manufacturers will perform the impedance calculations for the designer. Some will provide a service to measure the impedance after the PCB is fabricated.

PCB Layer StackUp

For a USB 2.0 high-speed design, use at least a four-layer PCB for best signal characteristics. With the primary components placed on the top side layer, the next layer must be a solid signal ground plane. A third voltage plane and fourth bottom side layer are typically the other two layers. The CY7C656XX component and its crystal must be placed on layer one, the top side. If you attempt a two-layer board you will need to reduce the thickness of the PCD along with increasing separation of traces and increased trace widths to maintain the impedance match of the data lines.

Figure 4 illustrates the recommended PCB stackup. This is the stackup used for the CY4602 TetraHub Reference Design.

Figure 4. Recommended PCB Stackup



The dielectric material thickness, ‘Prepreg’, between layers 1 and 2 and the thickness between layers 3 and 4 are shown. This dimension is a key element in the design to set the proper characteristic impedance for the USB data traces. This is the ‘h’ term mentioned in the prior section on PCB impedance design. Note that between layers 2 and 3 is the PCB's core material; this is not critical to characteristic impedance, but is used to determine the overall board thickness.

When designing with a two-layer board, control of the trace impedance becomes more difficult. To maintain the same impedance on a two-layer board, the board must become thinner and trace spacing and width will increase. Typically, since the thickness of the dielectric is the board thickness, the board must become thinner in order to hold the trace width down. Using half the thickness of the four-layer board will still result in traces that are 60 mil wide. A typical set of dimensions are listed below:

Table 4. Tolerance Values for Two-Layer Board

Parameter	Tolerances	Min.	Nominal	Max.
Material Thickness (mils)	±1.0	30.0	31	32
Material Dielectric	±0.2	3.8	4.0	4.2
Trace Thickness, 1 oz. (mils)	±0.1	2.3	2.4	2.5
Width (mils)	±0.5	59.5	60	60.5
Spacing (mils)	±1.0	59	60	61

Split Planes and Signal Routing

The shield/safety ground will be on one of the four layers of the PCB. However, when viewed across all layers of the PCB, the section with the shield/safety ground plane must not overlap other planes or signals. If the shield/safety ground is on the edge of the board with the USB connectors (as is the case with the CY4602 Reference Design), then there must be no other metal in other PCB layers directly above or below that area. Figure 5 illustrates a section of the ground layer of the CY4602's PCB. The shield/safety ground plane is on the same layer as the signal ground plane.

Figure 5. Section of CY4602's PCB Ground Plane

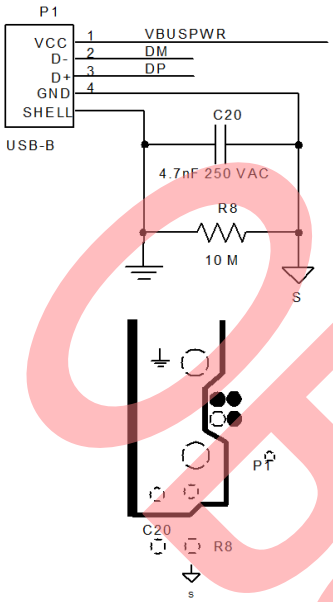


Figure 5 shows the schematic associated with the coupling across the CY4602 split plane using C21 and R13 components. The lower half of the diagram shows the associated section of PCB layer two. The width of the gap between the shield/safety ground and the signal ground must be not less than 25 mils in order to minimize the electrical edge coupling.

It is not necessary to have a large shield/safety ground plane like that shown for the CY4602. A 100-mil-wide trace for interconnect is sufficient.

Notice that the USB connector pins 1, 2, 3, and 4 are in the area of the signal ground, not the shield/safety ground. The USB signals from the connector route over the signal ground plane, never over the shield/safety ground. Signals must not route over the shield/safety ground plane. Other power or signal ground planes must not overlap the shield/safety ground plane.

All USB data signals must be routed exclusively on layer one, the top side. They must not route underneath any component except for their associated USB connector. Line length must be minimized. To minimize coupling between other USB data pairs and other non-USB signals, no USB data pair may be closer than 35 mils to another signal. Similarly, if a ground fill is to be used on the top side of the board, then to avoid significant impact to signal impedance, no USB data pair may be within 35 mil of the surface ground plane. These guidelines also apply to the crystal used for all the CY7C656XX components.

USB data lines must maintain proper differential pairing. This is not possible at either end of the line (CY7C656XX and associated USB connector), but as soon as physically possible the signal pairs must adhere to the proper trace design for the required 90-ohm differential impedance.

Thermal Design Considerations

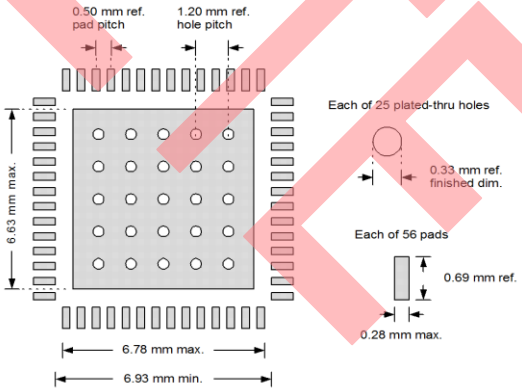
The QFN (Quad Flatpack No leads) is a package with a small footprint and low profile. It has excellent thermal properties: a very low Θ_{ja} of approximately 25 °C per watt. These thermal properties are ideal for high-performance Hubs.

The appropriate thermal design for use with the CY7C656XX is to dissipate heat from the QFN package by conduction, not airflow. Heat is conducted away from the package through its bond to the PCB. From there it is dissipated into the signal ground plane. Special attention to the heat transfer area below the package is required.

On the bottom of the package is a metal pad referred to as the exposed die attach paddle (or simply exposed paddle). The exposed paddle is the means by which most of the CY7C656XX thermal energy is dissipated away from the package. The exposed paddle is a square metal area approximately 6 mm on a side.

The design of the land area for the exposed paddle is critical to proper thermal transfer. The CY7C65620/30 can operate without the thermal pad but the results will cause the Θ_{ja} to increase to about 50 °C per watt. This is within the operating limits of the chip, but you will notice the heat difference on the chip. Maintaining the thermal pad and its connection will result in a much cooler die temperature. This thermal pad is a copper fill, which is to be designed into the PCB and under the QFN in order to assist thermal transfer. The CY7C65640A must have this thermal connection. Figure 6 is the diagram of the PCB land area for the CY7C656XX.

Figure 6. Diagram of the PCB Land Area



The heat is transferred to the solid signal ground plane of the board. The connection is made using a 5 x 5 array of 25 plated through holes in the PCB; each must have a finished diameter ranging from 12 mils to 13 mils. Since the CY4602 uses a 13 mil hole, that value will be used from here onward. Solder mask is placed over the top of each plated through hole to resist solder flow into the hole. The mask also is used to create voids in the flowed solder for outgassing during the solder reflow process.

Research done by Amkor, a package manufacturer, has determined that an array of more than 16 and less than 36 plated through holes should be used for the PCB land for the exposed paddle. Figure 7 shows thermal efficiency improving with an increase in number of plated through holes; a lower Qja is better. The figure is for the Amkor 7-mm 48-lead package. While the thermal values do not match the 8-mm 56-lead package used for the TetraHub, the values scale. For the CY7C65640A the number of vias must be at least 25.

Figure 7. Thermal Efficiency

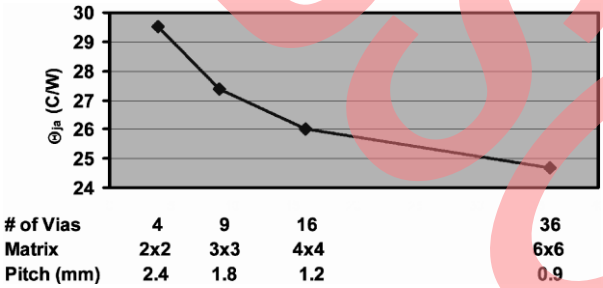
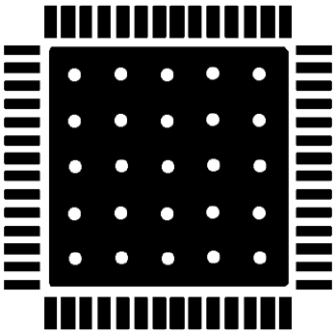


Figure 8 shows the solder mask region at the package. Each of the 25 plated through holes is in the center of each circle of solder mask. Black area indicates absence of solder mask.

Figure 8. Solder Mask



The signal ground plane provides the major area for thermal dissipation. The CY4602 uses the large internal layer of the PCB devoted to signal ground. This is a fairly large board intended for demonstration and evaluation of the CY7C65640A component.

For a fielded product, some developers may need a much smaller board size than the CY4602. To maximize area devoted to thermal dissipation, the designer must use the bottom layer of the PCB. This is in addition to the internal solid ground plane, which must be kept to maintain proper signal impedance. This metal fill must be connected to the signal ground plane at each of the 25 plated through holes under the QFN mounting. Additional 13-mil plated through holes may be placed throughout the board to connect to the internal signal ground plane as desired. Most holes must be placed as close to the QFN package as practical to improve thermal transfer.

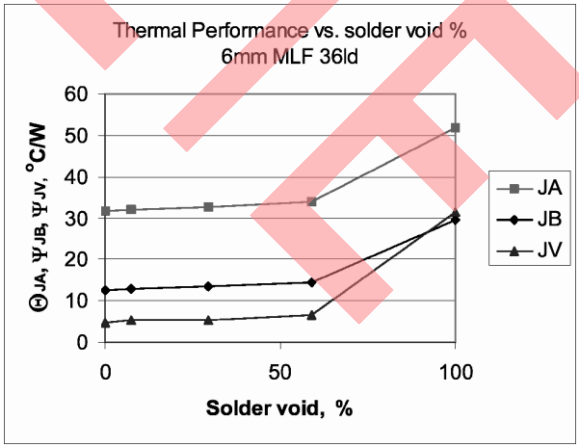
The enclosure for the circuit board assembly affects thermal performance. This application note does not give a specific example of an enclosure design. However, following the guidelines for PCB design described in this application note will assure the most efficient method to conduct heat away from the QFN package without the use of heat sinks. A large, solid ground plane with no large gaps close to the QFN mounting area will efficiently conduct heat through the PCB.

For further details on this package and methods and processes associated with its assembly to a printed circuit board, refer to the manufacturer's application note for the package. It is identified in the References section of this document.

TetraHub Assembly Recommendations

The solder stencil over the exposed paddle needs to permit at least 50% solder application coverage. Figure 9 is a graph from Amkor research showing how solder void much less than 50% has little influence on thermal transfer. The package is a smaller one than the CY7C656XX 8-mm 56-lead package, but the values do scale.

Figure 9. Thermal Performance vs. Solder Void



The manufacturing processes and practices of the assembly operation govern the stencil pattern used. Generally, arrays of either round or square patterns are used. A circular stencil was used for one assembly run of CY4602 boards.

Figure 10. Stencil Area for CY7C65620/30

Figure 11. Stencil Area for CY7C65640A

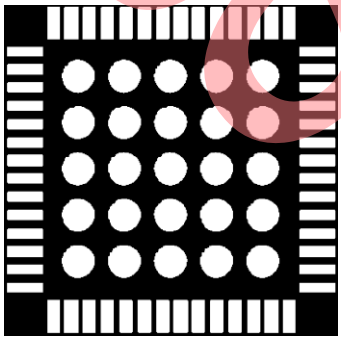


Figure 10 shows that the stencil area contains one hole. The hole is 3 mm square. The pad land on the PCB is 6 mm square. A large pattern of four squares could also be used. A solder stencil thickness of 0.125 mm is recommended for this package. With the CY7C65640A there needs to be an optimization for maximum heat dissipation. This is shown in Figure 11.

As there is no space under the package after soldering, use a 'No Clean,' type 3 solder paste. Nitrogen purge is recommended during solder reflow.

Summary

Following the recommendations of this application note should help the designer to produce a compliant and high-performance USB 2.0 hub design. Compliance can be confirmed with testing at the often-scheduled USB-IF Compliance Workshops. At this time, the only hubs that may participate at the workshops are the USB high-speed hubs, such as the TetraHub. To the extent possible, developers of USB products must test their designs for compliance prior to attending one of the workshops.

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**	1776985	NMMA	08/19/2008	New Application Note
*A	3150388	NMMA	01/21/2011	Changed Document Title from “CY7C656XX PCB DESIGN RECOMMENDATIONS” to “EZ-USB Hubs (CY7C656XX) PCB Design Recommendations”. Updated Asociated part family. Updated as per application note template.
*B	3355593	PRVE	08/29/2011	No change.
*C	4500817	PRJI	09/12/2014	No technical updates. Completing Sunset Review.
*D	5813071	AESATP12	07/12/2017	Updated logo and copyright.
*E	5962081	PRVE	11/09/2017	Obsolete document. Completing Sunset Review.

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