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Timing Uncertainty in High Performance Clock Distribution

Abstract

Several factors contribute to the timing uncertainty when using fanout buffers to distribute a clock to synchronize various devices within a system. For non-PLL clock fanout buffers, output skew, propagation delay, and edge rates play a critical role in determining system timing margin. This White Paper briefly discusses these parameters and their effect on system performance.

Introduction

The Cypress's high performance buffers (HPB) product family consists of high-frequency, low-additive phase jitter, low-skew, fast-edge fanout buffers operating at up to 1.5 GHz and providing up to ten differential outputs (LVPECL, LVDS, or CML). The family meets the high performance requirements of a wide variety of applications, including networking and communications, high-end servers, wireless base stations, and test equipment.

Table 1 lists the HPB product portfolio:

Table 1. HPB Product Portfolio

Part Number	Description	Package
CY2DP1510	2:10 LVPECL Buffer	32-pin TQFP
CY2DP1504	2:4 LVPECL Buffer	20-pin TSSOP
CY2DP1502	1:2 LVPECL Buffer	8-pin SOIC 8-pin TSSOP
CY2CP1504	2:4 LVCMOS to LVPECL Buffer	20-pin TSSOP
CY2DL1510	1:10 LVDS Buffer	32-pin TQFP
CY2DL15110	1:10 LVDS Buffer with Selectable input	32-pin TQFP
CY2DL1504	2:4 LVDS Buffer	20-pin TSSOP
CY2DM1502	1:2 CML Buffer	8-pin TSSOP
CY2DL1506	1:6 LVDS Buffer	24-pin TSSOP
CY2DL1508	1:8 LVDS Buffer	24-pin TSSOP

In networking, telecommunications and other high performance applications, fanout buffers are used to distribute a high performance clock signal to various points in the system. Typically the single most important purpose of this clock distribution tree is to synchronize the devices by delivering a clock edge to each system component at the same time. In practice, perfect synchronization is impossible, so system designers allow a timing budget such that all clock edges must occur within a defined window for the system to function properly. Thus, it is important when designing the clock distribution tree to minimize the variation of clock edge placement in time between the system components. This White Paper discusses the causes of clock edge uncertainty and ways to minimize their effects.

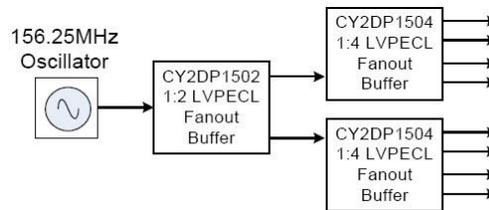
Critical Parameters in High-Speed Clock Distribution

As previously mentioned, the goal of building a clock tree in a synchronous system is to have all the clock edges occur at the same time. However, fanout buffers are the main component of clock distribution and they add uncertainty to the overall system timing in the form of clock skew and propagation delay. Additionally, the clock buffer edge rates can affect timing synchronization as well. In this note we discuss each of these parameters and how they may be mitigated to obtain the best possible system timing margin.

Figure 1 shows an example clock distribution tree. A high quality reference clock is provided by a 156.25 MHz oscillator. The signal is then distributed through a 1:2 fanout buffer, and the outputs of that buffer are used as inputs to two more 1:4 fanout buffers. The outputs of these buffers drive various devices within the system. Based on this topology, the components of timing uncertainty at the 1:4 fanout buffer loads include:

1. Output skew of the CY2DP1502
2. Difference in trace length between CY2DP1502 output pins and their respective loads (CY2DP1504 inputs)
3. Propagation delay of the CY2DP1504
4. a) Output skew of the CY2DP1504 for loads from the same CY2DP1504 buffer chip
b) Device skew of the CY2DP1504 for loads from different CY2DP1504 buffer chips
5. Difference in trace length between CY2DP1504 output pins and their respective loads

Figure 1. Example Clock Distribution Tree



Out of the five listed components, only #2 and #5 can be adjusted by the designer by changing the trace routing to match trace lengths. The remaining components are intrinsic properties of the fanout buffer devices; thus, the designer must carefully select fanout buffers based on the skew and propagation delay specifications as to the available timing margin in the system.

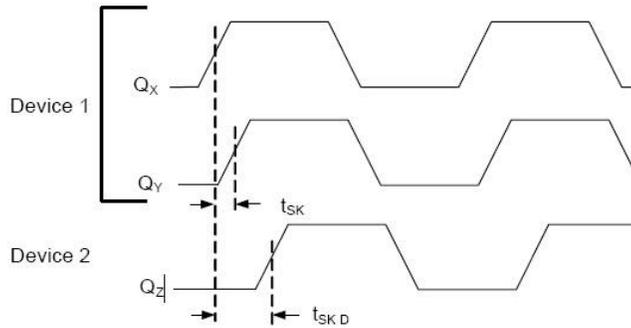
Clock Skew and Propagation Delay

Skew is the variation in the arrival time of two signals specified to occur at the same time. Skew consists of the output skew of the driving device and variation in the board delays caused by the layout variation of the board traces. The system performance is impacted when there is any variation in the arrival of the clock signal at its destination. Skew directly affects system margins by altering the arrival of a clock edge. Because elements in a synchronized system require clock signals to arrive at the same time, clock skew reduces the cycle time within which information can be passed from one device to the next.

Output skew (t_{sk}) is referred to as pin-to-pin skew. Output skew is the difference between delays of any two outputs on the same device at identical transitions. The absolute maximum difference between the rising edges of the outputs is specified as output skew. Figure 2 shows an example of output skew.

Device skew (t_{skD}) is known as part-to-part skew and package skew. Device skew is similar to output skew except that it applies to multiple identical devices. Device skew is defined as the magnitude of the difference in propagation delays between any specified outputs of two separate devices operating at identical conditions. The devices must have the same input signal, supply voltage, ambient temperature, package, load, environment, and so on. Figure 2 shows an example of device skew.

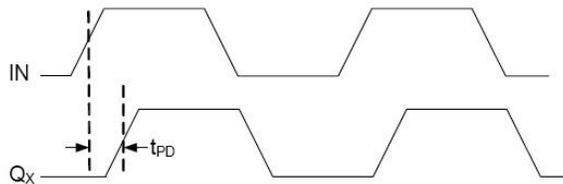
Figure 2. Output (Pin-to-Pin) and Device (Package) Skew



To minimize skew in the clock tree, the designer must select fanout buffers with very low output-to-output and device-to-device skew. Cypress’s HPB family of devices offer extremely low-output skew (20 ps max for 1:2 fanout buffers; 30 ps max for 1:4 fanout buffers, and 40 ps max for 1:10 fanout buffers) and low-device skew (150 ps max). The minimal skew contributed by these devices reduces the timing uncertainty of the clock tree and improves the overall system timing margin.

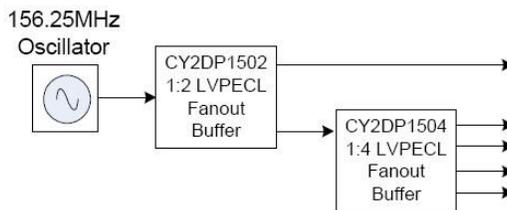
Propagation delay (t_{PD}) is the time between specified reference points on the input and output voltage waveforms with the output changing from one defined level (low) to the other (high). Propagation delay is shown in Figure 3.

Figure 3. Propagation Delay of a Clock Buffer



Since device propagation delay is accounted for in device skew, it does not play a significant role in clock trees with a topology similar to the one presented in Figure 1 on page 2. However, if a clock tree like the one shown in Figure 4 were to be implemented, propagation delay may become a concern. The t_{PD} of the CY2DP1504 may cause significant skew between the load of the CY2DP1502 and loads clocked by the CY2DP1504. However, this delay could be mitigated by extending the trace from the CY2DP1502 pin to its load by a length sufficient to counteract the added propagation delay of the CY2DP1504.

Figure 4. Alternative Clock Tree Topology with Propagation Delay Issue



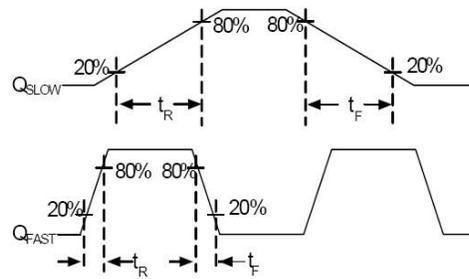
To obtain the best possible timing margin, select devices with low-propagation delay, although it is not quite as crucial as output and device skew and can be partially mitigated with careful clock tree planning.

Clock Edge Rates

Another important parameter in high performance clock distribution is the clock signal rise / fall time, called the edge rate. Figure 5 shows an example of how the edge rates of clock signals are commonly defined. Edge rates are specified in units of V/ns, while rise and fall times t_R and t_F are specified in units ns or ps. It is common to measure rise times from 20% to 80% of the peak-peak signal swing (and vice versa for fall times). In most high-speed or high performance applications, faster edge rates offer some advantages over slower edge rates.

Note The frequencies of the clock waveforms in Figure 5 and Figure 6 are intended to be the same; however, to show the concepts, the edge rates were exaggerated and thus the periods no longer match.

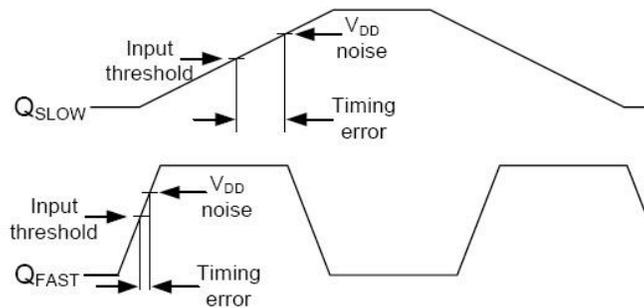
Figure 5. Slow Versus Fast Clock Edge Rates



First, clock signals with fast edges are less affected by different input trigger thresholds across devices. Because the clock input trigger voltage may vary slightly across devices in a system, a slow clock edge rate may widen the time difference between clock arrival at the different devices, increasing timing uncertainty.

Second, a faster edge rate makes the clock signal less susceptible to supply noise, cross talk, and jitter, allowing the designer to avoid potential timing margin issues. Figure 6 shows this advantage.

Figure 6. Edge Rates and Supply Noise Susceptibility



HPB devices offer fast edge rates (250 ps max rise or fall time for two output devices; 300 ps max rise or fall time for four or ten output devices), helping to avoid many possible timing margin issues in high-speed systems.

Summary

For high performance clock distribution applications, designers need to minimize clock skew, propagation delay, and clock rise or fall times to get the best timing margin possible for their systems. The HPB family of clock fanout buffers offers market-leading performance in all of these parameters, making these devices an ideal solution in networking and other high performance systems. For more information on our HPB product family, visit www.cypress.com.

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