AN47372

PrISM™ Technology for LED Dimming

Associated Project: No
Associated Part Family: CY8CLED0xD/G0x
Software Version: PSoC® Designer™ 5.1
Related Application Notes: AN51012

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AN47372 presents an overview of precision illumination signal modulation (PrISM™) technology for LED dimming applications. It also discusses the challenges faced in implementing high resolution PrISM and recommends solutions to address these issues.

Introduction

LED dimming or modulation of LED intensity is typically implemented using modulation schemes that use average duty cycle proportional to the desired dimming level in a fixed time period. These schemes are popularly known as pulse density modulation (PDM). Pulse-width modulator (PWM), which modulates width of pulses according to desired dimming levels, is the simplest example of PDM.

For LED dimming, the order in which individual pulses occur within a fixed time period is not important. However, the total high time or signal energy in the fixed time frame must be as configured. Cypress' PrISM serves as an alternative to traditional modulation schemes used for LED brightness control. PrISM technology is implemented using high resolution stochastic signal density modulation (SSDM) modules. In this application note, PrISM and SSDM are used interchangeably.

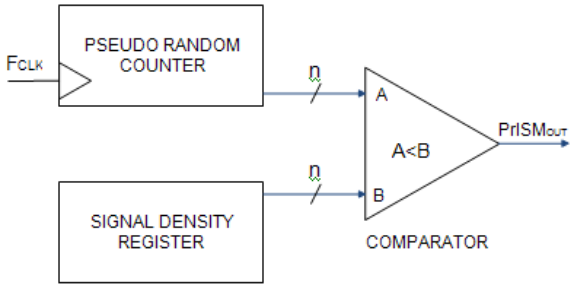
Although PWM has some excellent features, it suffers from significant harmonic generation at a relatively low frequency. Sometimes it may require intense filtering to remove high frequency components. Due to high electromagnetic interference (EMI) generation from PWM waves, SSDM is used to implement PrISM. The idea is to spread the energy at different frequencies so that it is easy to filter the higher harmonics, if required.

PrISM based dimming modulation is available as a configurable hardware block in the PowerPSoC family of devices. These devices can be used to design highly integrated LED driver circuits with power supply and LED dimming.

PrISM Technology

PrISM uses stochastic signal density modulation to generate the average signal density equivalent to dimming value. Figure 1 shows the basic components of a typical PrISM system.

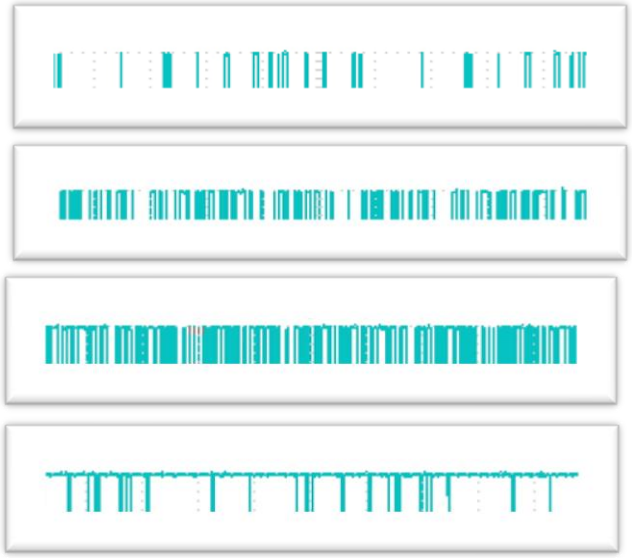
Figure 1. PrISM Block Diagram



The block diagram is divided into three major modules.

- Pseudo Random Counter: The top left block is a pseudo random counter, which generates n-bit pseudo random code at every tick of FCLK. It produces all codes ranging from 0 to 2^n–1. Generated codes are almost random. The counter repeats the codes every 2^{n+1} time.
- Signal Density Register: This is the left bottom block, which is a simple n-bit register. After reset, it is loaded with the desired signal density value and holds the same value until the user writes a new signal density value.
- Comparator: The block on the right is an asynchronous comparator, which continuously compares the content of the random counter with the value of signal density register. It makes the output HIGH when the signal density value is greater than the value of pseudo random counter. Pseudo random sequences for various dimming levels are shown in Figure 2.

Figure 2. Pseudo Random Sequences for Signal Density Values: 10%, 33%, 50%, 95%



Average Output Frequency

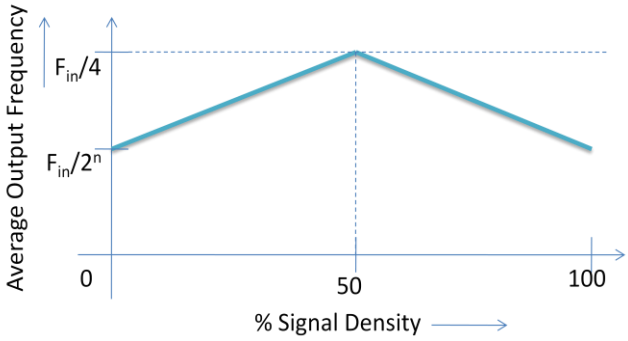
It is important to know the frequency content of the PrISM sequence. Unlike PWM, PrISM's output frequency is not fixed; it is variable and is a function of signal density.

SD% = (Signal Density Value / Period) * 100 → Equation 1

F_{OUT} = ½ SD. F_{IN} for (SD < = 0.5)

F_{OUT} = ½ (1- SD). F_{IN} for (SD > 0.5) → Equation 2

Figure 3. Average Output Frequency of PrISM



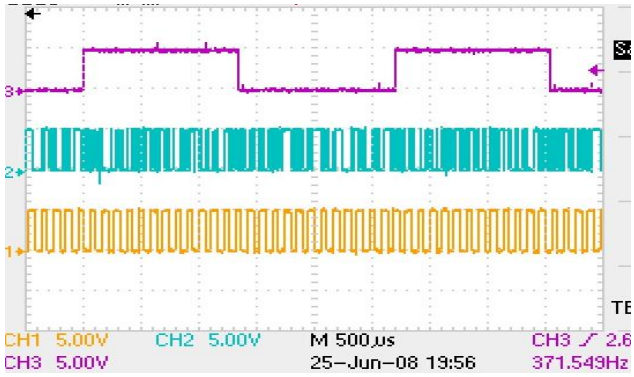
Maximum output frequency components present for any signal density in PrISM sequence are $F_{IN}/2$ and minimum are $F_{IN}/2^n$.

The average output frequency for 50% signal density is average of $F_{IN}/2$ (maximum value) and $F_{IN}/2^n$ (minimum value). For high n, the value of $F_{IN}/2^n$ is low compared to $F_{IN}/2$ and average output frequency is nearly $F_{IN}/4$.

Spectral Plot and Frequency Components

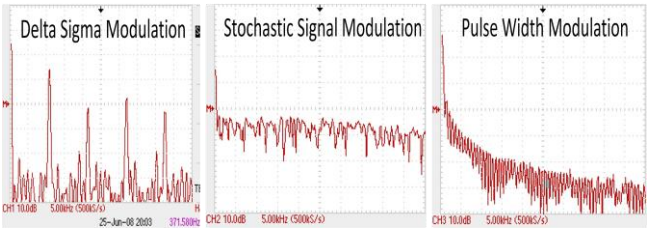
An important advantage of PrISM is less EMI compared to other modulation schemes such as PWM and delta sigma modulation (DSM). In PrISM, energy is spread at various frequencies. Therefore, there are no spikes at a particular frequency as they appear in PWM or DSM spectral plot.

Figure 4. PWM, PrISM, and DSM Wave at 50% Duty Cycle



For 50% signal density, on an average the improvement from PWM and DSM is about 35 dBm. Figure 5 shows the comparison of various modulation techniques for 50% duty cycle.

Figure 5. Spectrum Plots of DSM, PrISM, and PWM for 50% Signal Density



Design Considerations

LED dimming performance with PrISM technology depends on the minimum and maximum modulation frequency, among other factors. From Figure 2 and Figure 4 it is evident that switching is more in PrISM when compared to the equivalent PWM.

- **Minimum Output Frequency:** Minimum output frequency should be at least greater than 120 Hz to avoid the visible flickers. However, output frequency of 300 Hz is considered to be flicker free.
- **Maximum Output Frequency:** Maximum output frequency components (or thinnest pulses in case of spread spectrum) should be at least 10 times lower than switching frequency of regulator circuitry for efficient operation of regulation. Otherwise, these thin pulses are filtered out resulting in significant loss of signal density.

Boundary Conditions for F_{OUT}

- FOUT ~= 300 Hz
  To have flicker free LED dimming
- FOUT <= 1 KHz
  To minimize the inductor noise
- FOUT <= 0.1* FSW
  To make sure that regulator is not filtering out some of the high frequency components

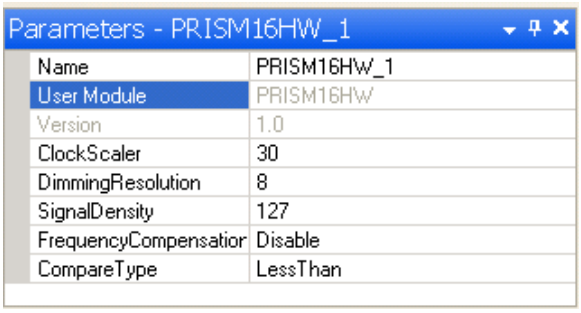
It may be impossible to completely eliminate the audible noise from inductors because the dimming frequency band overlaps with the human audible frequency band. However, noise can be minimized by choosing the right packaging for inductors.

PrISM Hardware Modulators in PowerPSoC

PowerPSoC provides integrated dimming modulators that interface with the constant current driver channels, and enable the modulation of high brightness LEDs. These modulators can be configured to implement PrISM (of up to 16-bit resolution) for LED dimming.

These PrISM modulators can be configured to directly control the hysteretic power channels of PowerPSoC to integrate LED dimming along with the LED power supply circuit. The modulator output can also be routed to an external pin. Figure 6 shows the parameters list of a 16-bit PrISM user module in PowerPSoC. See AN51012 POWERPSOC (R) FIRMWARE DESIGN GUIDELINES for more information on how to use PrISM user modules in PowerPSoC.

Figure 6. PrISM16HW User Module in PowerPSoC – Parameters List



Some of the most frequently used APIs of the hardware modulators are as follows. The function of these APIs is evident from their names.

- PRISM16HW_Start
- PRISM16HW_Stop
- PRISM16HW_SetSignalDensity
- PRISM16HW_SetDimmingResolution

The analysis of PrISM dimming for flicker and resolution is the same as with the implementation using SSDM user modules described in the following section.

SSDM User Modules in PowerPSoC

This section explains the implementation of PrISM using the SSDM user modules in PowerPSoC. This implementation uses the standard digital blocks in the PSoC core of PowerPSoC.

PSoC Designer™ incorporates SSDM modules and provides APIs to control them as part of the user module library. They are available in various resolutions such as 8-bit, 16-bit, 24-bit, and 32-bit. 8-bit SSDM module is used to generate the dimming resolution of 2 to 8 bits; 16-bit module generates anywhere from 2 to 16 bits. Either a PWM module or the clock resources available in PowerPSoC® (VC1, VC2, or VC3) can be used to provide the clocks to PrISM modules.

Table 1. User Module Parameters

Parameters	Values
Clock	VC3
SSDMOut	Row_x_Output_y
CompareType	Less Than Or Equal
DimmingResolution	8 or 16
SignalDensity	0
ClockSync	Sync to SysClock

Row_x_Output_y are the interconnect nets used to route the output of SSDM modules to external pins. Both x and y can have values from 0 to 3 in this implementation.

Table 2. Global Resources Setting for Sample Project

Resources	Values
VC3 Source	SysClk/1
VC3 Divider	4

VC3 gets the clock from SysClk and the divider is 4. If SysClk is set to 24 MHz, the SSDM modules tick at the rate of 6 MHz.

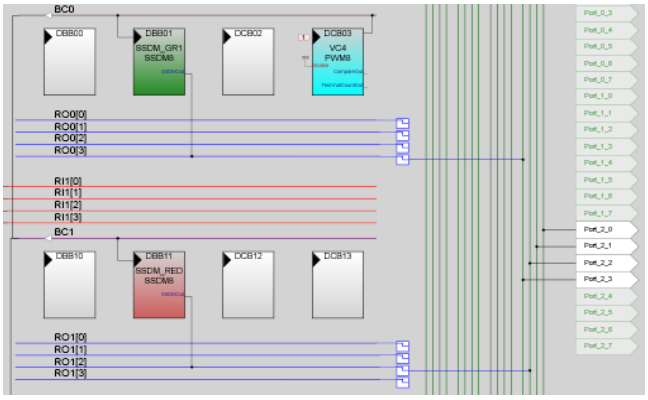
Some of the most frequently used APIs are as follows. The function of these APIs is evident from their names.

- SSDM_Start
- SSDM_Stop
- SSDM_WriteSignalDensity
- SSDM_WriteResolution

8-Bit PrISM

Figure 7 depicts implementation of 8-bit PrISM hardware. The two SSDM modules, clocking PWM, inter connection nets, and output ports are visible. In the current implementation, SSDM modules are clocked from a single PWM module. PWM based clock is generated appropriately by setting the duty cycle and time period of PWM module. Using an n-bit PWM, output clock ranging from $F_{IN}/2$ to $F_{IN}/2^n$ is generated. In 8-bit SSDM, codes generated by pseudo random counter for one signal density value ranges from 0 to 255.

Figure 7. 8-Bit PrISM Hardware Implementation



The main concern in LED dimming is that output frequency of SSDM should be at least 300 Hz to avoid flickers.

$F_{IN} = F_{OUT\ (MIN)} * 2^n = 300 * 256 \sim= 77$ KHz

F_{IN} of 77 KHz can be generated easily within the PSoC using VC clocks.

For F_{IN} = 77 KHz from Figure 3

$F_{OUT\ (MAX)} = F_{IN} / 2 = 77$ KHz / 2 = 38.5 KHz

F_{OUT} is below the typical switching frequency of regulator circuitry, which is 1 MHz. This ensures that the regulator is not filtering the thin pulses.

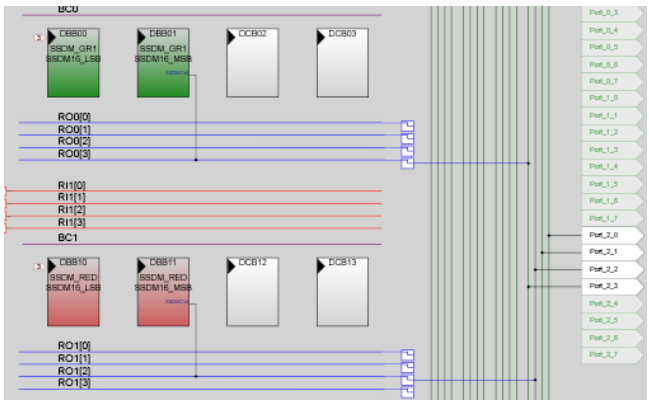
Although anything above the $F_{OUT\ (MIN)}$ of 300 Hz is acceptable, it is beneficial to bring the $F_{OUT\ (MIN)}$ closer to 300 Hz. This is because it brings the $F_{OUT\ (MAX)}$ well below the maximum limit, which is one tenth of the switching frequency of regulator circuitry.

16-Bit PrISM (Multi-Byte PrISM)

PrISM of higher than 8-bit resolution is called multi-byte PrISM. Each SSDM module consumes one digital PSoC block per 8 bits of resolution. So multi-byte PrISM consumes two digital blocks.

Codes generated by 16-bit pseudo random counter range from 0 to 65535. Figure 8 shows the implementation of multi-byte PrISM.

Figure 8. Multi-Byte PrISM Hardware Implementation



Analysis of PrISM Dimming

1. Assume the input frequency (F_{IN}) of multi-byte PrISM to be 1 MHz

   $F_{OUT\ (MIN)} = F_{IN} / 2^n$ = 1 MHz / 65536 ~= 15 Hz

   This output frequency is too low for LED dimming and results in visible flickers.

   To avoid the visible flickers, increase the $F_{OUT\ (MIN)}$. This is achieved by increasing the input frequency F_{IN}.

2. Increase the input frequency

   New input clock frequency to PrISM block is F_{IN} = 8 MHz

   $F_{OUT\ (MIN)} = F_{IN} / 2^n$ = 8 MHz / 65536 ~= 120 Hz

   This is good enough and hardly results in visible flickers but not better than 300 Hz. Also F_{IN} = 8 MHz is a high value for a system clock of 24 MHz.

   Increasing the input clock frequency also increases the maximum frequency components. For F_{IN} of 8 MHz:

   $F_{OUT\ (MAX)} = F_{IN} / 2$ = 8 MHz / 2 ~= 4 MHz

   This is very high when compared to for the regulator circuit's switching frequency of 2 MHz. The typical maximum is about 500 KHz which is four times less than the maximum possible switching frequency of 2 MHz.

   From this analysis, it is evident that flickers are avoided due to low frequency components by increasing the input frequency. However, this raises concerns because of high frequency components. For input frequency of 8 MHz, the high frequency components are as high as 4 MHz. This results in loss of average signal density for desired signal density value.

   To avoid filtering of high frequency components, the only solution is to reduce the resolution. This means, without increasing the switching frequency it is not possible to increase the dimming frequency to a very high value.

3. Reduce the resolution

   From the above analysis, increasing input frequency is not a good idea in most cases. The other option is to decrease the resolution up to the point where significant signal density is not lost.

   For $F_{OUT\ (MAX)}$ = 500 KHz (for switching frequency of 2 MHz)

   $F_{IN} = F_{OUT\ (MAX)} * 2$ = 1 MHz

   It is not a good idea to have dimming input clock frequency more than 1 MHz.

   Number of bits which does not lead to visible flickers

   $2^n = F_{IN} / F_{OUT}$ (MIN)

   To avoid the visible flickers, minimum output frequency is greater than 120 Hz.

   2^n = 1 MHz / 120 Hz ~= 8334 Hz

   After taking the log of both sides

   0.3010 * n = 3.92

   n = 13

From this analysis it is evident that up to 13-bit PrISM can be implemented without significant loss in average signal density for any signal density value. The number of bits is increased only when switching frequency of regulator circuitry increases.

Summary

This application note provides an overview of PrISM technology used for LED dimming applications. It explains the basic functionality of PrISM and its implementation details using SSDM and PrISM user modules in PowerPSoC. The application note also discusses the challenges faced in multi-byte PrISM and ways to overcome them.

Document History

Document Title: AN47372 - PrISM™ Technology for LED Dimming

Document Number: 001-47372

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2546747	RKSP	08/01/2008	New application note.
*A	2899888	UKK	03/29/2010	Added part number CY8CLED02.
*B	3169119	CJDV	02/10/2011	Updated software version. General update due to discontinued support for PSoC Express.
*C	3353160	SNVN	08/25/2011	Removed references to EZ-Color, vPrISM and sample projects. Added references to AN51012.
*D	4451444	SNVN	07/26/2014	Updated in new template. Completing Sunset Review.
*E	5701730	AESATMP9	04/19/2017	Updated logo and copyright.

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