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Spec No: 001-14705

Spec Title: EZ-USB(R) AT2LP(TM) Hardware Design Review Guide - AN14705

Replaced by: NONE

AN14705

EZ-USB® AT2LP™ Hardware Design Review Guide

Author: Rich Peng

Associated Project: No

Associated Part Family: CY7C68300C, CY7C68320C

Software Version: NA

Related Application Notes: None

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/AN14705.

AN14705 looks at each design component and guides designers as they review their AT2LP™ schematic during the design stage.

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Introduction

The information in this application note is organized to help customers review and resolve AT2LP hardware design issues, and reduce the time required to fix problems. This document covers most of the known hardware issues and their fixes. The schematic used in this document is the CY4615B reference schematic; it is divided into several functional examples that apply to each hardware component. Each part is described in detail. If used, this application note can help a designer filter most of their critical issues.

Power Component

Figure 1. AT2LP Power System Design

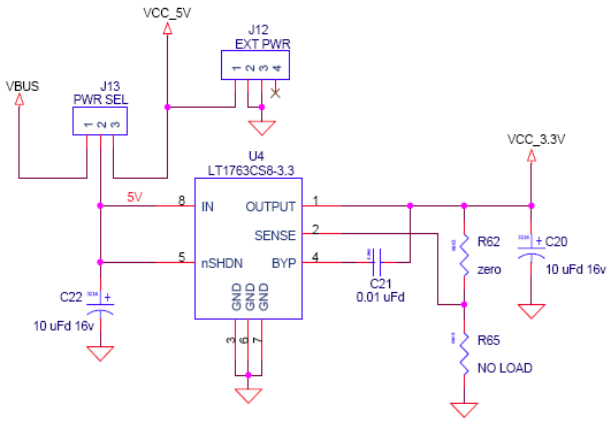


Figure 1 describes the AT2LP power system configuration.

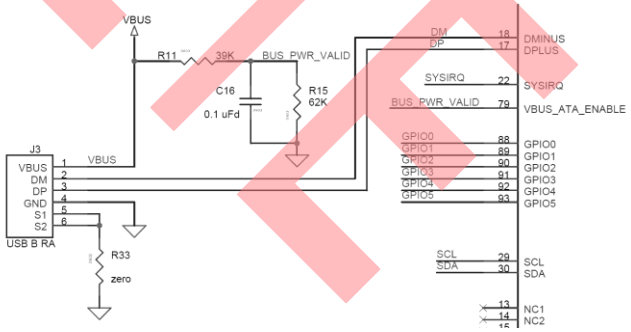
For the self-power design, use the external power to supply power to the IDE drive and AT2LP chip. The power can be separated into 12 V and 5 V. If there are slim type drives or small HDDs, then you must provide 5 V to those drives. Ensure the supplied power and VBUS are separated to avoid any power conflicts.

Use a regulator that can convert the 5 V to 3.3 V. Different regulators have different application circuits so be sure to follow the suggestions, provided with the regulator, in your design. Most importantly, ensure that the 5 V input can produce a 3.3 V output.

Install a test point on the 3.3 V line, to help troubleshoot if you need to debug your design.

USB Connector

Figure 2. AT2LP USB Connector Designs



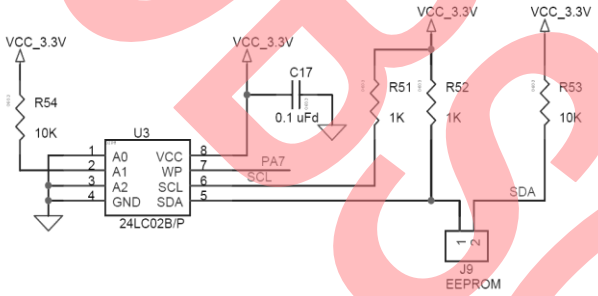
The VBUS pin is connected to the BUS_PWR_VALID through resistor R11. This signal indicates the AT2LP to start working. Add a 62 KΩ resistor to ground in order to bleed VBUS when it is disconnected (see Figure 2).

Connect the D+ / D- directly to the AT2LP chip, do not use resistors and capacitors. Because the AT2LP functions at high speed (480 MHz), impedance affects signal quality. To add a common choke for the EMS issue then its specifications must be evaluated carefully. The selections must pass both signal quality and EMS testing. The most important thing is to match the impedance requirement of the USB2.0 specification, which is 45 ohms single ended.

The only parts that may be connected to the D+ / D- bus of AT2LP USB connector are the H-S choke for EMI testing and H-S bead for ESD testing.

EEPROM Part

Figure 3. AT2LP EEPROM Design



Use I2C interface compatible EEPROM's such as 24LC02 part. 256 bytes are required to store the configuration data, V/PID, unique serial number, and strings.

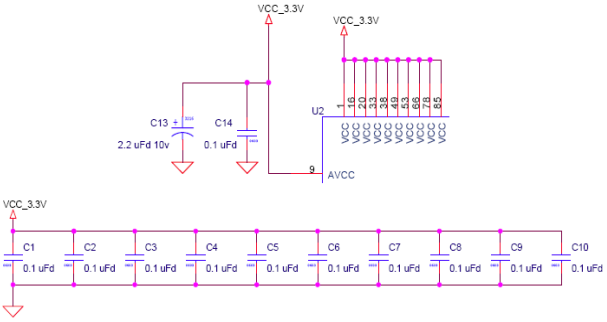
Address is '010' is used for the AT2LP to communicate with the small EEPROM.

Connect the write protect pin to the ATA_Reset# pin to avoid corrupting the EEPROM contents when the device powers on or off. When the device powers on, the WP pin is pulled high by ATA_Reset, ensuring that the EEPROM cannot be written. The AT2LP programming utility pulls this pin low, while the EEPROM is being programmed.

Connect the external pull up resistors to SCL and SDA to avoid initialization/enumeration problems.

VCC_3.3 V Circuit

Figure 4. AT2LP VCC 3.3 V Design

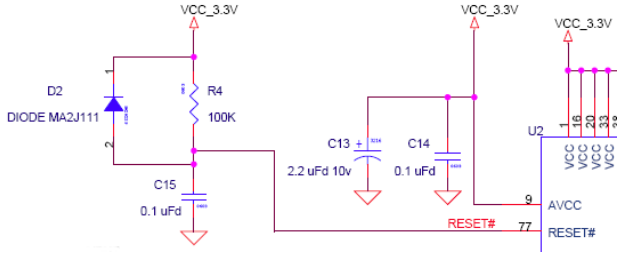


Add a 2.2 µF~4.7 µF electrolytic capacitor at the AVCC pin and a 0.1 µF capacitor to filter the analog power noise.

Add a bypass capacitor on each pin that has 3.3 V. Place the bypass capacitors as close to the chip as possible.

Reset Circuit

Figure 5. AT2LP Reset Circuit Design

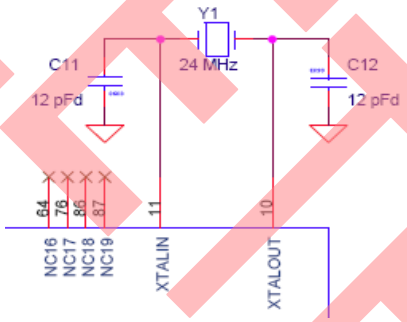


This chip has an active low RESET signal. Apply a low signal for 1.9 ms so that the chip senses the reset. To implement this, use an RC network with a 10 ms time constant.

For bus powered designs, do not use the RC reset circuit because of the potential for VBUS voltage droop, which may result in a startup time that exceeds the USB limit. Adding a diode helps to avoid potential voltage feedback.

Crystal Part

Figure 6. AT2LP Crystal Design



Make certain that you use the proper frequency. The AT2LP requires 24 MHz (±100 ppm, 12 pF load capacitor, 500 µW, parallel resonant, and fundamental mode).

The AT2LP can also use the 24 MHz square wave (3.3 V, 50/50 duty cycle). Apply it to XTALIN and leave XTALOUT disconnected.

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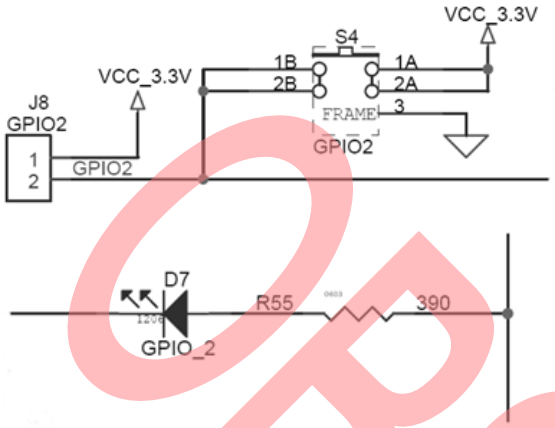
Understanding the GPIO Circuit

Figure 7. AT2LP GPIO Design

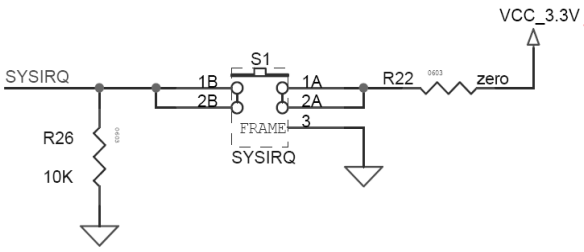


The maximum number of allowable CY7C68320C-100TQFP GPIOs is six; three GPIOs are for use with the CY7C68320C-56 QFN. The GPIOs may be configured as input or output pins using the EEPROM. If configured as outputs, set the default value to either High or Low.

Typically, the GPIO pins are used to make LEDs blink or implement special features using the software, such as the one touch backup feature.

SYSIRQ Pin

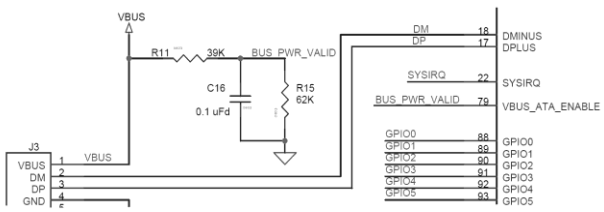
Figure 8. T2LP SYSIRQ Pin Designs



The SYSIRQ pin on CY7C68320C-100 TQFP provides a way for systems to request service from the host software by using the USB interrupt pipe on EP1. Refer to datasheet EZ-USB AT2LP™ USB 2.0 to ATA/ATAPI Bridge for more information.

VBUS_ATA_Enable Pin (ATA_EN Pin in AT2+ backward compatible mode)

Figure 9. AT2LP VBUS_ATA_Enable Pin Design



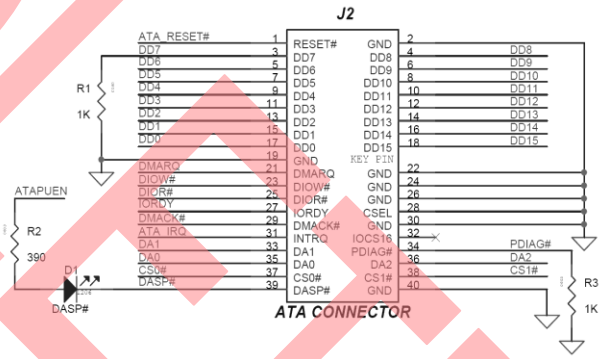
To use this pin's functionality, set the EEPROM address 0x08 bit 4.

If bit 4 of the configuration address 0x08 is '0', the ATA interface is still driven when the VBUS_ATA_Enable pin is '0'. If bit 4 of the configuration address 0x08 is '1', the ATA interface pins are placed in a Hi-Z state when VBUS_ATA_Enable is '0'.

Ensure the VBUS_ATA_Enable pin is connected.

ATA Connector

Figure 10. AT2LP ATA Connector Design



Ensure that DD7 has a pull-down resistor to GND to achieve the best compatibility with different IDE devices. The resistor is required for manufacturing mode.

A pull-down resistor is also required to meet ATA/ATAPI 6 specifications.

The DASP# indicates that data transfer is in progress (the drive is busy). Add an LED to use as an indicator to visually see the signal status.

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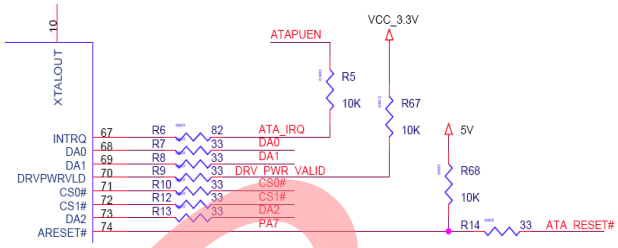
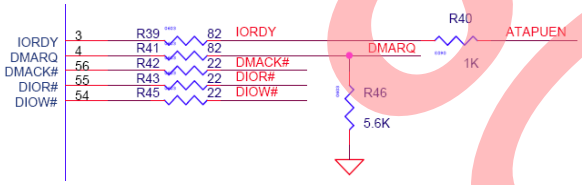
Figure 11. ATA Connector Control Signals (1) Design



Make certain that a pull up resistor is connected to the ATA_RESET pin when power is applied so that Reset executes properly. This pin can be connected to the EEPROM write protect pin to prevent the EEPROM contents from being corrupted during the power transient.

To avoid an impedance mismatch, verify that the remaining IDE device control pins have a 33 Ω serial resistor for each pin.

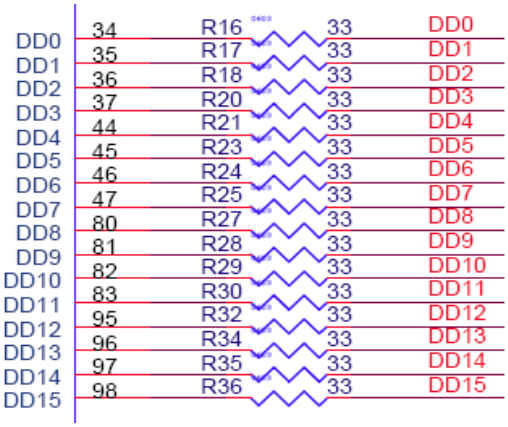
Figure 12. AT2LP ATA Connector Control Signals (2) Design



Ensure that ATA_IRQ, IORDY, and DMARQ# have an 82 Ω serial resistor. DMARQ# needs a pull down resistor connected to GND to meet ATA/ATAPI 6 specifications.

Ensure that DMACK#, DIOR#, and DIOW# have a 22 Ω serial resistor to meet the ATA/ATAPI 6 specifications.

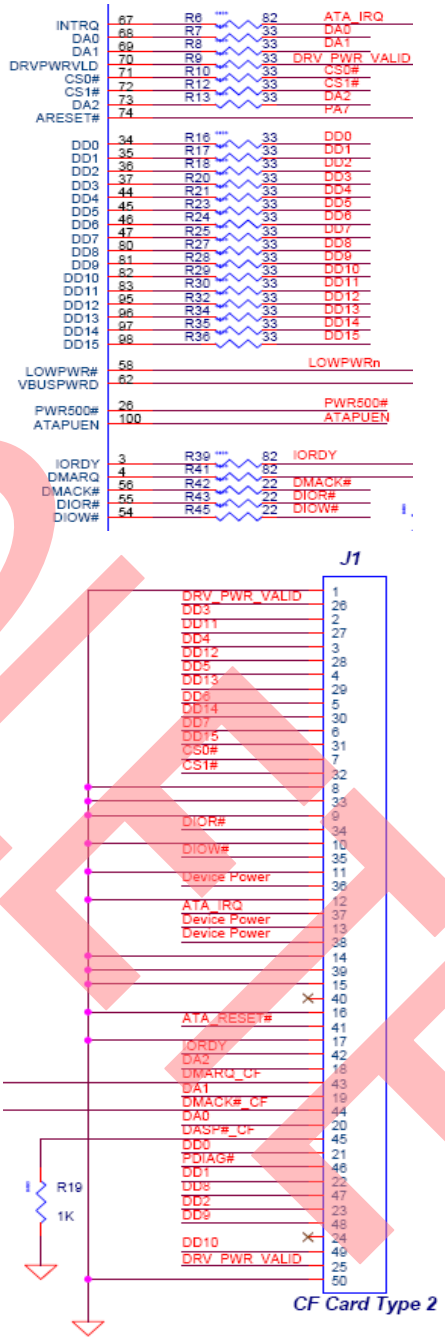
Figure 13. AT2LP ATA Connector Data Bus Design



On the data bus (DD0~DD15), to avoid PCB data transfer problems make certain that there are 33 Ω serial resistors on each pin to get an impedance match.

CF Card Type 2 Reader Design

Figure 14. AT2LP CF Card Reader Design



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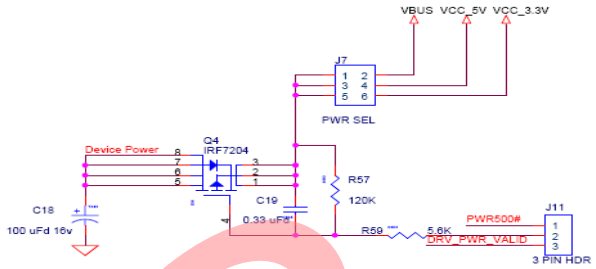

To design a bus power IDE device, start your design with the CY4615B Micro Drive design as a reference. Use the IDE mode to control the CF Card Type mass storage device. Load the *56_bus_MD.iic* for the Micro Drive design and the *56_bus_CF.iic* for the CF Card Reader design.

For maximum performance, use the DMARQ#_CF and DMACK#_CF tied to the DMARQ# and DMACK# directly. Load the *56_bus_CF_UDMA.iic* to get the UDMA support with the CF Card Reader design.

Be careful with the DRVPWRVLD pin. When this pin is enabled, using bit 0 of configuration address 0x08 (DRVPWRVLD Enable), the AT2LP informs the host that a removable device is present. Details of this issue are available under section DRVPWRVLD in EZ-USB AT2LP™ USB 2.0 to ATA/ATAPI Bridge datasheet.

The IIC files are included in CY4615B Reference Design kit software. They are located at CY4615B_r1_1\ManufacturingSoftware\Config_files. This directory includes different IIC files to match different mass storage applications that use the AT2LP.

Summary

This application note guides you in checking each design component. Following guidelines in this application note, you can eliminate most AT2LP hardware design issues. The EEPROM configuration affects the hardware design.

Here are some ways to effectively use the information in this application note.

- Use this application note with AT2LP in conjunction with the AT2LP datasheet.
- Check the availability of AT2LP chip parts to be used in the design in the Ordering Information table of the datasheet. The table is revised regularly with active parts in “production” status.
- Record the IDE control pin’s behavior when used with EEPROM configuration data. Use this information to achieve the correct behavior with your design.
- Every time you use the AT2LP design with your products. Before proceeding to design a custom board based on AT2LP use CY4615B board from cypress to test the mass storage device you want to connect. This allows you to make certain that there are no compatibility issues.
- Observe if there is any odd behavior while using the CY4615B. In case of no issues, proceed to design a custom board.
- In the event of a failure observed during test, submit a case to Cypress Support Forums. Provide the schematic, the mode used with the AT2LP chip (AT2LP or AT2+ compatible mode), and the name of the IIC file.

Additional Resources

- *CY4615B Reference Design Kit*
- ATA/ATAPI-6 Specification
- USB Mass storage Bulk-Only-Transport Specification
- USB specification version 2.0.

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*A	3126242	NMMA	01/07/2011	Added Additional Resources.
*B	3278459	NMMA	06/09/2011	Updated Summary (Added Ordering Information table check in the section).
*C	4418238	HBM	06/24/2014	Updated in new template. Completing Sunset Review.
*D	5836273	RAJV	07/28/2017	This spec is obsolete.

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