Features

- Industry-standard NXP® I²C bus interface
- Supports Slave, Master, Multi-Master and Multi-Master-Slave operation
- Only two pins (SDA and SCL) required to interface to I²C bus
- Standard data rates of 100/400/1000 kbps supported
- High-level APIs require minimal user programming

General Description

The I²C component supports I²C Slave, Master, and Multi-Master configurations. The I²C bus is an industry-standard, two-wire hardware interface developed by Philips. The master initiates all communication on the I²C bus and supplies the clock for all slave devices.

The I²C component supports standard clock speeds up to 1000 kbps. The I²C component is compatible with other third-party slave and master devices.

Note This version of the component datasheet covers both the fixed hardware I²C block and the UDB version.

When to Use an I²C Component

The I²C component is an ideal solution when networking multiple devices on a single board or small system. The system can be designed with a single master and multiple slaves, multiple masters, or a combination of masters and slaves.
Input/Output Connections

This section describes the various input and output connections for the I²C component. An asterisk (*) in the list of I/Os indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

sda – In/Out

Serial data (SDA) is the I²C data signal. It is a bidirectional data signal used to transmit or receive all bus data. The pin connected to sda should be configured as Open-Drain-Drives-Low.

scl – In/Out

Serial clock (SCL) is the master-generated I²C clock. Although the slave never generates the clock signal, it may hold the clock low, stalling the bus until it is ready to send data or ACK/NAK¹ the latest data or address. The pin connected to scl should be configured as Open-Drain-Drives-Low.

clock – Input *

The clock input is available when the Implementation parameter is set to UDB. The UDB version needs a clock to provide 16 times oversampling.

<table>
<thead>
<tr>
<th>Bus</th>
<th>Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 kbps</td>
<td>800 kHz</td>
</tr>
<tr>
<td>100 kbps</td>
<td>1.6 MHz</td>
</tr>
<tr>
<td>400 kbps</td>
<td>6.4 MHz</td>
</tr>
<tr>
<td>1000 kbps</td>
<td>16 MHz</td>
</tr>
</tbody>
</table>

reset – Input *

The reset input is available when the Implementation parameter is set to UDB. If the reset pin is held to logic high, the I²C block is held in reset, and communication over I²C stops. This is a hardware reset only. Software must be independently reset using the I2C_Stop() and I2C_Start() APIs. The reset input may be left floating with no external connection. If nothing is connected to the reset line, the component will assign it a constant logic 0.

¹ NAK is an abbreviation for negative acknowledgment or not acknowledged. I²C documents commonly use NACK while the rest of the networking world uses NAK. They mean the same thing.
Schematic Macro Information

By default, the PSoC Creator Component Catalog contains four Schematic Macro implementations for the I²C component. These macros contain already connected and configured pins and provide a clock source, as needed. The Schematic Macros use I²C Slave and Master components, configured for fixed-function and UDB hardware, as shown below.

Fixed-Function I²C Slave with Pins

Fixed-Function I²C Master Pins

UDB I²C Slave with Clock and Pins

UDB I²C Master with Clock and Pins
Component Parameters
Drag an \( \text{i}^2\text{C} \) component onto your design and double click it to open the Configure dialog.

The \( \text{i}^2\text{C} \) component provides the following parameters.

**Mode**
This option determines what modes are supported, Slave, Master, Multi-Master, or Multi-Master-Slave.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slave</td>
<td>Slave only operation (default).</td>
</tr>
<tr>
<td>Master</td>
<td>Master only operation.</td>
</tr>
<tr>
<td>Multi-Master</td>
<td>Supports more than one master on the bus.</td>
</tr>
<tr>
<td>Multi-Master-Slave</td>
<td>Simultaneous slave and multi-master operation.</td>
</tr>
</tbody>
</table>
**Data Rate**

This parameter is used to set the \(i^2C\) data rate value up to 1000 kbps; the actual speed may differ based on available clock speed and divider range. The standard data rates\(^2\) are 50, 100 (default), 400, and 1000 kbps. If Implementation is set to UDB and the UDB Clock Source parameter is set to External Clock, the Data Rate parameter is ignored; the 16x input clock determines the data rate.

**Slave Address**

This is the \(i^2C\) address that will be recognized by the slave. If slave operation is not selected, this parameter is ignored. A slave address between 0 and 127 (0x00 and 0x7F) may be selected; the default is 4. This address is the 7-bit right-justified slave address and does not include the R/W bit. The value may be entered as decimal or hexadecimal; for hexadecimal numbers type ‘0x’ before the address. If a 10-bit slave address is required, you must use software address decoding and provide decode support for the second byte of the 10-bit address in the ISR.

**Implementation**

This option determines how the \(i^2C\) hardware is implemented on the device.

<table>
<thead>
<tr>
<th>Implementation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed Function</td>
<td>Use the fixed-function block on the device (default).</td>
</tr>
<tr>
<td>UDB</td>
<td>Implement the (i^2C) in the UDB array.</td>
</tr>
</tbody>
</table>

**Address Decode**

This parameter allows you to choose between software and hardware address decoding. For most applications where the provided APIs are sufficient and only one slave address is required, hardware address decoding is preferred. In applications where you prefer to modify the source code to provide detection of multiple slave addresses, you must use software address detection. **Hardware** is the default. If hardware address decode is enabled, the block automatically NAKs addresses that are not its own without CPU intervention. It automatically interrupts the CPU on correct address reception, and holds the SCL line low until CPU intervention.

**Pins**

This parameter determines which type of pins to use for SDA and SCL signal connections. There are three possible values: **Any**, **I2C0**, and **I2C1**. The default is **Any**.

**Any** means general-purpose I/O (GPIO or SIO). If Enable wakeup from Sleep Mode is not required, **Any** should be used for SDA and SCL. If Enable wakeup from Sleep Mode is

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\(^2\) Fixed-Function implementation supports only standard data rates 50, 100 or 400 kbps for PSoC 3 ES2 and PSoC 5 devices. The UDB-based implementation should be used instead for different data rates up to 1000 kbps.
required, **I2C0** or **I2C1** must be used; using either **I2C0** or **I2C1** allows you to configure the device for wakeup on I²C address match.

The I²C component does not check the correct pin assignments.

<table>
<thead>
<tr>
<th>Value</th>
<th>Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>Any</td>
<td>Any GPIO or SIO pins through schematic routing</td>
</tr>
<tr>
<td>I2C0</td>
<td>SCL = SIO pin P12[4], SDA = SIO pin P12[5]</td>
</tr>
<tr>
<td>I2C1</td>
<td>SCL = SIO pin P12[0], SDA = SIO pin P12[1]</td>
</tr>
</tbody>
</table>

**Enable wakeup from Sleep Mode**

This option allows the system to be awakened from sleep when an address match occurs. This option is only valid if **Address Decode** is set to **Hardware** and the SDA and SCL signals are connected to SIO pins (**I2C0** or **I2C1**). The option is disabled by default. This option is not supported by the PSoC 3 ES2 and PSoC 5 devices.

You must enable the possibility for the I²C to wake up the device on slave address match while switching to the sleep mode. You can do this by calling the I2C_Sleep() API; also refer to the **Wakeup on Hardware Address Match** section and to the “Power Management APIs” section of the **System Reference Guide**.

**UDB Clock Source**

This parameter allows you to choose between an internally configured clock and an externally configured clock for data rate generation. When set to **Internal Clock**, the required clock frequency is calculated and configured by PSoC Creator based on the **Data Rate** parameter and taking into account 16 times oversampling. In **External Clock** mode the component does not control the data rate but displays the actual data rate based on the user-connected clock source. If this parameter is set to **Internal Clock** then the clock input is not visible on the symbol.

You can enter the desired tolerance values for the internal clock. Clock tolerances are specified as a percentage. The default range for Slave mode is **-5% to +50%**. The clock can be fast in this mode. For the remaining modes, the default range is **-25% to +5%**. Again the master can be slow. At the maximum data rate (1000 kbps), the clock should be equal or slower, but not higher than expected. This could cause unexpected behavior.

**Enable UDB Slave Fixed Placement**

This parameter allows you to choose a fixed component placement that improves the component performance over unconstrained placement. If this parameter is set, all of the component resources are fixed in the top right corner of the device. This parameter controls the assignment of pins connected to the component. The choice of pin assignment is not a determining factor for component performance. This option is only valid if **Mode** is set to **Slave** and **Implementation** is set to **UDB**. This option is disabled by default.
The fixed placement aspect of the component removes the variability that is accounted for with the "Maximum with All Routing" case (see DC and AC Electrical Characteristics (UDB Implementation) for details). It also allows the fixed placement to continue to operate the same as a non-fixed placed design would in a fairly empty design.

### Clock Selection

When the internal clock configuration is selected, PSoC Creator calculates the needed frequency and clock source and generates the resource for implementation. Otherwise, you must supply the clock component and calculate the required clock frequency. That frequency is 16x the desired data rate available. For example, a 1.6-MHz clock is required for 100-kHz data rate.

The fixed-function block uses BUS_CLK, which is calculated by the customizer divider to archive the 16/32 oversampling rate (50-kHz oversampling rate is 32, all other rates are 16).

**Note** Look at Errata Item 49. I^2^C Clocking to provide desired clock for the I^2^C fixed-function block on early silicon versions.

### Resources

The following configuration settings were used to generate the resource usage information:

1. **Address Decode** set to **Software**;
2. **Enable wakeup from Sleep Mode** deselected; **UDB Clock Source** set to **External Clock**.

The fixed I^2^C block is used for fixed-function implementation.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Resource Type</th>
<th>API Memory (Bytes)</th>
<th>Pins (per External I/O)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I^2^C Fixed Blocks</td>
<td>Flash</td>
<td>RAM</td>
</tr>
<tr>
<td>Slave</td>
<td>1</td>
<td>916</td>
<td>22</td>
</tr>
<tr>
<td>Master</td>
<td>1</td>
<td>1737</td>
<td>20</td>
</tr>
<tr>
<td>Multi-Master</td>
<td>1</td>
<td>1889</td>
<td>20</td>
</tr>
<tr>
<td>Multi-Master-Slave</td>
<td>1</td>
<td>2550</td>
<td>34</td>
</tr>
</tbody>
</table>
For UDB implementation, see the following table.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Resource Type</th>
<th>API Memory (Bytes)</th>
<th>Pins (per External I/O)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Datapaths</td>
<td>PLDs</td>
<td>Status Cells</td>
</tr>
<tr>
<td>Slave</td>
<td>1</td>
<td>12</td>
<td>1</td>
</tr>
<tr>
<td>Master</td>
<td>2</td>
<td>14</td>
<td>1</td>
</tr>
<tr>
<td>Multi-Master</td>
<td>2</td>
<td>18</td>
<td>1</td>
</tr>
<tr>
<td>Multi-Master-Slave</td>
<td>2</td>
<td>32</td>
<td>1</td>
</tr>
</tbody>
</table>

**Application Programming Interface**

Application Programming Interface (API) routines allow you to configure the component during runtime. The following table lists and describes the interface to each function. The subsequent sections cover each function in more detail.

By default, PSoC Creator assigns the instance name “I2C_1” to the first instance of a component in a given design. You can rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is “I2C.”

All API functions assume that data direction is from the perspective of the I²C master. A write event occurs when data is written from the master to the slave. A read event occurs when the master reads data from the slave.

**Generic Functions**

This section includes the functions that are generic to I²C slave or master operation.

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_Start()</td>
<td>Initializes and enables I²C component. The I²C interrupt is enabled, I²C traffic can be responded to.</td>
</tr>
<tr>
<td>I2C_Stop()</td>
<td>Stops responding to I²C traffic (disables I²C interrupt).</td>
</tr>
<tr>
<td>I2C_EnableInt()</td>
<td>Enables interrupt, which is required for most I²C operations.</td>
</tr>
<tr>
<td>I2C_DisableInt()</td>
<td>Disables interrupt. The I2C_Stop() API does this automatically.</td>
</tr>
<tr>
<td>I2C_Sleep()</td>
<td>Stops I²C operation and saves I²C nonretention configuration registers (disables interrupt). Prepares wake on address match operation If Wakeup from Sleep Mode is enabled (disables I²C interrupt).</td>
</tr>
<tr>
<td>I2C_Wakeup()</td>
<td>Restores I²C nonretention configuration registers and enables I²C operation (enables I²C interrupt).</td>
</tr>
</tbody>
</table>
### Function Description

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_Init()</td>
<td>Initializes I²C registers with initial values provided from customizer.</td>
</tr>
<tr>
<td>I2C_Enable()</td>
<td>Activates I²C hardware and begins component operation.</td>
</tr>
<tr>
<td>I2C_SaveConfig()</td>
<td>Saves I²C nonretention configuration registers (disables I²C interrupt).</td>
</tr>
<tr>
<td>I2C_RestoreConfig()</td>
<td>Restores I²C nonretention configuration registers saved by I2C_SaveConfig() or I2C_Sleep() (enables I²C interrupt).</td>
</tr>
</tbody>
</table>

### Global Variables

Knowledge of these variables is not required for normal operations.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_initVar</td>
<td>I2C_initVar indicates whether the I²C component has been initialized. The variable is initialized to 0 and set to 1 the first time I2C_Start() is called. This allows the component to restart without reinitialization after the first call to the I2C_Start() routine. If reinitialization of the component is required, then the I2C_Init() function can be called before the I2C_Start() or I2C_Enable() function.</td>
</tr>
<tr>
<td>I2C_state</td>
<td>Current state of I²C state machine.</td>
</tr>
<tr>
<td>I2C_mstrStatus</td>
<td>Current status of I²C master.</td>
</tr>
<tr>
<td>I2C_mstrControl</td>
<td>Controls master end of transaction with or without generating a stop.</td>
</tr>
<tr>
<td>I2C_mstrRdBufPtr</td>
<td>Pointer to master read buffer.</td>
</tr>
<tr>
<td>I2C_mstrRdBufSize</td>
<td>Size of master read buffer.</td>
</tr>
<tr>
<td>I2C_mstrRdBufIndex</td>
<td>Current index within master read buffer.</td>
</tr>
<tr>
<td>I2C_mstrWrBufPtr</td>
<td>Pointer to master write buffer.</td>
</tr>
<tr>
<td>I2C_mstrWrBufSize</td>
<td>Size of master write buffer.</td>
</tr>
<tr>
<td>I2C_mstrWrBufIndex</td>
<td>Current index within master write buffer.</td>
</tr>
<tr>
<td>I2C_slStatus</td>
<td>Current status of I²C slave.</td>
</tr>
<tr>
<td>I2C_slAddress</td>
<td>Software address of I²C slave.</td>
</tr>
<tr>
<td>I2C_slRdBufPtr</td>
<td>Pointer to slave read buffer.</td>
</tr>
<tr>
<td>I2C_slRdBufSize</td>
<td>Size of slave read buffer.</td>
</tr>
<tr>
<td>I2C_slRdBufIndex</td>
<td>Current index within slave read buffer.</td>
</tr>
<tr>
<td>I2C_slWrBufPtr</td>
<td>Pointer to slave write buffer.</td>
</tr>
<tr>
<td>I2C_slWrBufSize</td>
<td>Size of slave write buffer.</td>
</tr>
<tr>
<td>I2C_slWrBufIndex</td>
<td>Current index within slave write buffer.</td>
</tr>
</tbody>
</table>
Generic Functions

void I2C_Start(void)

Description: This is the preferred method to begin component operation. I2C_Start() calls the I2C_Init() function, and then calls the I2C_Enable() function. I2C_Start() must be called before I2C bus operation.
This API enables the I2C interrupt. Interrupts are required for most I2C operations.
The I2C Slave buffers must be set up before this function call to avoid reading or writing partial data while buffers set up.
I2C Slave behavior is as follows when enabled and buffers are not set up:
I2C Read transfer – Returns 0xFF until the read buffer is set up. Use function I2C_SlaveInitReadBuf() to set up read buffer;
I2C Write transfer – Send NAK because there is no place to store received data up. Use function I2C_SlaveInitWriteBuf() to set up read buffer;

Parameters: None
Return Value: None
Side Effects: None

void I2C_Stop(void)

Description: Disables I2C hardware and interrupt.
FF implementation (Production PSoC 3 only): Releases the I2C bus if it was locked up by device and sets it to the idle state.
UDB implementation: Releases the I2C bus if it was locked up by the device and sets it to the idle state.

Parameters: None
Return Value: None
Side Effects: None

void I2C_EnableInt(void)

Description: Enables I2C interrupt. Interrupts are required for most operations.

Parameters: None
Return Value: None
Side Effects: None
void I2C_DisableInt(void)

Description: Disables I2C interrupt. This function is not normally required because the I2C_Stop() function disables the interrupt.

Parameters: None

Return Value: None

Side Effects: If the I2C interrupt is disabled while the I2C is still running, it may cause the I2C bus to lock up.

void I2C_Sleep(void)

Description: This is the preferred API to prepare the component for sleep. The I2C interrupt is disabled after function call.

Wakeup on address match enabled: If a transaction intended for this device executes during this API call, it waits until the current transaction is completed. All subsequent I2C traffic intended for this device is NAKed until the device is put to sleep. The address match event wakes up the chip.

Wakeup on address match disabled: This API checks current I2C component state, saves it, and disables the component by calling I2C_Stop() if it is currently enabled. I2C_SaveConfig() is then called to save the I2C nonretention configuration registers. Call the I2C_Sleep() function before calling the CyPmSleep() or the CyPmHibernate() function. Refer to the PSoC Creator System Reference Guide for more information about power-management functions.

Parameters: None

Return Value: None

Side Effects: None

void I2C_Wakeup(void)

Description: This is the preferred API to restore the component to the state when I2C_Sleep() was last called. The I2C interrupt is enabled after function call.

Wakeup on address match enabled: This API enables I2C master functionality if it was enabled before sleep, and disables the I2C backup regulator. The incoming transaction continues as soon as the I2C interrupt is enabled.

Wakeup on address match disabled: This API restores the I2C nonretention configuration registers by calling I2C_RestoreConfig(). If the component was enabled before the I2C_Sleep() function was called, I2C_Wakeup() re-enables it.

Parameters: None

Return Value: None

Side Effects: Calling the I2C_Wakeup() function without first calling the I2C_Sleep() or I2C_SaveConfig() function may produce unexpected behavior.
void I2C_Init(void)

Description: Initializes or restores the component according to the customizer Configure dialog settings. It is not necessary to call I2C_Init() because the I2C_Start() API calls this function, which is the preferred method to begin component operation.

Parameters: None

Return Value: None

Side Effects: All registers will be set to values according to the customizer Configure dialog.

void I2C_Enable(void)

Description: Activates the hardware and begins component operation. It is not necessary to call I2C_Enable() because the I2C_Start() API calls this function, which is the preferred method to begin component operation. If this API is called, I2C_Start() or I2C_Init() must be called first.

Parameters: None

Return Value: None

Side Effects: None

void I2C_SaveConfig(void)

Description: This function saves the I2C component nonretention configuration registers and disables I2C interrupt

Wakeup on address match enabled: This API disables the I2C master, if it was enabled before, and enables the I2C backup regulator. If a transaction intended for this device executes during this API call, it waits until the current transaction is completed and I2C is ready to go to sleep. All subsequent I2C traffic is NAKed until the device is put to sleep.

Wakeup on address match disabled: Refer to main description above.

Disabling the I2C interrupt does not depend on whether wakeup on address match is enabled or disabled.

Parameters: None

Return Value: None

Side Effects: None
void I2C_RestoreConfig(void)

Description: This function restores the I²C component nonretention configuration registers, to the state they were in before I2C_Sleep() or I2C_SaveConfig() was called. Enables I²C interrupt.

Wakeup on address match enabled: This API enables I²C master functionality, if it was enabled before, and disables the I²C backup regulator.

Wakeup on address match disabled: Refer to main description above.

Enabling the I²C interrupt does not depend on whether wakeup on address match is enabled or disabled.

Parameters: None
Return Value: None
Side Effects: Calling this function without first calling the I2C_Sleep() or I2C_SaveConfig() function may produce unexpected behavior.

Slave Functions

This section lists the functions that are used for I²C slave operation. These functions are available if slave operation is enabled.

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_SlaveStatus()</td>
<td>Returns slave status flags.</td>
</tr>
<tr>
<td>I2C_SlaveClearReadStatus()</td>
<td>Returns read status flags and clears slave read status flags.</td>
</tr>
<tr>
<td>I2C_SlaveClearWriteStatus()</td>
<td>Returns the write status and clears the slave write status flags.</td>
</tr>
<tr>
<td>I2C_SlaveSetAddress()</td>
<td>Sets slave address, a value between 0 and 127 (0x00 to 0x7F).</td>
</tr>
<tr>
<td>I2C_SlaveInitReadBuf()</td>
<td>Sets up the slave receive data buffer. (master &lt;- slave)</td>
</tr>
<tr>
<td>I2C_SlaveInitWriteBuf()</td>
<td>Sets up the slave write buffer. (master -&gt; slave)</td>
</tr>
<tr>
<td>I2C_SlaveGetReadBufSize()</td>
<td>Returns the number of bytes read by the master since the buffer was reset.</td>
</tr>
<tr>
<td>I2C_SlaveGetWriteBufSize()</td>
<td>Returns the number of bytes written by the master since the buffer was reset.</td>
</tr>
<tr>
<td>I2C_SlaveClearReadBuf()</td>
<td>Resets the read buffer counter to zero.</td>
</tr>
<tr>
<td>I2C_SlaveClearWriteBuf()</td>
<td>Resets the write buffer counter to zero.</td>
</tr>
</tbody>
</table>
uint8 I2C_SlaveStatus(void)

Description: Returns the slave’s communication status.
Parameters: None
Return Value: uint8: Current status of I²C slave.

<table>
<thead>
<tr>
<th>Slave Status Constants</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_SSTAT_RD_CMPT</td>
<td>Slave read transfer complete. Set when master indicates it is done reading by sending a NAK</td>
</tr>
<tr>
<td>I2C_SSTAT_RD_BUSY</td>
<td>Slave read transfer in progress. Set when master addresses slave with a read, cleared when RD_CMPT is set.</td>
</tr>
<tr>
<td>I2C_SSTAT_RD_ERR_OVFL</td>
<td>Master attempted to read more bytes than are in buffer.</td>
</tr>
<tr>
<td>I2C_SSTAT_WR_CMPT</td>
<td>Slave write transfer complete. Set at reception of a Stop condition, or when WR_ERR_OVFL is set</td>
</tr>
<tr>
<td>I2C_SSTAT_WR_BUSY</td>
<td>Slave write transfer in progress. Set when the master addresses the slave with a write, cleared at reception of a Stop condition or when WR_ERR_OVFL is set</td>
</tr>
<tr>
<td>I2C_SSTAT_WR_ERR_OVFL</td>
<td>Master attempted to write past end of buffer.</td>
</tr>
</tbody>
</table>

Side Effects: None

uint8 I2C_SlaveClearReadStatus(void)

Description: Clears the read status flags and returns their values. No other status flags are affected.
Parameters: None
Return Value: uint8: Current read status of slave. See the I2C_SlaveStatus() function for constants.
Side Effects: None

uint8 I2C_SlaveClearWriteStatus(void)

Description: Clears the write status flags and returns their values. No other status flags are affected.
Parameters: None
Return Value: uint8: Current write status of slave. See the I2C_SlaveStatus() function for constants.
Side Effects: None
void I2C_SlaveSetAddress(uint8 address)

Description: Sets the I^2^C slave address
Parameters: uint8 address: I^2^C slave address for the primary device. This value may be any address between 0 and 127 (0x00 to 0x7F). This address is the 7-bit right-justified slave address and does not include the R/W bit.

Return Value: None
Side Effects: None

void I2C_SlaveInitReadBuf(uint8 * rdBuf, uint8 bufSize)

Description: Sets the buffer pointer and size of the read buffer. This function also resets the transfer count returned with the I2C_SlaveGetReadBufSize() function.
Parameters: uint8* rdBuf: Pointer to the data buffer to be read by the master.
uint8 bufSize: Size of the buffer exposed to the I^2^C master.

Return Value: None
Side Effects: If this function is called during a bus transaction, data from the previous buffer location and the beginning of the current buffer may be transmitted.

void I2C_SlaveInitWriteBuf(uint8 * wrBuf, uint8 bufSize)

Description: Sets the buffer pointer and size of the write buffer. This function also resets the transfer count returned with the I2C_SlaveGetWriteBufSize() function.
Parameters: uint8* wrBuf: Pointer to the data buffer to be written by the master.
uint8 bufSize: Size of the write buffer exposed to the I^2^C master.

Return Value: None
Side Effects: If this function is called during a bus transaction, data may be received in the previous buffer and the current buffer location.

uint8 I2C_SlaveGetReadBufSize(void)

Description: Returns the number of bytes read by the I^2^C master since an I2C_SlaveInitReadBuf() or I2C_SlaveClearReadBuf() function was executed. The maximum return value is the size of the read buffer.

Parameters: None
Return Value: uint8: Bytes read by master.
Side Effects: None
uint8 I2C_SlaveGetWriteBufSize(void)

Description: Returns the number of bytes written by the I²C master since an I2C_SlaveInitWriteBuf() or I2C_SlaveClearWriteBuf() function was executed.

The maximum return value is the size of the write buffer.

Parameters: None

Return Value: uint8: Bytes written by master.

Side Effects: None

void I2C_SlaveClearReadBuf(void)

Description: Resets the read pointer to the first byte in the read buffer. The next byte read by the master will be the first byte in the read buffer.

Parameters: None

Return Value: None

Side Effects: None

void I2C_SlaveClearWriteBuf(void)

Description: Resets the write pointer to the first byte in the write buffer. The next byte written by the master will be the first byte in the write buffer.

Parameters: None

Return Value: None

Side Effects: None

Master and Multi-Master Functions

These functions are only available if Master or Multi-Master mode is enabled.

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_MasterStatus()</td>
<td>Returns the master status.</td>
</tr>
<tr>
<td>I2C_MasterClearStatus()</td>
<td>Returns the master status and clears the status flags.</td>
</tr>
<tr>
<td>I2C_MasterWriteBuf()</td>
<td>Writes the referenced data buffer to a specified slave address.</td>
</tr>
<tr>
<td>I2C_MasterReadBuf()</td>
<td>Reads data from the specified slave address and places the data in the referenced buffer.</td>
</tr>
<tr>
<td>I2C_MasterSendStart()</td>
<td>Sends only a start to the specific address.</td>
</tr>
<tr>
<td>I2C_MasterSendRestart()</td>
<td>Sends only a restart to the specified address.</td>
</tr>
<tr>
<td>I2C_MasterSendStop()</td>
<td>Generates a stop condition.</td>
</tr>
<tr>
<td>Function</td>
<td>Description</td>
</tr>
<tr>
<td>---------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>I2C_MasterWriteByte()</td>
<td>Writes a single byte. This is a manual command that should only be used with</td>
</tr>
<tr>
<td></td>
<td>the I2C_MasterSendStart() or I2C_MasterSendRestart() functions.</td>
</tr>
<tr>
<td>I2C_MasterReadByte()</td>
<td>Reads a single byte. This is a manual command that should only be used with</td>
</tr>
<tr>
<td></td>
<td>the I2C_MasterSendStart() or I2C_MasterSendRestart() functions.</td>
</tr>
<tr>
<td>I2C_MasterGetReadBufSize()</td>
<td>Returns the byte count of data read since the I2C_MasterClearReadBuf()</td>
</tr>
<tr>
<td></td>
<td>function was called.</td>
</tr>
<tr>
<td>I2C_MasterGetWriteBufSize()</td>
<td>Returns the byte count of the data written since the</td>
</tr>
<tr>
<td></td>
<td>I2C_MasterClearWriteBuf() function was called.</td>
</tr>
<tr>
<td>I2C_MasterClearReadBuf()</td>
<td>Resets the read buffer pointer back to the beginning of the buffer.</td>
</tr>
<tr>
<td>I2C_MasterClearWriteBuf()</td>
<td>Resets the write buffer pointer back to the beginning of the buffer.</td>
</tr>
</tbody>
</table>
uint8 I2C_MasterStatus(void)

Description: Returns the master’s communication status.
Parameters: None
Return Value: uint8: Current status of I2C master. I2C master status constants may be ORed together.

<table>
<thead>
<tr>
<th>Master status constants</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_MSTAT_RD_CMPLT</td>
<td>Read transfer complete. The error condition bits must be checked to ensure that read transfer was successful.</td>
</tr>
<tr>
<td>I2C_MSTAT_WR_CMPLT</td>
<td>Write transfer complete. The error condition bits must be checked to ensure that write transfer was successful.</td>
</tr>
<tr>
<td>I2C_MSTAT_XFER_INP</td>
<td>Transfer in progress</td>
</tr>
<tr>
<td>I2C_MSTAT_XFER_HALT</td>
<td>Transfer has been halted. The I2C bus is waiting for restart or stop condition generation.</td>
</tr>
<tr>
<td>I2C_MSTAT_ERR_SHORT_XFER</td>
<td>Error condition: Write transfer completed before all bytes were transferred.</td>
</tr>
<tr>
<td>I2C_MSTAT_ERR_ADDR_NAK</td>
<td>Error condition: Slave did not acknowledge address.</td>
</tr>
<tr>
<td>I2C_MSTAT_ERR_ARB_LOST</td>
<td>Error condition: Master lost arbitration during communications with slave.</td>
</tr>
<tr>
<td>I2C_MSTAT_ERR_XFER</td>
<td>Error condition: This is the ORed value of error conditions provided above. If all error condition bits are cleared, but this is set, the transfer was aborted due to Slave operation.</td>
</tr>
</tbody>
</table>

Side Effects: None

uint8 I2C_MasterClearStatus(void)

Description: Clears all status flags and returns the master status.
Parameters: None
Return Value: uint8: Current status of master. See the I2C_MasterStatus() function for constants.
Side Effects: None
uint8 I2C_MasterWriteBuf(uint8 slaveAddress, uint8 * wrData, uint8 cnt, uint8 mode)

**Description:** Automatically writes an entire buffer of data to a slave device. Once the data transfer is initiated by this function, further data transfer is handled by the included ISR in byte-by-byte mode. Enables I2C interrupt.

**Parameters:**
- uint8 slaveAddress: Right-justified 7-bit Slave address (valid range 0 to 127).
- uint8 wrData: Pointer to buffer of data to be sent.
- uint8 cnt: Number of bytes of buffer to send.
- uint8 mode: Transfer mode defines: (1) Whether a start or restart condition is generated at the beginning of the transfer, and (2) Whether the transfer is completed or halted before the stop condition is generated on the bus.

Transfer mode, mode constants may be ORed together.

<table>
<thead>
<tr>
<th>Mode Constants</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_MODE_COMPLETE_XFER</td>
<td>Perform complete transfer from Start to Stop.</td>
</tr>
<tr>
<td>I2C_MODE_REPEAT_START</td>
<td>Send Repeat Start instead of Start.</td>
</tr>
<tr>
<td>I2C_MODE_NO_STOP</td>
<td>Execute transfer without a Stop</td>
</tr>
</tbody>
</table>

**Return Value:** uint8: Error Status. See the I2C_MasterSendStart() function for constants.

**Side Effects:** None

uint8 I2C_MasterReadBuf(uint8 slaveAddress, uint8 * rdData, uint8 cnt, uint8 mode)

**Description:** Automatically reads an entire buffer of data from a slave device. Once the data transfer is initiated by this function, further data transfer is handled by the included ISR in byte by byte mode. Enables I2C interrupt.

**Parameters:**
- uint8 slaveAddress: Right-justified 7-bit Slave address (valid range 0 to 127).
- uint8 rdData: Pointer to buffer where to put data from slave.
- uint8 cnt: Number of bytes of buffer to read.
- uint8 mode: Transfer mode defines: (1) Whether a start or restart condition is generated at the beginning of the transfer and (2) Whether the transfer is completed or halted before the stop condition is generated on the bus.

Transfer mode, mode constants may be ORed together.

<table>
<thead>
<tr>
<th>Mode Constants</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_MODE_COMPLETE_XFER</td>
<td>Perform complete transfer for Start to Stop.</td>
</tr>
<tr>
<td>I2C_MODE_REPEAT_START</td>
<td>Send Repeat Start instead of Start.</td>
</tr>
<tr>
<td>I2C_MODE_NO_STOP</td>
<td>Execute transfer without a Stop</td>
</tr>
</tbody>
</table>

**Return Value:** uint8: Error Status. See the I2C_MasterSendStart() function for constants.

**Side Effects:** None
uint8 I2C_MasterSendStart(uint8 slaveAddress, uint8 R_nW)

Description: Generates start condition and sends slave address with read/write bit. Disables the I2C interrupt.

Parameters:  
uint8 slaveAddress: Right justified 7-bit Slave address (valid range 0 to 127).  
uint8 R_nW: Set to zero, send write command; set to nonzero, send read command.

Return Value: uint8: Error Status.

<table>
<thead>
<tr>
<th>Mode Constants</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_MSTR_NO_ERROR</td>
<td>Function complete without error.</td>
</tr>
<tr>
<td>I2C_MSTR_BUS_BUSY</td>
<td>Bus is busy occurred, start condition generation not started.</td>
</tr>
<tr>
<td>I2C_MSTR_NOT_READY</td>
<td>Master is not valid master on the bus or Slave operation is in progress.</td>
</tr>
<tr>
<td>I2C_MSTR_ERR_LB_NAK</td>
<td>Last byte was NAKed.</td>
</tr>
<tr>
<td>I2C_MSTR_ERR_ARB_LOST</td>
<td>Master lost arbitration while start is generated. (This status is only valid if Multi-Master enabled.)</td>
</tr>
<tr>
<td>I2C_MSTR_ABORT_XFER</td>
<td>The start condition generation was aborted due to start of Slave operation. (This status is only valid in Multi-Master-Slave mode.)</td>
</tr>
</tbody>
</table>

Side Effects: This function is blocking and doesn’t exit until the byte_complete bit is set in the I2C_CSR register.

uint8 I2C_MasterSendRestart(uint8 slaveAddress, uint8 R_nW)

Description: Generates restart condition and sends slave address with read/write bit.

Parameters:  
uint8 slaveAddress: Right-justified 7-bit Slave address (valid range 0 to 127).  
uint8 R_nW: Set to zero, send write command; set to nonzero, send read command.

Return Value: uint8: Error Status. See I2C_MasterSendStart() function for constants.

Side Effects: This function is blocking and doesn’t exit until the byte_complete bit is set in the I2C_CSR register.
uint8 I2C_MasterSendStop(void)

Description: Generates I^2^C stop condition on bus. This function does nothing if start or restart conditions failed before this function was called.

Parameters: None

Return Value: uint8: Error Status. See the I2C_MasterSendStart() command for constants.

Side Effects: This function is blocking and doesn’t exit until:

Master: This function waits while a stop condition is generated.

Multi-Master, Multi-Master-Slave: This function waits while a stop condition is generated or arbitrage is lost on ACK/NAK bit.

uint8 I2C_MasterWriteByte(uint8 theByte)

Description: Sends one byte to a slave. A valid start or restart condition must be generated before calling this function. This function does nothing if start or restart conditions failed before this function was called.

Parameters: uint8 theByte: Data byte to send to the slave.

Return Value: uint8: Error Status.

Side Effects: 

<table>
<thead>
<tr>
<th>Mode Constants</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_MSTR_NO_ERROR</td>
<td>Function complete without error.</td>
</tr>
<tr>
<td>I2C_MSTR_NOT_READY</td>
<td>Master is not valid master on the bus or Slave operation is in progress.</td>
</tr>
<tr>
<td>I2C_MSTR_ERR_LB_NAK</td>
<td>Last byte was NAKed.</td>
</tr>
<tr>
<td>I2C_MSTR_ERR_ARB_LOST</td>
<td>Master lost arbitration while start is generated. (This status is only valid if Multi-Master is enabled.)</td>
</tr>
</tbody>
</table>

uint8 I2C_MasterReadByte(uint8 acknNak)

Description: Reads one byte from a slave and ACKs or NAKs the transfer. A valid start or restart condition must be generated before calling this function. This function does nothing and returns a zero value if start or restart conditions failed before this function was called.

Parameters: uint8 acknNak: If zero, sends a NAK; if nonzero sends an ACK.

Return Value: uint8: Byte read from the slave

Side Effects: This function is blocking and doesn’t exit until the byte_complete bit is set in the I2C_CSR register.
uint8 I2C_MasterGetReadBufSize(void)
Description: Returns the number of bytes that has been transferred with an I2C_MasterReadBuf() function.
Parameters: None
Return Value: uint8: Byte count of transfer. If the transfer is not yet complete, it returns the byte count transferred so far.
Side Effects: None

uint8 I2C_MasterGetWriteBufSize(void)
Description: Returns the number of bytes that have been transferred with an I2C_MasterWriteBuf() function.
Parameters: None
Return Value: uint8: Byte count of transfer. If the transfer is not yet complete, it returns the byte count transferred so far.
Side Effects: None

void I2C_MasterClearReadBufSize(void)
Description: Resets the read buffer pointer back to the first byte in the buffer.
Parameters: None
Return Value: None
Side Effects: None

void I2C_MasterClearWriteBufSize(void)
Description: Resets the write buffer pointer back to the first byte in the buffer.
Parameters: None
Return Value: None
Side Effects: None

Multi-Master-Slave Functions
Multi-Master-Slave incorporates Slave and Multi-Master functions.
Bootloader Support

The I²C component can be used as a communication component for the Bootloader. Use the following configuration to support communication protocol from an external system to the Bootloader:

- Mode: Slave
- Implementation: Either fixed-function or UDB-based
- Data Rate: Must match Host (boot device) data rate.
- Slave Address: Must match Host (boot device) selected slave address.
- Address Match: Doesn’t care (Hardware is preferred)
- Pin Connections: Doesn’t care

For more information about the Bootloader, refer to the “Bootloader System” section of the System Reference Guide.

For additional information about I²C communication component implementation, refer to the Bootloader Protocol Interaction with I²C Communication Component section.

The I²C Component provides a set of API functions for the Bootloader usage.

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_CyBtldrCommStart</td>
<td>Starts the I²C component and enables its interrupt.</td>
</tr>
<tr>
<td>I2C_CyBtldrCommStop</td>
<td>Disable the I²C component and disables its interrupt.</td>
</tr>
<tr>
<td>I2C_CyBtldrCommReset</td>
<td>Sets read and write I²C buffers to the initial state and resets the slave status.</td>
</tr>
<tr>
<td>I2C_CyBtldrCommWrite</td>
<td>Allows the caller to write data to the bootloader host. This function handles polling to allow a block of data to be completely sent to the host device.</td>
</tr>
<tr>
<td>I2C_CyBtldrCommRead</td>
<td>Allows the caller to read data from the bootloader host. This function handles polling to allow a block of data to be completely received from the host device.</td>
</tr>
</tbody>
</table>

**void I2C_CyBtldrCommStart(void)**

**Description:**
Starts the I²C component and enables its interrupt.
Every incoming I²C write transaction is treated as a command for the bootloader.
Every incoming I²C read transaction returns 0xFF until the bootloader provides a response to the executed command.

**Parameters:**
None

**Return Value:**
None

**Side Effects:**
None
void I2C_CyBtldrCommStop(void)

Description: Disables the I²C component and disables its interrupt.
Parameters: None
Return Value: None
Side Effects: None

void I2C_CyBtldrCommReset(void)

Description: Sets read and write I²C buffers to the initial state and resets the slave status.
Parameters: None
Return Value: None
Side Effects: None

cystatus I2C_CyBtldrCommRead(uint8 * Data, uint16 size, uint16 * count, uint8 timeOut)

Description: Allows the caller to read data from the bootloader host. The function handles polling to allow a block of data to be completely received from the host device.
Parameters: uint8 *Data: Pointer to the block of data to send to the device.
uint16 size: Number of bytes to write.
uint16 *count: Pointer to variable to write the number of bytes actually written.
uint8 timeOut: Number of units in 10 ms to wait before returning because of a timeout.
Return Value: cystatus: Returns CYRET_SUCCESS if no problem was encountered or returns the value that best describes the problem. For more information, refer to the "Return Codes" section of the System Reference Guide.
Side Effects: None

cystatus I2C_CyBtldrCommWrite(uint8 * Data, uint16 size, uint16 * count, uint8 timeOut)

Description: Allows the caller to write data to the bootloader host. The function handles polling to allow a block of data to be completely sent to the host device.
Parameters: uint8 *Data: Pointer to the block of data to send to the device.
uint16 size: Number of bytes to write.
uint16 *count: Pointer to variable to write the number of bytes actually written.
uint8 timeOut: Number of units in 10 ms to wait before returning because of a timeout.
Return Value: cystatus: Returns CYRET_SUCCESS if no problem was encountered or returns the value that best describes the problem. For more information refer to the "Return Codes" section of the System Reference Guide.
Side Effects: None
Sample Firmware Source Code

PSOC Creator provides many example projects that include schematics and example code in the Find Example Project dialog. For component-specific examples, open the dialog from the Component Catalog or an instance of the component in a schematic. For general examples, open the dialog from the Start Page or File menu. As needed, use the Filter Options in the dialog to narrow the list of projects available to select.

Refer to the “Find Example Project” topic in the PSOC Creator Help for more information.

Functional Description

This component supports I²C slave, master, multi-master, and multi-master-slave configurations. The following sections provide an overview of how to use the slave, master, and multi-master components.

This component requires that you enable global interrupts since the I²C hardware is interrupt driven. Even though this component requires interrupts, you do not need to add any code to the ISR (interrupt service routine). The component services all interrupts (data transfers) independent of your code. The memory buffers allocated for this interface look like simple dual-port memory between your application and the I²C master/slave.

Slave Operation

The slave interface consists of two buffers in memory, one for data written to the slave by a master and a second buffer for data read by a master from the slave. Remember that reads and writes are from the perspective of the I²C master. The I²C slave read and write buffers are set by the initialization commands below. These commands do not allocate memory, but instead copy the array pointer and size to the internal component variables. You must instantiate the arrays used for the buffers because they are not automatically generated by the component. The same buffer may be used for both read and write buffers, but you must be careful to manage the data properly.

```c
void I2C_SlaveInitReadBuf(uint8 * rdBuf, uint8 bufSize)
void I2C_SlaveInitWriteBuf(uint8 * wrBuf, uint8 bufSize)
```

Using the functions above sets a pointer and byte count for the read and write buffers. The bufSize for these functions may be less than or equal to the actual array size, but it should never be larger than the available memory pointed to by the rdBuf or wrBuf pointers.
When the `I2C_SlaveInitReadBuf()` or `I2C_SlaveInitWriteBuf()` functions are called, the internal index is set to the first value in the array pointed to by `rdBuf` and `wrBuf`, respectively. As bytes are read or written by the I²C master, the index is incremented until the offset is one less than the `byteCount`. At any time the number of bytes transferred may be queried by calling either `I2C_SlaveGetReadBufSize()` or `I2C_SlaveGetWriteBufSize()` for the read and write buffers, respectively. Reading or writing more bytes than are in the buffers causes an overflow error. The error is set in the slave status byte and may be read with the `I2C_SlaveStatus()` API.

To reset the index back to the beginning of the array, use the following commands.

```c
void I2C_SlaveClearReadBuf(void)
void I2C_SlaveClearWriteBuf(void)
```

This resets the index back to zero. The next byte read or written to by the I²C master is the first byte in the array. Before these clear buffer commands are used, the data in the arrays should be read or updated.

Multiple reads or writes by the I²C master continue to increment the array index until the clear buffer commands are used or the array index attempts to grow beyond the array size. Figure 2 shows an example where an I²C master has executed two write transactions. The first write was four bytes and the second write was six bytes. The sixth byte in the second transaction was NAKed by the slave to signal that the end of the buffer had occurred. If the master tried to write a seventh byte for the second transaction or started to write more bytes with a third transaction, each byte would be NAKed and discarded until the buffer is reset.

Using the `I2C_SlaveClearWriteBuf()` function after the first transaction resets the index back to zero and causes the second transaction to overwrite the data from the first transaction. Make
sure data is not lost by overflowing the buffer. The data in the buffer should be processed by the slave before resetting the buffer index.

Figure 2. System Memory

Both the read and write buffers have four status bits to signal transfer complete, transfer in progress, and buffer overflow. When a transfer starts, the busy flag is set. When the transfer is complete, the transfer complete flag is set and the busy flag is cleared. If a second transfer is started, both the busy and transfer complete flags may be set at the same time. The following table shows read and write status flags.

<table>
<thead>
<tr>
<th>Slave Status Constants</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_SSTAT_RD_CMPT</td>
<td>0x01</td>
<td>Slave read transfer complete</td>
</tr>
<tr>
<td>I2C_SSTAT_RD_BUSY</td>
<td>0x02</td>
<td>Slave read transfer in progress (busy)</td>
</tr>
<tr>
<td>I2C_SSTAT_RD_OVFL</td>
<td>0x04</td>
<td>Master attempted to read more bytes than are in buffer</td>
</tr>
<tr>
<td>I2C_SSTAT_WR_CMPT</td>
<td>0x10</td>
<td>Slave write transfer complete</td>
</tr>
<tr>
<td>I2C_SSTAT_WR_BUSY</td>
<td>0x20</td>
<td>Slave Write transfer in progress (busy)</td>
</tr>
<tr>
<td>I2C_SSTAT_WR_OVFL</td>
<td>0x40</td>
<td>Master attempted to write past end of buffer</td>
</tr>
</tbody>
</table>

The following code example initializes the write buffer then waits for a transfer to complete. Once the transfer is complete, the data is then copied into a working array to handle the data. In many applications, the data does not have to be copied to a second location, but instead can be processed in the original buffer. You could create an almost identical read buffer example by replacing the write functions and constants with read functions and constants. Processing the data may mean new data is transferred into the slave buffer instead of out.
```c
uint8 wrBuf[10];
uint8 userArray[10];
uint8 byteCnt;

/* Initialize write buffer before call I2C_Start */
I2C_SlaveInitWriteBuf((uint8 *)wrBuf, 10);

/* Start I2C Slave operation */
I2C_Start();

/* Wait for I2C master to complete a write */
for(;;) /* loop forever */
{
    /* Wait for I2C master to complete a write */
    if(0u != (I2C_SlaveStatus() & I2C_SSTAT_WR_CMPT))
    {
        byteCnt = I2C_SlaveGetWriteBufSize();
        I2C_SlaveClearWriteStatus();
        for(i=0; i < byteCnt; i++)
        {
            userArray[i] = wrBuf[i]; /* Transfer data */
        }
        I2C_SlaveClearWriteBuf();
    }
}
```

### Master/Multi-Master Operation

Master and Multi-Master\(^3,4\) operation are basically the same, with two exceptions. When operating in Multi-Master mode, the bus should always be checked to see if it is busy. Another master may already be communicating with another slave. In this case, the program must wait until the current operation is complete before issuing a start transaction. The program looks at the return value, which sets an error if another master has control of the bus.

The second difference is that, in Multi-Master mode, two masters can start at the exact same time. If this happens, one of the two masters loses arbitration. You must check for this condition after each byte is transferred. The component automatically checks for this condition and responds with an error if arbitration is lost.

There are two options when operating the \(^2\)C master: manual and automatic. In the automatic mode, a buffer is created to hold the entire transfer. In the case of a write operation, the buffer is

---

\(^3\) In fixed-function implementation for PSoC 3 ES2 and PSoC 5 in Master or Multi-Master mode, if the STOP condition is set by the software immediately after the START condition, the module will generate the STOP condition. This happens after the address field (sends 0xFF if data write), and the clock line remains low. To avoid this condition, do not set the STOP condition immediately after START; transfer at least a byte and set the STOP condition after NAK or ACK.

\(^4\) Fixed-Function implementation does not support undefined bus conditions. Avoid these conditions, or use the UDB-based implementation instead.
prefilled with the data to be sent. If data is to be read from the slave, a buffer at least the size of the packet needs to be allocated. To write an array of bytes to a slave in automatic mode, use the following function.

```c
uint8 I2C_MasterWriteBuf(uint8 slaveAddress, uint8 * xferData, uint8 cnt, uint8 mode)
```

The slaveAddress variable is a right-justified 7-bit slave address of 0 to 127. The component API automatically appends the write flag to the LSb of the address byte. The array of data to transfer is pointed to with the second parameter, xferData. The cnt parameter is the number of bytes to transfer. The last parameter, mode, determines how the transfer starts and stops. A transaction may begin with a restart instead of a start, or halt before the stop sequence. These options allow back-to-back transfers where the last transfer does not send a stop and the next transfer issues a restart instead of a start.

A read operation is almost identical to the write operation. The same parameters with the same constants are used.

```c
uint8 I2C_MasterReadBuf(uint8 slaveAddress, uint8 * xferData, uint8 cnt, uint8 mode);
```

Both of these functions return status. See the status table for the I2C_MasterStatus() function return value. Since the read and write transfers complete in the background during the I2C interrupt code, the I2C_MasterStatus() function can be used to determine when the transfer is complete. A code snippet that shows a typical write to a slave follows.

```c
I2C_MasterClearStatus(); /* Clear any previous status */
I2C_MasterWriteBuf(4, (uint8 *) wrData, 10, I2C_MODE_COMPLETE_XFER);
for(;;)
{
    if(0u != (I2C_MasterStatus() & I2C_MSTAT_WR_CMPLT))
    {
        /* Transfer complete. Check Master status to make sure that transfer completed without errors. */

        break;
    }
}
```

The I2C master can also be operated manually. In this mode, each part of the write transaction is performed with individual commands.

```c
status = I2C_MasterSendStart(4, I2C_WRITE_XFER_MODE);
if(status == I2C_MSTR_NO_ERROR) /* Check if transfer completed without errors */
{
    /* Send array of 5 bytes */
    for(i=0; i<5; i++)
    {
        status = I2C_MasterWriteByte(userArray[i]);
        if(status != I2C_MSTR_NO_ERROR)
        {
```
break;
}
}
I2C_MasterSendStop(); /* Send Stop */

A manual read transaction is similar to the write transaction except the last byte should be NAKed. The example below shows a typical manual read transaction.

```c
status = I2C_MasterSendStart(4, I2C_READ_XFER_MODE);
if(status == I2C_MSTR_NO_ERROR) /* Check if transfer completed without errors */
{
    /* Read array of 5 bytes */
    for(i=0; i<5; i++)
    {
        if(i < 4)
            userArray[i] = I2C_MasterReadByte(I2C_ACK_DATA);
        else
            userArray[i] = I2C_MasterReadByte(I2C_NAK_DATA);
    }
}
I2C_MasterSendStop(); /* Send Stop */
```

### Multi-Master-Slave Mode Operation

Both Multi-Master and Slave are operational in this mode. The component may be addressed as a slave, but firmware may also initiate master mode transfers. In this mode, when a master loses arbitration during an address byte, the hardware reverts to Slave mode and the received byte generates a slave address interrupt.

For Master and Slave operation examples look at the Slave Operation and Master/Multi-Master Operation sections.

**Arbitrage on address byte limitations with hardware address match enabled:** When a master loses arbitration during an address byte, the slave address interrupt is only generated if slave is addressed. In other cases, the lost arbitration status is lost by interrupt-based functions. The software address detect eliminates this possibility, but excludes the Wakeup on Hardware Address Match feature.

The manual function I2C_MasterSendStart() provides correct status information in the case described above.

### Start of Multi-Master-Slave Transfer

When using Multi-Master-Slave, the Slave can be addressed at any time. The Multi-Master must take time to prepare to generate a start condition when the bus is free. During this time, the Slave could be addressed and, in this case, the Multi-Master transaction is lost and Slave
operation proceeds. Be careful not to break the Slave operation; the I²C interrupt must be disabled before generating a start condition to prevent the transaction from passing the address stage. This action allows you to abort a Multi-Master transaction and start Slave operation correctly. The following cases are possible when disabling the I²C interrupt:

- The bus is busy (Slave operation is in progress or other traffic is on the bus) before start generation. The Multi-Master does not try to generate a start condition. Slave operation proceeds when the I²C interrupt is enabled. The I2C_MasterWriteBuf(), I2C_MasterReadBuf(), or I2C_MasterSendStart() call returns the status I2C_MSTR_BUS_BUSY.

- The bus is free before start generation. The Multi-Master generates a start condition on the bus and proceeds with operation when I²C interrupt is enabled. The I2C_MasterWriteBuf(), I2C_MasterReadBuf(), or I2C_MasterSendStart() call returns the status I2C_MSTR_NO_ERROR.

- The bus is free before start generation. The Multi-Master tries to generate a start but another Multi-Master addresses the Slave before this and the bus becomes busy. The start condition generation is queued. The Slave operation stops at the address stage because of a disabled I²C interrupt. When I²C interrupt is enabled, the Multi-Master transaction is aborted from queue and Slave operation proceeds. The I2C_MasterWriteBuf() or I2C_MasterReadBuf() call does not notice this and returns I2C_MSTR_NO_ERROR. The I2C_MasterStatus() returns I2C_MSTAT_WR_CMPLT or I2C_MSTAT_RD_CMPLT with I2C_MSTAT_ERR_XFER (all other error condition bits are cleared) after the Multi-Master transaction is aborted. The I2C_MasterSendStart() call returns the error status I2C_MSTR_ABORT_XFER.

Interrupt Function Operation

- I2C_MasterWriteBuf();

- I2C_MasterReadBuf();

    I2C_MasterClearStatus(); /* Clear any previous status */
    I2C_DisableInt(); /* Disable interrupt */

    status = I2C_MasterWriteBuf(4, (uint8 *) wrData, 10, I2C_MODE_COMPLETE_XFER);
    /* Try to generate, start. The disabled I2C interrupt halt the transaction on address stage in case of Slave addressed or Master generates start condition */

    I2C_EnableInt(); /* Enable interrupt and proceed Master or Slave transaction */

    for(;;)
    {
        if(0u != (I2C_MasterStatus() & I2C_MSTAT_WR_CMPLT))
        {
            /* Transfer complete. Check Master status to make sure that transfer completed without errors. */
            break;
        }
if (0u != (I2C_MasterStatus() & I2C_MSTAT_ERR_XFER))
{
    /* Error occurred while transfer, clean up Master status and
    retry the transfer */
}

Manual Function Operation

Manual Multi-Master operation assumes that I²C interrupt is disabled, but it is best to take the
following precaution:

I2C_DisableInt(); /* Disable interrupt */
status = I2C_MasterSendStart(4, I2C_WRITE_XFER_MODE);; /* Try to generate start
condition */
if (status == I2C_MSTR_NO_ERROR) /* Check if start generation completed without
errors */
{
    /* Proceed the write operation */
    /* Send array of 5 bytes */
    for (i=0; i<5; i++)
    {
        status = I2C_MasterWriteByte(userArray[i]);
        if (status != I2C_MSTR_NO_ERROR)
            break;
    }
    I2C_MasterSendStop(); /* Send Stop */
}
I2C_EnableInt(); /* Enable interrupt, if it was enabled before */

Wakeup on Hardware Address Match

The wakeup from sleep on I²C address match event is possible if the following demands are met:

- The I²C slave should be enabled. Slave or Multi-Master-Slave mode is selected.
- The I²C Hardware address detection is selected.
- The SIO pair is connected to SCL and SDA and the proper pair is selected in the customizer:
  I2C0 – SCL P12[4], SDA P12[5] and I2C1 – SCL P12[0], SDA P12[1].

The following demands are controlled by the I²C component customizer, except correct pin
assignments.
How it Works

The I^2C block responds to transactions on the I^2C bus during sleep mode. The I2C wakes the system if the incoming address matches with the slave address. Once the address matches, wakeup interrupt is asserted to wake up the system and SCL is pulled low. The ACK is sent out after the system wakes up and the CPU determines the next action in the transaction.

Wakeup and Clock Stretching

The I^2C slave stretches the clock while exiting sleep mode. All clocks in the system must be restored before continuing the I^2C transactions. The I^2C interrupt is disabled before going to sleep and only enabled after the I2C_Wakeup() function is called. The time between wakeup and end of calling I2C_Wakeup(), SCL line is pulled low.

Sample code:

```c
...  
I2C_Sleep();  /* Go to Sleep and disable I2C interrupt */  
CyPmSaveClocks();  /* Save clocks settings */  
CyPmSleep(PM_SLEEP_TIME_NONE, PM_SLEEP_SRC_I2C);  
CyPmRestoreClocks();  /* Restore clocks */  
I2C_Wakeup();  /* Wakeup, enable I2C interrupt and ACK the address, till end of this call the SCL is pulled low */  
...  
```

Bootloader Protocol Interaction with I^2C Communication Component

The bootloader protocol is implemented as command (write transaction) and response (read transaction).

The time between the Host issuing the command and the bootloader sending back the response is the command execution time. The I^2C communication component for the bootloader is designed in this way: when the Host asks for a response, and bootloader still executes command, 0xFF is returned.

**Startup:** The I^2C bootloader communication component expects to receive the command and does not have a valid response yet. All read transactions from the Host return 0xFF. All write transactions are treated as command.
Bootloader process: The Host is issued the command with single write transaction and starts polling for a response. The \( \text{I}^2\text{C} \) communication component answers with 0xFF until a valid response is passed by the bootloader. After receiving 0x01, the Host must perform another read to get the remaining N – 1 bytes of the response. Once both reads are complete, the results should be combined to form the full response packet.

Polling must be executed by reading one byte; reading more bytes could corrupt the response. For example, 0xFF 0x01 0x03 (two bytes of response were read, instead of one). The next read of the full response returns two invalid bytes, because these bytes were already read (0x01 and 0x03).

How to avoid polling: You should measure the command execution time (\( T_{\text{com}_{-}\text{ex}} \)) plus response setup time (\( T_{\text{resp}_{-}\text{set}} \)) according to the system settings (CPU speed, compiler, compiler optimization level). The Host must ask for the response after this time. The command execution time changes across the commands, so you should choose the greater time.

Clock stretching while polling: The \( \text{I}^2\text{C} \) communication component requires that interrupts be enabled while in operation. The command Program Row (0x39), which writes one row of flash data to the device, requires interrupts to be disabled. Clock stretching occurs if the address is accepted by the \( \text{I}^2\text{C} \) communication component while interrupts are disabled.

How to Avoid Clock Stretching: To avoid clock stretching, the Command Program Row (0x39) execution time (\( T_{\text{com}_{-}\text{ex}} \)) should be measured according to the system settings (CPU speed, compiler, compiler optimization level). The Host must ask for response after this time.
External Electrical Connections

As Figure 3 shows, the I²C bus requires external pull-up resistors. The pull-up resistors (R_P) are determined by the supply voltage, clock speed, and bus capacitance. Make the minimum sink current for any device (master or slave) no less than 3 mA at V_{OL\text{max}} = 0.4 V for the output stage. This limits the minimum pull-up resistor value for a 5-V system to about 1.5 kΩ. The maximum value for R_P depends upon the bus capacitance and clock speed. For a 5-V system with a bus capacitance of 150 pF, the pull-up resistors are no larger than 6 kΩ. For more information about sizing pull-up resistors and other physical bus specifications, see *The I²C-Bus Specification* on the NXP web site at www.nxp.com.

Figure 3. Connection of Devices to the I²C Bus

![Diagram of I²C bus connections](image)

**Note** Purchase of I²C components from Cypress or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips. As of October 1, 2006, Philips Semiconductors has a new trade name - NXP Semiconductors.

Interrupt Service Routine

The interrupt service routine is used by the component code and should not be modified.

The following user sections are provided for Slave:

- Custom includes and definitions
- Additional address compare
- Prepare read buffer

There are no user sections provided for Master.
The I^2C component uses interrupt for most operations; the status of a transaction is updated there. Status read and clear functions are not protected from interrupting. These functions are listed below:

Master or Multi-Master:
- I2C_MasterStatus()
- I2C_MasterClearStatus()
- I2C_MasterGetReadBufSize()
- I2C_MasterGetWriteBufSize()
- I2C_MasterClearReadBuf()
- I2C_MasterClearWriteBuf()

Slave:
- I2C_SlaveStatus()
- I2C_SlaveClearReadStatus()
- I2C_SlaveClearWriteStatus()
- I2C_SlaveInitReadBuf()
- I2C_SlaveInitWriteBuf()
- I2C_SlaveGetReadBufSize()
- I2C_SlaveGetWriteBufSize()
- I2C_SlaveClearReadBuf()
- I2C_SlaveClearWriteBuf()
## Registers

The functions provided support the common runtime functions required for most applications. The following register references provide brief descriptions for the advanced user. The I2C_Data register may be used to write data directly to the bus without using the API. This may be useful for either CPU or DMA use.

The registers available to each of the configurations of the I²C component are grouped according to the implementation as fixed function or UDB.

### Fixed-Function Master/Slave Registers

See the chip Technical Reference Manual (TRM) for more information on these registers. All bits that are added in the Production PSoC3 chip are indicated with an asterisk (*) in the definitions listed below.

#### I2C_XCFG

The extended configuration register is available in the fixed-function hardware block to configure the hardware address mode and clock source.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>csr_clk_en</td>
<td>i2c_on*</td>
<td>ready_to_sleep*</td>
<td>force_nak*</td>
<td>RSVD</td>
<td>hw_addr_en</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **csr_clk_en**: Used to enable gating for the fixed function block core logic.
- **i2c_on***: Used to select I²C block as wakeup source.
- **ready_to_sleep***: Used to notify that block is ready to sleep.
- **force_nak***: Used to force NAK the transaction.
- **hw_addr_en**: Used to enable hardware address comparison.

#### I2C_ADDR

The slave address register is available in the fixed function hardware block to configure the slave device address for hardware comparison mode if enabled in the XCFG register above.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>RSVD</td>
<td></td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>slave_address</td>
</tr>
</tbody>
</table>

- **slave_address**: Used to define the 7-bit slave address for hardware address comparison mode.
I2C_CFG

The configuration register is available in the fixed function hardware block to configure the basic functionality.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>sio_select</td>
<td>pselect</td>
<td>bus_error_ie</td>
<td>stop_ie</td>
<td>clock_rate[1:0]</td>
<td>en_mstr</td>
<td>en_slave</td>
<td></td>
</tr>
</tbody>
</table>

- **sio_select**: Used to select between SIO1 and SIO2 lines for SCL and SDA; pselect must be set for this bit to have an effect.
- **pselect**: Used to select between SIO direct connections or DSI routed GPIO/SIO pins for SCL and SDA lines.
- **bus_error_ie**: Used to enable interrupt generation for bus_error.
- **stop_ie**: Used to enable interrupt generation on stop bit detection.
- **clock_rate**: Used to select between 16-bit or 32-bit oversample. Production PSoC3 only uses bit2.
- **en_mstr**: Used to enable master mode.
- **en_slave**: Used to enable slave mode.

I2C_CSR

The control and status register is available in the fixed-function hardware block for runtime control and status feedback.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>bus_error</td>
<td>lost_arb*</td>
<td>stop_status</td>
<td>ack</td>
<td>address</td>
<td>transmit</td>
<td>lrb</td>
<td>byte_complete</td>
</tr>
</tbody>
</table>

- **bus_error**: Bus error detection status bit. This must be cleared by writing a ‘0’ to this bit position.
- **lost_arb***: Lost arbitration detection status bit.
- **stop_status**: Stop detection status bit. This must be cleared by writing a ‘0’ to this position.
- **ack**: Acknowledge control bit. This bit must be set to ‘1’ to ACK the last byte received or ‘0’ to NAK the last byte received.
- **address**: Set if the byte just received was an address byte.
- **transmit**: Used by firmware to define the direction of a byte transfer.
- **lrb**: Last Received Bit status. This bit indicates the state of the ninth bit (ACK/NAK) response from the receiver for the last byte transmitted.
- byte_complete: Transmit or receive status since last read of this register. In Transmit mode, this bit indicates 8 bits of data plus ACK/NAK have been transmitted since last read. In Receive mode, this bit indicates 8 bits of data have been received since last read of this register.

### I2C_DATA

The data register is available in the fixed-function hardware block for runtime transmit and receipt of data.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- data: In Transmit mode, this register is written with the data to transmit. In Receive mode, this register is read upon status receipt of byte_complete.

### I2C_MCSR

The Master control and status register is available in the fixed-function hardware block for runtime control and status feedback of Master mode operations.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>RSVD</td>
<td>stop_gen*</td>
<td>bus_busy</td>
<td>master_mode</td>
<td>restart_gen</td>
<td>start_gen</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- stop_gen*: If set, a stop is generated in master transmitter mode at the end of a byte transfer.
- bus_busy: Indicates bus status. 0 means a stop condition was detected, 1 indicates a start condition was detected.
- master_mode: Indicates that a valid start condition was generated and a hardware device is operating as bus master.
- restart_gen: Control registers to create a restart condition on the bus. This bit is cleared by hardware after the restart has been implemented (may be read as status after setting to poll for completion of the condition).
- start_gen: Control registers to create a start condition on the bus. This bit is cleared by hardware after the start has been implemented (may be read as status after setting to poll for completion of the condition).
**UDB Master**

The UDB register definitions are derived from the Verilog implementation of \( \text{I}^2\text{C} \). Refer to the specific mode implementation Verilog for more information on these registers definitions.

**I2C_CFG**

The control register is available in the UDB implementation for runtime control of the hardware.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>start_gen</td>
<td>stop_gen</td>
<td>restart_gen</td>
<td>ack</td>
<td>RSVD</td>
<td>transmit</td>
<td>en_master</td>
<td>RSVD</td>
</tr>
</tbody>
</table>

- **start_gen**: Set to 1 to generate a start condition on the bus. This bit must be cleared by firmware before initiating the next transaction.
- **stop_gen**: Set to 1 to generate a stop condition on the bus. This bit must be cleared by firmware before initiating the next transaction.
- **restart_gen**: Set to 1 to generate a restart condition on the bus. This bit must be cleared by firmware after a restart condition is generated.
- **ack**: Set to 1 to NAK the next read byte. Clear to ACK next read byte. This bit must be cleared by firmware between bytes.
- **transmit**: Set to 1 to set the current mode to transmit or clear to 0 to receive a byte of data. This bit must be cleared by firmware before starting the next transmit or receive transaction.
- **en_master**: Set to 1 to enable the master functionality.

**I2C_CSR**

The status register is available in the UDB implementation for runtime status feedback from the hardware. The status data is registered at the input clock edge of the counter for all bits configured with mode = 1. These bits are sticky and are cleared on a read of the status register. All other bits are configured as mode = 0 read directly from the inputs to the status register. They are not sticky and therefore not cleared on read. All bits configured as mode = 1 are indicated with an asterisk (*) in the definitions listed below.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>RSVD</td>
<td>lost_arb*</td>
<td>stop_status*</td>
<td>bus_busy</td>
<td>address</td>
<td>master_mode</td>
<td>lrb</td>
<td>byte_complete</td>
</tr>
</tbody>
</table>

- **lost_arb**: If set, indicates arbitration was lost (Multi-Master and Multi-Master-Slave modes).
- **stop_status**: If set, indicates a stop condition was detected on the bus.
- **bus_busy**: If set, indicates the bus is busy. Data is currently being transmitted or received.
- **address**: Address detection. If set, indicates that an address byte was sent.
- **master_mode**: Indicates that a valid start condition was generated and a hardware device is operating as bus master.

- **lbr**: Last Received Bit. Indicates the state of the last received bit, which is the ACK/NAK received for the last byte transmitted. Cleared = ACK and set = NAK.

- **byte_complete**: Transmit or receive status since last read of this register. In Transmit mode this bit indicates 8 bits of data plus ACK/NAK have been transmitted since last read. In Receive mode this bit indicates 8 bits of data have been received since last read of this register.

### I2C_INT_MASK

The Interrupt mask register is available in the UDB implementation to configure which status bits are enabled as interrupt sources. Any of the status register bits may be enabled as in interrupt source with a one-to-one bit correlation to the status registers bit-field definitions in I2C_CSR above.

### I2C_ADDRESS

The slave address register is available in the UDB implementation to configure the slave device address for hardware comparison mode.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>RSVD</td>
<td>slave_address</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **slave_address**: Used to define the 7-bit slave address for hardware address comparison mode

### I2C_DATA

The data register is available in the UDB implementation block for runtime transmit and receipt of data.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td></td>
<td>data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **data**: In Transmit mode this register is written with the data to transmit. In Receive mode this register is read upon status receipt of byte_complete.

### I2C_GO

The Go register forces data in the data register to be transmitted when master transmits. The Go register forces data to be received in data register when master receives. Any write to this register forces this action, no matter which value is written.
UDB Slave

The UDB register definitions are derived from the Verilog implementation of I²C. Refer to the specific mode implementation Verilog for more information on these registers definitions.

I2C_CFG

The control register is available in the UDB implementation for runtime control of the hardware.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>nak</td>
<td>any_address</td>
<td>transmit</td>
<td>RSVD</td>
<td>en_slave</td>
</tr>
</tbody>
</table>

- nak: If set, used to NAK the last byte received. This bit must be cleared by firmware between bytes.
- any_address: If set, used to enable the device to respond any device addresses it receives rather than just the single address provided in I2C_ADDRESS.
- transmit: Used to set the mode to transmit or receive data. This bit must be cleared by firmware between bytes. Set = transmit. Cleared = receive.
- en_slave: Set to 1 to enable the slave functionality.

I2C_CSR

The status register is available in the UDB implementation for runtime status feedback from the hardware. The status data is registered at the input clock edge of the counter for all bits configured with mode = 1. These bits are sticky and are cleared on a read of the status register. All other bits are configured as mode = 0 and read directly from the inputs to the status register. They are not sticky and therefore not cleared on read. All bits configured as mode = 1 are indicated with an asterisk (*) in the definitions listed below.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>RSVD</td>
<td>RSVD</td>
<td>stop*</td>
<td>RSVD</td>
<td>address</td>
<td>RSVD</td>
<td>lrb</td>
<td>byte_complete</td>
</tr>
</tbody>
</table>

- stop*: If set, indicates a stop condition was detected on the bus.
- address: Address detection. If set, indicates that an address byte was received.
- lrb: Last Received Bit. Indicates the state of the last received bit which is the ACK/NAK received for the last byte transmitted. Cleared = ACK and set = NAK.
- byte_complete: Transmit or receive status since last read of this register. In Transmit mode this bit indicates 8 bits of data plus ACK/NAK have been transmitted since last read. In Receive mode this bit indicates 8 bits of data have been received since last read of this register.
I2C_INT_MASK
The Interrupt mask register is available in the UDB implementation to configure which status bits are enabled as interrupt sources. Any of the status register bits may be enabled as in interrupt source with a one-to-one bit correlation to the status register bit-field definitions in the I2C_CSR register. Two interrupt sources are used during operation: byte_complete and stop.

I2C_ADDRESS
The slave address register is available in the UDB implementation to configure the slave device address for hardware comparison mode.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>RSVD</td>
<td>slave_address</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- slave_address: Used to define the 7-bit slave address for hardware address comparison mode

I2C_DATA
The data register is available in the UDB implementation block for runtime transmit and receipt of data.

<table>
<thead>
<tr>
<th>Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td></td>
<td>data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- data: In Transmit mode this register is written with the data to transmit. In Receive mode this register is read upon status receipt of byte_complete.

I2C.GO
The Go register forces data in the data register to be transmitted when master transmits. The Go register forces the data register to receive data when master receives. Any write to this register forces this action, no matter which value is written.

DC and AC Electrical Characteristics (FF Implementation)
The following values indicate expected performance and are based on initial characterization data.
I²C DC Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block current consumption</td>
<td>Enabled, configured for 100 kbps</td>
<td>--</td>
<td>--</td>
<td>250</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enabled, configured for 400 kbps</td>
<td>--</td>
<td>--</td>
<td>260</td>
<td>µA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wake from sleep mode</td>
<td>--</td>
<td>--</td>
<td>30</td>
<td>µA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

I²C AC Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit rate</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>Mbps</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DC and AC Electrical Characteristics (UDB Implementation)

The following values indicate expected performance and are based on initial characterization data.

Timing Characteristics “Maximum with All Routing”

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{SCL}$</td>
<td>SCL clock frequency</td>
<td>--</td>
<td>100</td>
<td>--</td>
<td>kHz</td>
</tr>
<tr>
<td>Standard mode</td>
<td>--</td>
<td>--</td>
<td>$16 \times f_{SCL}$</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Fast mode</td>
<td>--</td>
<td>400</td>
<td>--</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Fast mode plus</td>
<td>--</td>
<td>1000</td>
<td>--</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>$f_{CLOCK}$</td>
<td>Component input clock frequency</td>
<td>--</td>
<td>16</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>$t_{LOW}$</td>
<td>Low period of the SCL clock</td>
<td>--</td>
<td>8</td>
<td>$t_{CY _clock}$</td>
<td></td>
</tr>
<tr>
<td>$t_{HIGH}$</td>
<td>High period of the SCL clock</td>
<td>--</td>
<td>8</td>
<td>$t_{CY _clock}$</td>
<td></td>
</tr>
<tr>
<td>$t_{HD _STA}$</td>
<td>Hold time (repeated) start condition</td>
<td>--</td>
<td>15</td>
<td>$t_{CY _clock}$</td>
<td></td>
</tr>
<tr>
<td>$t_{SU _STA}$</td>
<td>Setup time for a repeated start condition</td>
<td>--</td>
<td>9</td>
<td>$t_{CY _clock}$</td>
<td></td>
</tr>
<tr>
<td>$t_{HD _DAT}$</td>
<td>Data hold time</td>
<td>--</td>
<td>1</td>
<td>$t_{CY _clock}$</td>
<td></td>
</tr>
<tr>
<td>$t_{SU _DAT}$</td>
<td>Data setup time</td>
<td>--</td>
<td>7</td>
<td>$t_{CY _clock}$</td>
<td></td>
</tr>
<tr>
<td>$t_{SU _STO}$</td>
<td>Setup time for stop condition</td>
<td>--</td>
<td>9</td>
<td>$t_{CY _clock}$</td>
<td></td>
</tr>
<tr>
<td>$t_{BUF}$</td>
<td>Bus free time between a stop and start condition</td>
<td>--</td>
<td>32</td>
<td>$t_{CY _clock}$</td>
<td></td>
</tr>
<tr>
<td>$t_{RESET}$</td>
<td>Reset pulse width</td>
<td>--</td>
<td>2</td>
<td>$t_{CY _clock}$</td>
<td></td>
</tr>
</tbody>
</table>

$5 t_{CY \_clock} = 1/f_{CLOCK}$. This is the cycle time of one clock period
How to Use STA Results for Characteristics Data

Nominal route maximums are gathered through multiple test passes with Static Timing Analysis (STA). The maximums may be calculated for your designs using the STA results with the following mechanisms.

**f\text{CLOCK}**  
Maximum Component Clock Frequency is provided in Timing results in the clock summary as the named component clock (CLK in this case). The maximum component clock is limited to \( f_{\text{CLOCK}} = 16 \times f_{\text{SCL}} = 16 \times 1000 \text{ kHz} = 16 \text{ MHz} \), so STA report must be used only to check that the reported maximum clock frequency (Max Freq) is not violated. An example of the component clock limitations from the _timing.html file is below:

<table>
<thead>
<tr>
<th>Clock</th>
<th>Actual Freq</th>
<th>Max Freq</th>
<th>Violation</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUS_CLK</td>
<td>48.000 MHz</td>
<td>112.664 MHz</td>
<td></td>
</tr>
<tr>
<td>(Clock</td>
<td>16.000 MHz</td>
<td>20.571 MHz)</td>
<td></td>
</tr>
</tbody>
</table>

The rest of the parameters are implementation specific and are measured in clock cycles. The I^2C component is compatible with I^2C-bus specification Rev. 3 from June 2007.

**t_{\text{SCL}}**  
Defines the I^2C data rate value up to 1000 kbps; The standard data rates are 50, 100, 400, and 1000 kbps. The 16x input clock is required to get a needed data rate.

**t_{\text{LOW}}**  
Low period of the SCL clock. The component generates 50-percent duty clock cycle.

**t_{\text{HIGH}}**  
High period of the SCL clock. The component generates 50-percent duty clock cycle.

**t_{\text{HD_STA}}**  
The minimum amount of time the SCL signal is high after a high-to-low transition of SDA to generate the start condition. After this period, the first clock pulse is generated.

**t_{\text{SU_STA}}**  
The minimum amount of time the SCL signal is high before a high-to-low transition of SDA to generate the start condition.
**t\textsubscript{HD\_DAT}** The minimum amount of time the data should be valid after the falling edge of the SCL signal.

**t\textsubscript{SU\_DAT}** The minimum amount of time the data should be valid before the rising edge of the SCL signal.

**t\textsubscript{SU\_STO}** The minimum amount of time the SCL should be high before a low-to-high transition of the SDA signal to generate the stop condition.

**t\textsubscript{BUF}** The period of time the bus is considered to be free after the stop condition.

**t\textsubscript{RESET}** The component implementation requires two cycles width of the reset signal.

---

**Component Changes**

This section lists the major changes in the component from the previous version.

<table>
<thead>
<tr>
<th>Version</th>
<th>Description of Changes</th>
<th>Reason for Changes / Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0</td>
<td>Minor datasheet edits and updates</td>
<td></td>
</tr>
<tr>
<td>3.0.a</td>
<td>Minor datasheet edits and updates</td>
<td></td>
</tr>
<tr>
<td>3.0</td>
<td>Changed customizer appearance</td>
<td>Looks much more intuitive and easy to use.</td>
</tr>
<tr>
<td>3.0</td>
<td>Added the UDB clock tolerance setting.</td>
<td>Avoids the appearance of clock warning for many configurations.</td>
</tr>
<tr>
<td>3.0</td>
<td>The component in FF implantation with Enable from Sleep option restores configuration correctly after exit hibernate.</td>
<td>Fix component behavior in hibernate mode.</td>
</tr>
<tr>
<td>3.0</td>
<td>The I\textsuperscript{2}C interrupt is enabled after I2C_Start() is called.</td>
<td>No errors appear when the user forgets to enable interrupt after I2C_Start() in Slave mode.</td>
</tr>
<tr>
<td>3.0</td>
<td>Added support of internal clock for UDB implementation.</td>
<td>Functionality enhancement.</td>
</tr>
<tr>
<td>3.0</td>
<td>Removed functions SlaveGetWriteByte() and SlavePutReadByte()</td>
<td>These functions are not usable.</td>
</tr>
<tr>
<td>2.20</td>
<td>Add bootloader communication support to UDB-based implementation of component.</td>
<td>Allows more than one I\textsuperscript{2}C component that supports bootloading to be present in the design. This can be used with the custom bootloader feature included with cy_boot v2.21.</td>
</tr>
<tr>
<td>2.20</td>
<td>Fixed misplaced start condition detection while transaction due zero data hold time.</td>
<td>Slave operates correctly with zero data hold time from master.</td>
</tr>
<tr>
<td>2.10</td>
<td>Add Multi-Master-Slave mode</td>
<td>The support of Multi-Master-Slave functionality is added to component.</td>
</tr>
<tr>
<td>2.10</td>
<td>Customizer labels and description edits</td>
<td>Improve feel and content of component customizer.</td>
</tr>
<tr>
<td>Version</td>
<td>Description of Changes</td>
<td>Reason for Changes / Impact</td>
</tr>
<tr>
<td>---------</td>
<td>----------------------------------------------------------------------------------------</td>
<td>-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td></td>
<td>I²C bootloader communication component behavior was changed to suppress clock stretching on read.</td>
<td>I²C bootloader communication component holds SCL Low forever if read command issued before start boot process.</td>
</tr>
<tr>
<td></td>
<td>Added characterization data to datasheet.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Minor datasheet edits and updates</td>
<td></td>
</tr>
<tr>
<td>2.0.a</td>
<td>Moved component into subfolders of the component catalog</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Minor datasheet edits and updates</td>
<td></td>
</tr>
<tr>
<td>2.0</td>
<td>Added Sleep/Wakeup and Init/Enable APIs.</td>
<td>To support low power modes, as well as to provide common interfaces to separate control of initialization and enabling of most components.</td>
</tr>
<tr>
<td></td>
<td>Component was updated to support Production PSoC 3 and above. Updated the Configure dialog:</td>
<td>New requirement to support the Production PSoC 3 device, thus a new 2.0 version was created. Version 1.xx supports PSoC 3 ES2 and PSoC 5 silicon revisions.</td>
</tr>
<tr>
<td></td>
<td>Added configuration of I2C pins connection port for the wakeup on I²C address match feature.</td>
<td>The I²C component will be able to wake up the device from Sleep mode on I²C address match.</td>
</tr>
<tr>
<td></td>
<td>Datasheet was updated.</td>
<td>The Parameters and Setup, Clock Selection, and Resources sections have been updated to reflect the UDB Implementation. Error in sample code has been fixed.</td>
</tr>
<tr>
<td></td>
<td>Add Reentrancy support to the component.</td>
<td>Allows users to make specific APIs reentrant if reentrancy is desired.</td>
</tr>
</tbody>
</table>

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