Asynchronous SRAM With ECC Solution Examples

ECC = Error-Correcting Code

High-Speed and Low-Power Asynchronous SRAMs With On-Chip ECC to Improve System Reliability

MoBL®[1] SRAM With ECC[2] Solution Example – Multi-Function Printer (MFP)

MoBL SRAM With ECC Value

Design Challenges

Write configuration and status data at access times of 45 ns
Retain the data with battery back-up on power loss
Provide error detection and correction to ensure data reliability

MoBL SRAM With ECC Solution

Provides SRAM memory with 45-ns access time
Provides 1-µA/Mb standby current for long battery life
Provides on-chip ECC with a FIT[3] rate of <0.1 FIT/Mb

Suggested Collateral

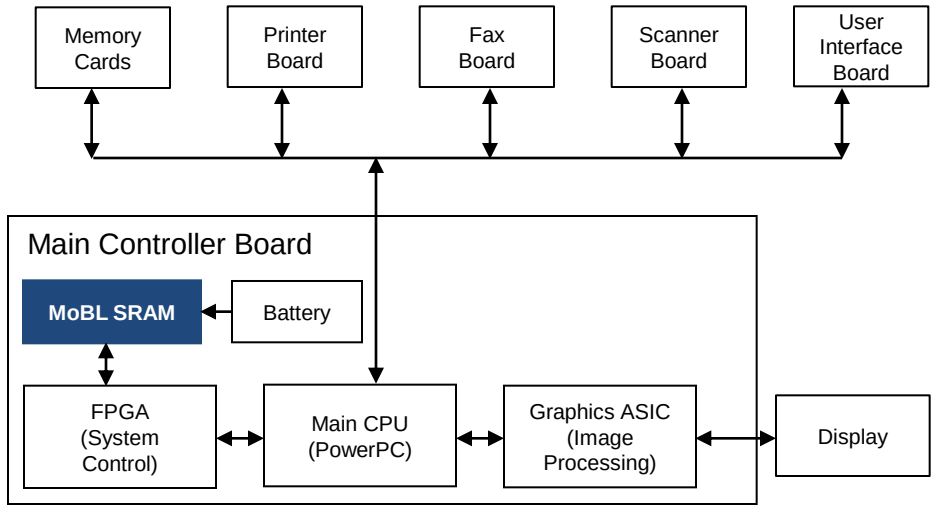
Application Notes:	MoBL SRAM application notes
Knowledge Base Articles:	MoBL SRAM articles
Datasheets:	MoBL SRAM datasheets

Discovery Questions

How do you retain the MFP's configuration and status data on power loss?
How important is memory power consumption for your system?
Is system reliability and soft-error[4] mitigation a critical concern?

Block Diagram

MoBL SRAM With ECC Solution for Multi-Function Printer



Multi-Function Printer By Canon

Incorporates multiple functions (email, fax, photocopier, printer and scanner)

[1] Low-power Asynchronous SRAMs with less than 1-µA/Mb standby current
[2] Encoding and decoding of a bit stream using extra bits to detect and correct bit errors
[3] Failure in Time: A reliability measurement of the projected failure rate of a device. One FIT equals one projected failure per billion device-hours
[4] A data error caused by background radiation

Fast[1] SRAM With ECC[2] Solution Example – Programmable Logic Controller

Fast SRAM With ECC Value

Design Challenges

Write real-time data at access times as fast as 10 ns
Provide error detection and correction to ensure data reliability
Require a reliable and cost-effective memory solution

Fast SRAM With ECC Solution

Provides 10-ns access time
Provides on-chip ECC with a FIT[3] rate of <0.1 FIT/Mb
Provides on-chip ECC, reducing board space and cost

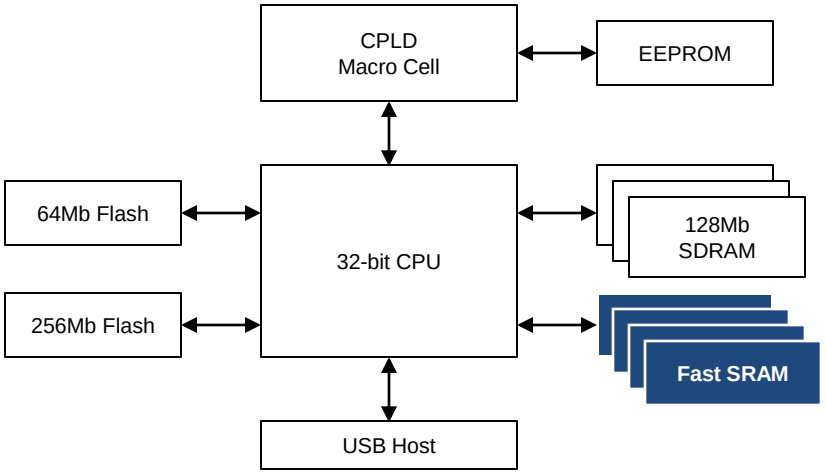
Suggested Collateral

Application Notes:	Fast SRAM application notes
Knowledge Base Articles:	Fast SRAM articles
Datasheets:	Fast SRAM datasheets

Discovery Questions

What memory solution are you using for program execution?
How important is memory access time for your system?
Are system reliability and soft-error[4] mitigation a critical concern?

Block Diagram



Programmable Logic Controller
By Siemens

[1] High-speed Asynchronous SRAMs with access times ≤20 ns
[2] Encoding and decoding of a bit stream using extra bits to detect and correct bit errors
[3] A reliability measurement of the projected failure rate of a device. One FIT equals one projected failure per billion device-hours
[4] A data error caused by background radiation