Enhanced 8-Bit PWM Dead Band Datasheet PWMDB8L V 1.10

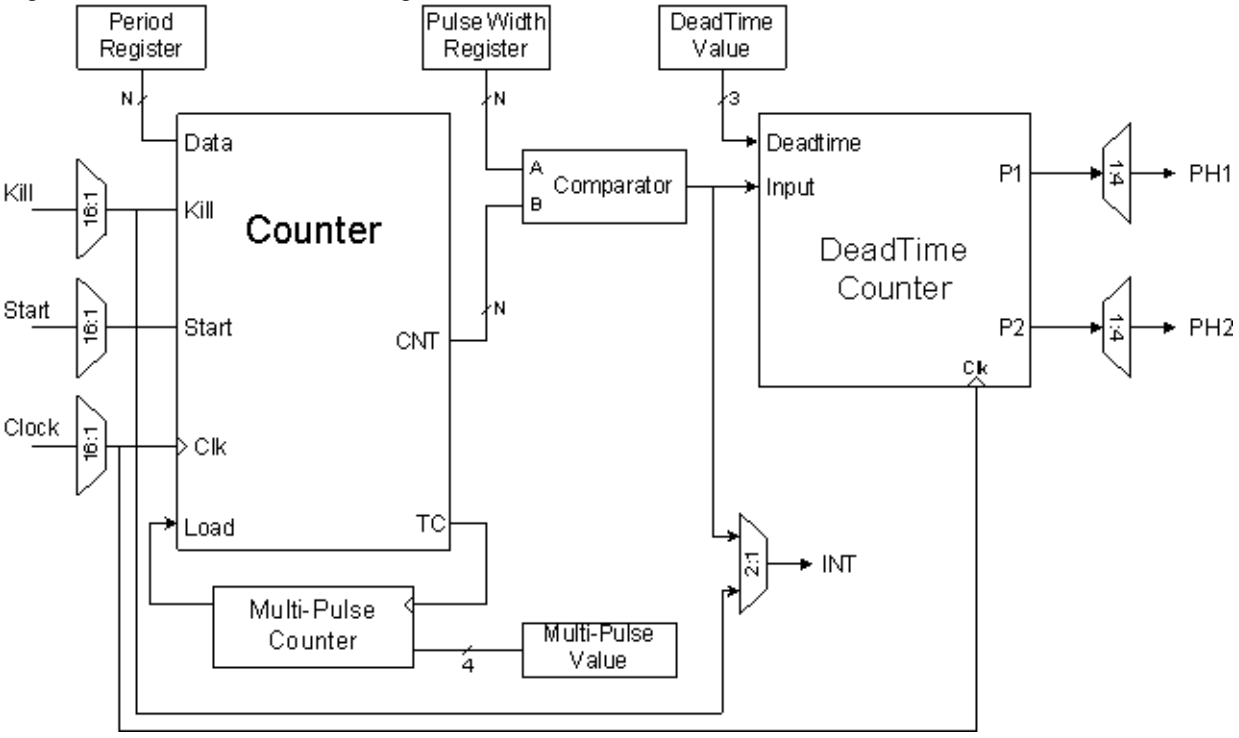
Resources	PSoC® Blocks			API Memory (Bytes)		Pins (per External I/O)
	Digital	Analog CT	Analog SC	Flash	RAM	
CY8C21x45, CY8C22x45, CY8C28xxx, CY8CTMA140, CY8CTMA30xx						
8-bit	1	0	0	107	0	2

Features and Overview

- 8-bit general purpose pulse width modulator (PWM) with 8-bit dead band generator, occupies one PSoC block
- Combines the counter and deadband functions in one digital block with limited deadband width selection
- Phase1 (PH1) and Phase2 (PH2) under-lapped outputs track the frequency of the generated PWM signal
- Programmable duty cycle
- Programmable dead time
- Dead Band Kill input drives Phase1 (PH1) and Phase2 (PH2) outputs low
- Has one-shot/multi-shot feature
- Counter clocking up to 48 MHz
- Interrupt option triggered on rising edge of the PWM Phase1 signal or Kill input

The Enhanced 8-Bit PWM Dead Band User Module (PWMDB8L) is an enhanced version of the PWM8 User Module that supports the deadband in one digital block. It has improved features like one-shot or multi-shot. The pulse width modulator gives a programmable period and pulse width input signal to the dead band generator. The dead band generator outputs two underlapped signals, with programmable dead time at the same frequency as the input signal. When asserted, the Dead Band Kill input will drive the Phase1 and Phase2 output signals low. The clock and enable signals can be selected from several sources. The Phase1 and Phase2 output signals can be routed to the external pin ports or to the global output buses for internal use by other user modules. An interrupt can be programmed to effectively trigger on the rising edge of the PWM Phase1 signal or Kill input of the PWM module.

Figure 1. PWMDB8L Block Diagram



Functional Description

The PWMDB8L User Module employs one digital PSoC block and consists of a period register, a synchronous down counter, a pulse width register, and a deadtime counter.

The PWMDB8L implements a pulse width modulator with programmable period and pulse width. The pulse width modulated output signal is fed into the deadband generator with programmable dead time. The two output signals, Phase1 and Phase2, give the PWMDB8L outputs.

The Control registers start and stop the PWMDB8L. Writing the Period register while stopped, causes the new Period register value to be copied to the Counter register. Writing the DeadTime bits of the Control1 register while stopped, causes the new DeadTime value to be loaded. While the PWMDB8L is stopped the Phase1 and Phase2 outputs are asserted low.

The PWMDB8L is gated by an active high Start signal. While asserted low, the PWMDB8L PSoC block is effectively disabled from operating. Asserting the Start signal continues operation without modifying current register contents.

When started and enabled, PWM decrements the Counter register on each rising edge of the clock. On the clock edge that follows the Counter register's terminal count, the Counter register is reloaded from the Period register. The Period register can be modified with a new period value at anytime. The Period register value is a parameter that may be assigned using the Device Editor or at run time using the API.

The output period of PWM is effectively the period value programmed in the Period register, plus one.

Equation 1

$$\mathrm{OutputPeriod} = \mathrm{PeriodValue} + 1$$

The duty cycle of the generated waveform is defined by the relationship of the period and the pulse width values. The value in the PulseWidth register defines at what count, within the period, the output will be set high. On every clock, PWM compares the values in the Counter and PulseWidth registers. When the count value is “Equal To or Less Than” the period value, the output is set high on the following clock. When the automatic reload of the period occurs, the Counter- and PulseWidth-register comparison fails and the output is set low on the following clock.

The duty cycle can be computed as:

Equation 2

$$DutyCycle = \frac{PulseWidthValue + 1}{PeriodValue + 1}$$

If the period and the pulse width values are equal, the output remains high indefinitely. The pulse width value may have a value from zero to the period value loaded in the Period register. The PulseWidth register value is a parameter that may be set using the Device Editor or at run time using the API.

An interrupt can be programmed to occur on the rising edge of PWM Phase1 signal or Kill input of the PWM module. The interrupt option can be set using the Device Editor. Enabling or disabling interrupts is done at run time with the API.

For each edge of the input signal, the following is repeated:

Rising Edge

- The Phase2 signal is reset low on the rising edge of the next clock cycle.
- The DeadTime value is loaded from the DeadTime bit field of the Control1 register.
- The DeadTime value is decremented on each rising edge of the input clock until it reaches the terminal count. Phase1 is then set high on the next falling edge of the clock.

Falling Edge

- The Phase1 signal is reset low on the rising edge of the following clock cycle.
- The DeadTime value is loaded from the DeadTime bit field of the Control1 register.
- The DeadTime value is decremented on each rising edge of the input clock until it reaches the terminal count. Phase 2 is then set high on the next falling edge of the clock.

Phase1 and Phase2 track the frequency of the input signal received from PWM. Phase1 tracks the duty cycle of the input signal, minus the dead time. Phase2 tracks the inverted cycle of the input signal, minus the dead time.

The effective dead time for each phase of the input signal is:

Equation 3

$$DeadTime = ClockPeriod \times (DeadTime + 1)$$

The DeadTime bits must be loaded with a 3-bit value. So the DeadTime value can be 0, 1, 2, 4, 8, 16, or 32 block clocks in size.

The DeadTime value is a parameter that may be assigned using the Device Editor or at run time using the API.

When asserted high, the Dead Band Kill input will drive the Phase1 and Phase2 outputs low. This signal only affects the output gating of Phase1 and Phase2 signals and not the DeadTime value. When the Dead Band Kill input is released (asserted low), the first applicable phase output may incur a jitter less than the

DeadTime clock counts, but at least one. At this time, the dead band generator will be synced with the pulse width modulated input. This means that the first output pulse will be lengthened.

If the PWMDB output must be be synchronized to the generated PWM input in your application, do the following when the Dead Band Kill input deasserts (repeat the same actions when you detect Dead Band Kill high assertion):

1. Stop the PWMDB8L by calling the Stop() API function.
2. Call the WriteDeadTime() API function to rewrite the Dead Time period.
3. Start the PWMDB8L upon the detection of the Dead Band de-assertion.

Three KILL modes are supported. In all cases, The KILL signal asynchronously forces the outputs to logic '0'. The differences in the modes come from how dead band processing is restarted.

1. **Synchronous Restart Mode**: When KILL is asserted high the internal state is held in reset and the initial dead band period is reloaded into the counter. While KILL is held high, incoming PWM reference edges are ignored. When KILL is negated, the next incoming PWM reference edge restarts dead band processing. See the Synchronous Restart Kill Mode Figure below.
2. **Asynchronous Restart Mode**: When KILL is asserted high the internal state is not affected. When KILL is negated, outputs are restored subject to a minimum disable time between one-half and one and one-half clock cycles. See the Asynchronous Restart Kill Mode Figure.

3. **Disable Mode**: There is no specific timing associated with Disable Mode. The block is disabled and the user must re-enable the function in firmware to continue processing.

Figure 2. Synchronous Restart KILL Mode

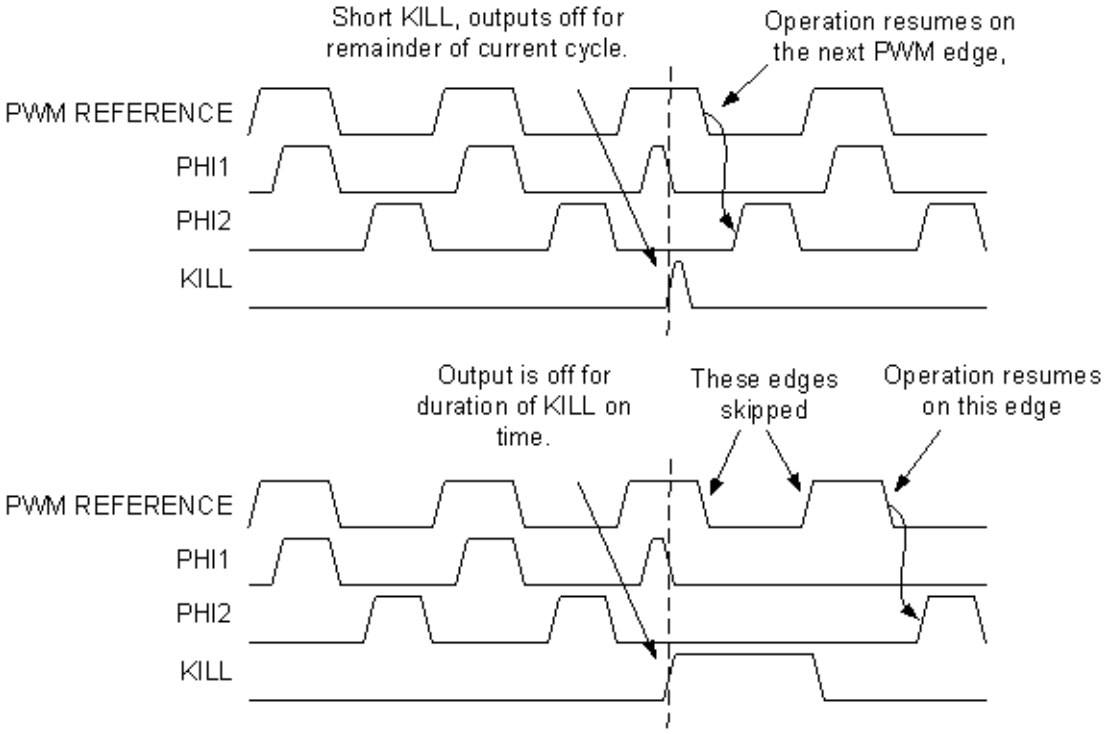
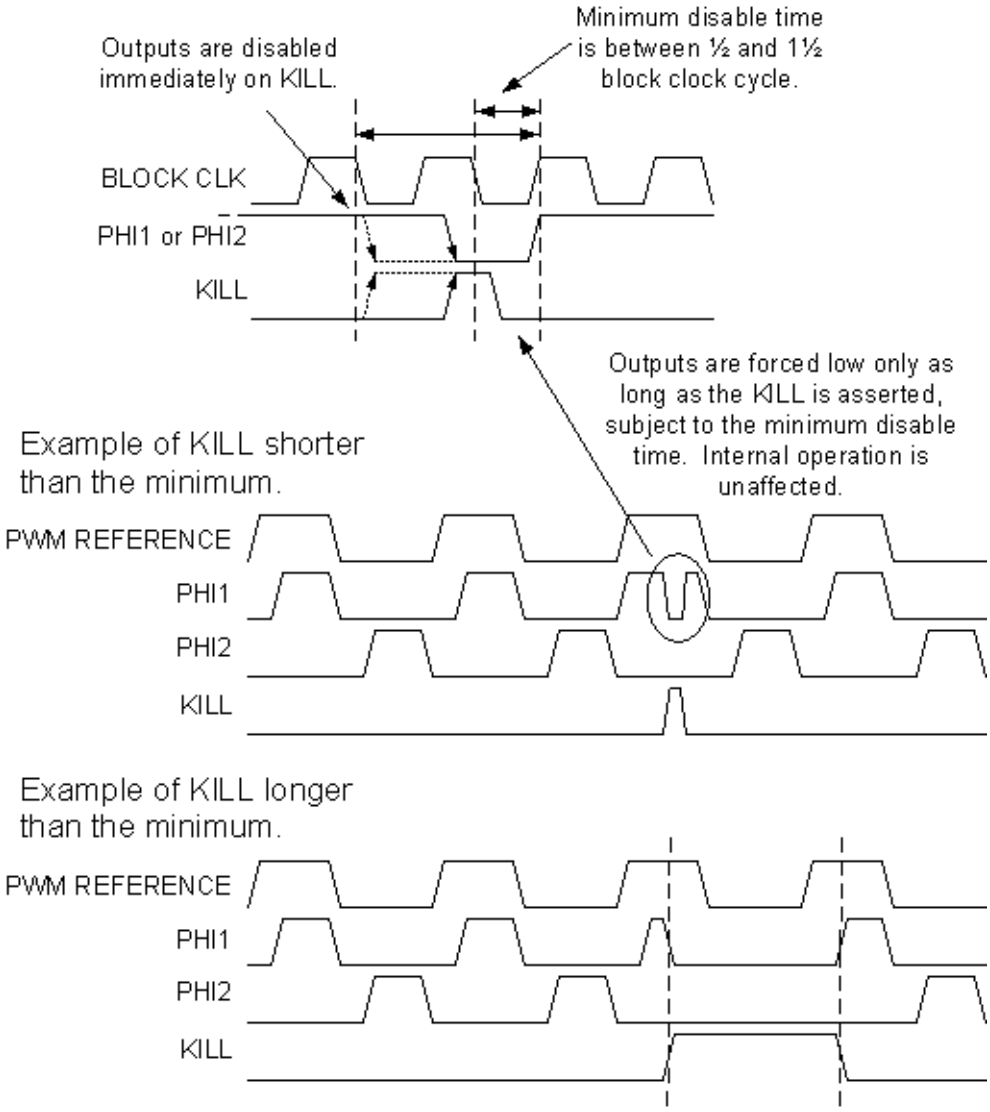


Figure 3. Asynchronous Restart Kill Mode



The PWMDB8L function is identical to the to the Counter function except for the following points:

- There is no counter gate input. Counting down is controlled by different sub modes.
- The multi-shot mode in PWMDB8L is called PPG mode (stands for Programmable Pulse Generator). To start PWMDB8L in the PPG mode the multi-shot register should be set to a non-zero value. The function will not go to disable mode at last-shot. It simply stops counting. Hardware or software start (writing a 1 to the enable bit) resumes counting. The last-shot with START held high will not stop counting. Holding START high will not affect the count.
- The comparison is DR0 > DR2 instead of DR0 <= DR2 or DR0 < DR2. So the compare out waveform is reversed.
- Writing to DR2 is always buffered when the PWMDB8L User Module is running.
- You do not need to set the register as you do in the counter function.
- You can not output the TC. Compare out can not be output directly (it must be output through the deadband function).
- The KILL modes will follow the deadband function setting.
  - SyncRestartKill

  - DisableKill
  - AsyncKill

- KILL will not affect the counter except in the DisableKill mode. The whole function is disabled when KILL is asserted in DisableKill mode.

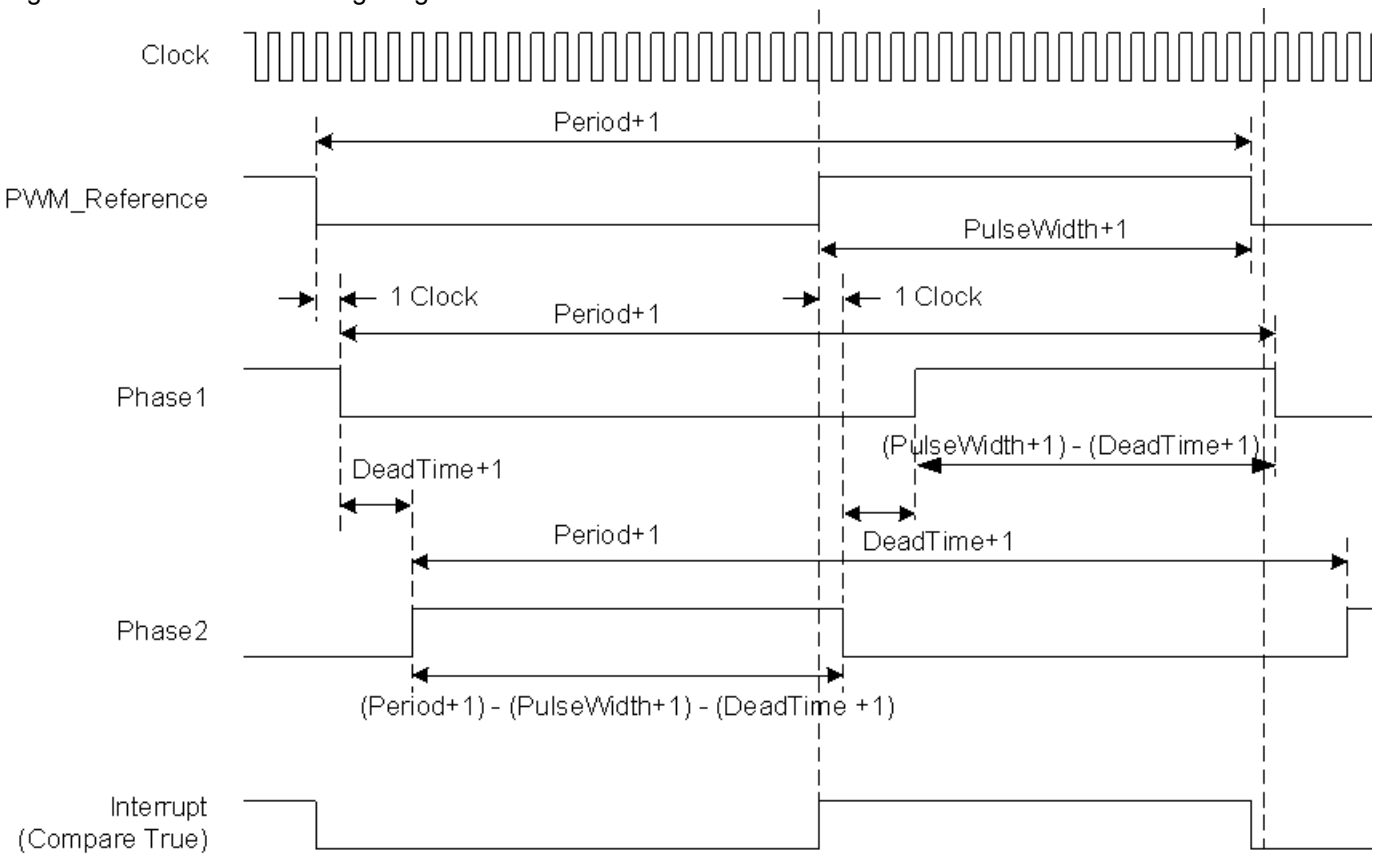
The PWMDB8L deadband function is identical to the DeadBand function except for the following points:

- You do not need to set the reference clock input from the previous block. The reference clock comes from the counter function's compare out in the current block.
- Deadband width selections are limited. The deadband can only be 0, 1, 2, 4, 8, 16, 32, or 64 block clock cycles. Setting the deadband to 0 clock cycles disbables deadband protection.
- The Deadband function uses the block clock. The Counter function runs off of the same clock.
- The user module has an additional interrupt source from the KILL signal.

Timing

PWMDB8L operation may be gated On and Off, or clocked by external pins routed by the global bus feature of the device.

Figure 4. PWMDB8L Timing Diagram



DC and AC Electrical Characteristics

Table 1. PWMDB8L DC and AC Electrical Characteristics

Parameter	Conditions and Notes	Typical	Limit	Units
$FOutput_{max}$	5.0V and 48 MHz input clock	--	24[1]	MHz
	3.3V and 24 MHz input clock	--	12[2]	MHz

Electrical Characteristics Notes

1. If the output is routed through the global buses, then the frequency is constrained to a maximum of 12 MHz.
2. Fastest clock available to PSoC blocks is 24 MHz at 3.3V operation.

Placement

The PWMDB8L User Module occupies an enhanced digital block.

Parameters and Resources

Clock

The PWMDB8L UM is clocked by one of a number of sources. The Global I/O busses may be used to connect the clock input to an external pin or a clock function generated by a different PSoC block. The 48 MHz clock, the CPU_32 kHz clock, one of the divided clocks (24V1 or 24V2), or another PSoC block output can be specified as the clock input. When using an external digital clock for the block, the row input synchronization should be turned off for best accuracy, and sleep operation.

Start

The Start parameter selects a Start signal source from a number of sources. A high signal input enables continuous counting in the digital block, while a low signal input disables counting without resetting the counter. The output is not affected by the state of the input signal. For example, if the output is high when the signal is de-asserted, the output remains in a high state.

This signal selection parameter is equivalent to the Enable signal selection parameter of many other user modules that occupy digital blocks. The Start signal can be thought of as an Enable signal of the block. This Start parameter should not be confused with the Start API function, which is used to start the user module operation in application code.

InvertStart

This parameter allows you to invert the incoming Start signal.

Period

This parameter sets the period of the PWM counter. The 8-bit PWM allows you to select values between 0 and 255. The period is loaded into the Period register. The effective period of the PWM is the period count + 1. You can modify the value at run time using the API.

PulseWidth

This parameter sets the pulse width of the PWM output. Allowed values are between zero a nd the period value. You can modify the value at run time using the API. Note: Phase2 output is direct. Phase1 output is inverted.

InterruptType

This parameter sets the interrupt trigger type. The interrupt can be set up so that it triggers on the rising edge of the PWM Phase1 signal or Kill input of the PWM module. A separate register independently enables the interrupt.

DeadTime

This parameter is used to control the deadband width. The deadband can be 0, 1, 2, 4, 8, 16, 32, or 64 block clock cycles. Setting the deadband to 0 clock cycles disbables deadband protection.

Phase1

This output parameter may be routed to one of four global output buses.

Phase2

This output parameter may be routed to one of four global output buses.

DeadBandKill

This parameter is selected from one of a number of sources. When it is asserted high, Phase1 and Phase2 outputs are driven low.

InvertDeadBandKill

This parameter allows you to invert the incoming DeadBand Kill signal.

DeadBandKillMode

This parameter is selected from one of three Kill modes, SyncRestartKill, DisableKill, or AsyncKill. See the earlier section on the Dead Band Generator for more information.

ClockSync

This parameter may be used to control clock skew and ensure proper operation when reading and writing PSoC block register values. Appropriate values for this parameter should be determined from the following:

ClockSync value	Description
Sync to SysClk	Use this setting for any 24 MHz (SysClk) derived clock source that is divided by two or more. Examples include VC1, VC2, VC3 (when VC3 is driven by SysClk), 32 kHz, and digital PSoC blocks with SysClk-based sources. Externally generated clock sources should also use this value to ensure that proper synchronization occurs.
Sync to SysClk*2	Use this setting for any 48 MHz (SysClk*2) based clock unless the resulting frequency is 48 MHz (in other words, when the product of all divisors is 1).
SysClk Direct	Use this setting when a 24 MHz (SysClk/1) clock is required. This does not actually perform synchronization but gives low-skew access to the system clock itself. If selected, this option overrides the setting of the Clock parameter, above. It should always be used instead of VC1, VC2, VC3 or Digital Blocks where the net result of all dividers in combination produces a 24 MHz output.
Unsynchronized	Use this setting when the 48 MHz (SysClk*2) input is selected. Use when unsynchronized inputs are required. In general, this use is advisable only when interrupt generation is the sole application of the Counter. This setting is required for blocks that remain active during sleep.

PWMEdgeAlign

When this parameter is set, the compare output will be delayed a half clock cycle. It is used to achieve a higher resolution when the 48 MHz clock is used as the block clock.

Trigger Mode

This parameter is used to control the software trigger enable control bit. When set to Software, the PWM will be triggered only by writing a 1 to Bit[0] of the PWMDB8L_CONTROL0_REG in software. If MultiShot[3:0] is not equal to zero, the PWMDB8L runs in the multi-shot mode. When this parameter is set to Hardware, the PWM module will be triggered only by the hardware.

Application Programming Interface

The Application Programming Interface (API) routines are given as part of the user module to allow the designer to deal with the module at a higher level. This section specifies the interface to each function together with related constants given by the include files.

Each time a user module is placed, it is assigned an instance name. By default, PSoC Designer assigns the PWMDB8L_1 to the first instance of this user module in a given project. It can be changed to any unique value that follows the syntactic rules for identifiers. The assigned instance name becomes the prefix of every global function name, variable, and constant symbol. In the following descriptions the instance name has been shortened to PWMDB8L for simplicity.

Note

** In this, as in all user module APIs, the values of the A and X register may be altered by calling an API function. It is the responsibility of the calling function to preserve the values of A and X prior to the call if those values are required after the call. This “registers are volatile” policy was selected for efficiency reasons and has been in force since version 1.0 of PSoC Designer. The C compiler automatically takes care of this requirement. Assembly language programmers must ensure their code observes the policy, too. Though some user module API functions may leave A and X unchanged, there is no guarantee they will do so in the future.

For Large Memory Model devices, it is also the caller's responsibility to preserve any value in the CUR_PP, IDX_PP, MVR_PP, and MVW_PP registers. Even though some of these registers may not be modified now, there is no guarantee that will remain the case in future releases.

PWMDB8L_Start

Description:

Starts both the pulse width modulator and the dead band generator PSoC blocks. The PWM Period register is loaded into the Counter register and the PWMDB8L clock is started. If the input enable is high, the counter will begin to down count.

C Prototype:

```
void PWMDB8L_Start(void);
```

Assembly:

```
lcall PWMDB8L_Start
```

Parameters:

None

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_Stop

Description:

Disables the PWMDB8L PSoC block.

C Prototype:

```
void PWMDB8L_Stop(void);
```

Assembler:

```
lcall PWMDB8L_Stop
```

Parameters:

None

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_EnableInt

Description:

Enables the interrupt mode operation.

C Prototype:

```
void PWMDB8L_EnableInt(void);
```

Assembler:

```
lcall PWMDB8L_EnableInt
```

Parameters:

None

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_DisableInt

Description:

Disables the interrupt mode operation.

C Prototype:

```
void PWMDB8L_DisableInt(void);
```

Assembler:

```
lcall PWMDB8L_DisableInt
```

Parameters:

None

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_WritePeriod

Description:

Writes the PWMDB8L Period register with the period value.

C Prototype:

```
void PWMDB8L_WritePeriod(BYTE bPeriod);
```

Assembler:

```
mov A,[bPeriod]
lcall PWMDB8L_WritePeriod
```

Parameters:

bPeriod value is a value from 0 to 255 and is passed in the Accumulator.

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_WritePulseWidth

Description:

Writes the PWMDB8L PulseWidth register with the pulse width value.

C Prototype:

```
void PWMDB8L_WritePulseWidth(BYTE bPulseWidth);
```

Assembler:

```
mov A,[bPulseWidth]
lcall PWMDB8L_WritePulseWidth
```

Parameters:

bPulseWidth is the pulse width value. Valid values are from zero to the period value. The value is passed in the Accumulator.

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_WriteDeadTime

Description:

Writes the DeadTime bits of the Control1 register with the dead time count value - DeadTime[2:0].

C Prototype:

```
void PWMDB8L_WriteDeadTime(BYTE bDeadTime);
```

Assembler:

```
mov A,[bDeadTime]
lcall PWMDB8L_WriteDeadTime
```

Parameters:

bDeadTime is a value that sets the dead time. Valid values are from 0 to 7. The value is passed in the Accumulator.

Value	Description
0	No deadtime
1	Deadtime is 1 block clock
2	Deadtime is 2 block clock
3	Deadtime is 4 block clock
4	Deadtime is 8 block clock
5	Deadtime is 16 block clock
6	Deadtime is 32 block clock
7	Deadtime is 64 block clock

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_TriggerMultiShot

Description:

Set PWMDB8L Enable bit, or bit[0] in PWMDB8L_CONTROL0_REG.

Note When the multi-shot register is set to non-zero, the PWMDB8L User Module runs into the Programmable Pulse Generator (PPG) mode. It stops output pulse at last shot. Only a hardware and software start (writing 1 again to ‘EN’ bit) can resume the pulse output.

C Prototype:

```
void PWMDB8L_TriggerMultiShot(void);
```

Assembler:

```
lcall PWMDB8L_TriggerMultiShot
```

Parameters:

None

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_SetTrigMode

Description:

Set PWM software trigger mode, SWTrigger, or Bit[1] in PWMDB8L_CONTROL0_REG.

C Prototype:

```
void PWMDB8L_SetTrigMode(BYTE bSWTMode);
```

Assembler:

```
mov A,[bSWTMode]
lcall PWMDB8L_SetTrigMode
```

Parameters:

Symbolic Name	Value	Description
PWMDB8L_TRIGMODE_SOFTWARE_DISABLE	0	Disable software trigger mode
PWMDB8L_TRIGMODE_SOFTWARE_ENABLE	1	Enable software trigger mode

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_SetEdgeAlign

Description:

Sets the PWM edge-alignment mode, NPS, or Bit[3] in PWMDB8L_CONTROL0_REG.

C Prototype:

```
void PWMDB8L_SetEdgeAlign(BYTE bEdgeAlign);
```

Assembler:

```
mov A,[bEdgeAlign]
lcall PWMDB8L_SetEdgeAlign
```

Parameters:

Symbolic name	Value	Description
PWMDB8L_EDGEALIGN_DISABLE	0	Normal mode
PWMDB8L_EDGEALIGN_ENABLE	1	Compare output will be delayed by half clock cycle to be finished. It is used to achieve a higher resolution when a 48 MHz clock is used as a block clock

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_WriteMultiShotCounter

Description:

Writes the PWMDB8L multi-shot counter register with the multi-shot count value - MULTI_SHOT[3:0], or Bit[7:4] in PWMDB8L_CONTROL1_REG.

C Prototype:

```
void PWMDB8L_WriteMultiShotCounter(BYTE bMultiShotCounter);
```

Assembler:

```
mov A,[bMultiShotCounter]
lcall PWMDB8L_WriteMultiShotCounter
```

Parameters:

The multishot counter value is a value from 0 to 15 and is passed in the Accumulator

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_bReadPulseWidth

Description:

Reads the PWMDB8L PulseWidth register.

C Prototype:

```
BYTE PWMDB8L_bReadPulseWidth(void);
```

Assembler:

```
lcall PWMDB8L_bReadPulseWidth
mov [bPulseWidth],A
```

Parameters:

None

Return Value:

The PulseWidth value is stored in the PulseWidth register and returned in the Accumulator.

Side Effects:

See Note** at the beginning of the API section.

PWMDB8L_ClearInt

Description:

Clears pending interrupts for the UM.

C Prototype:

```
void PWMDB8L_ClearInt(void);
```

Assembly:

```
lcall PWMDB8L_ClearInt
```

Parameters:

None

Return Value:

None

Side Effects:

See Note** at the beginning of the API section.

Sample Firmware Source Code

In the following examples, the correspondence between the C and assembly code is simple and direct. The values shown for period and compare value are each "off-by-1" from the cardinal values because the registers are zero-based; i.e., zero is the terminal count in their down-count cycle. Passing a simple one byte parameter in the A register rather than on the stack is a performance optimization used by both the assembler and C compiler for user module APIs. The C compiler employs this mechanism for "INT" types instead of pushing the argument on the stack when it sees the #pragma fastcall declarations in the PWMDB8L.h file.

The following assembly language source code illustrates using APIs:

```
;
;  This sample shows how to generate 20% under-lapped output signals.
;
; OVERVIEW:
;
;  The PWMDB8L output can be routed to any pin.
;  In this example the PWMDB8L outputs is routed to P0[4] and P1[3] pins.
;  The pin P0[4] has the 40% duty cycle output pulse with frequency = 50 kHz.
;  The pin P1[3] has the 40% duty cycle output pulse with frequency = 50 kHz.
;  The second output is shifted to 50% (or 10 usec) relative to first one.
;
;The following changes need to be made to the default settings in the Device Editor:
;
;   1. Select PWMDB8L user module.
;   2. The User Module will occupy the space in dedicated system resources.
;   3. Rename User Module's instance name to PWMDB8L.
```

```
;   4. Set PWMDB8L's Clock Parameter to VC1.
;   5. Set PWMDB8L's Enable Parameter to High.
;   6. Set PWMDB8L's Phase1 Parameter to Row_0_Output_0.
;   7. Set PWMDB8L's DeadBandKill Parameter to Low.
;   8. Set PWMDB8L's ClockSync Parameter to SyncSysClk.
;   9. Set PWMDB8L's Phase2 Parameter to Row_0_Output_3.
;   10. Click on Row_0_Output_0 and connect Row_0_Output_0 to GlobalOutEven_4.
;   11. Select GlobalOutEven_4 for P0[4] in the Pinout.
;   12. Click on Row_0_Output_3 and connect Row_0_Output_3 to GlobalOutOdd_3.
;   13. Select GlobalOutOdd_3 for P1[3] in the Pinout.
;   14. Generate the project (Ctrl + F6).
;
; CONFIGURATION DETAILS:
;
;  1. The clock selected should be 30 times the required period.
;  2. The UM's instance name must be shortened to PWMDB8L.
;
; PROJECT SETTINGS:
;
;     IMO setting (SysClk)  = 24MHz     System clock is set to 24MHz
;     VC1=SysClk/1  = 16 (default)
;
; USER MODULE PARAMETER SETTINGS:
;
;  ------------------------------------------------------------------------------
;  UM         Parameter         Value                Comments
;  ------------------------------------------------------------------------------
;  PWMDB8L    Name              PWMDB8L               UM's instance name
;             Clock             VC1
;             Enable            High
;             Period            0                    The Code changes it.
;             PulseWidth        0                    The Code changes it.
;             InterruptType     Terminal Count
;             PWMOutput         Row_0_Output_1
;             DeadTime          0                    The Code changes it.
;             Phase1            Row_0_Output_0
;             Phase2            Row_0_Output_3
;             DeadBandKill      Low
;             DeadBandKill_Mode SyncRestartKill
;             ClockSync         SyncSysClk
;             InvertDeadBandKill Normal
;             InvertEnable      Normal
;
;  ------------------------------------------------------------------------------

;-------------------------------------------------------------------------
; Assembly code begins here
;-------------------------------------------------------------------------

include "m8c.inc"       ; part specific constants and macros
include "memory.inc"    ; Constants & macros for SMM/LMM and Compiler
include "PSoCAPI.inc"   ; PSoC API definitions for all User Modules

export _main
```

```
PWMDB_PERIOD:     equ 29
PWMDB_PULSEWIDTH: equ 14
PWMDB_DEADTIME:   equ 2

_main:

    ; M8C_EnableGInt             ; Uncomment this line to enable Global Interrupts
    mov   A, PWMDB_PERIOD         ; set the period to be 30 counts of the clock
    lcall PWMDB8L_WritePeriod
    mov   A, PWMDB_PULSEWIDTH     ; set the pulse width to create 50% duty cycle
    lcall PWMDB8L_WritePulseWidth
    mov   A, PWMDB_DEADTIME       ; set the dead time to 20% ->  (15*0.2)-1
    lcall PWMDB8L_WriteDeadTime
    lcall PWMDB8L_Start            ; start the PWMDB8L - counter will start to
                                   ; count when the enable input is asserted high
    ; Insert your main assembly code here.

.terminate:
    jmp .terminate
```

The same code in C is:

```
//
//  This sample shows how to generate 20% under-lapped output signals.
//
// OVERVIEW:
//
//  The PWMDB8L output can be routed to any pin.
//  In this example the PWMDB8L outputs is routed to P0[4] and P1[3] pins.
//  The pin P0[4] has the 40% duty cycle output pulse with frequency = 50 kHz.
//  The pin P1[3] has the 40% duty cycle output pulse with frequency = 50 kHz.
//  The second output is shifted to 50% (or 10 usec) relative to first one.
//
//The following changes need to be made to the default settings in the Device Editor:
//
//   1. Select PWMDB8L user module.
//   2. The User Module will occupy the space in dedicated system resources.
//   3. Rename User Module's instance name to PWMDB8L.
//   4. Set PWMDB8L's Clock Parameter to VC1.
//   5. Set PWMDB8L's Enable Parameter to High.
//   6. Set PWMDB8L's Phase1 Parameter to Row_0_Output_0.
//   7. Set PWMDB8L's DeadBandKill Parameter to Low.
//   8. Set PWMDB8L's ClockSync Parameter to SyncSysClk.
//   9. Set PWMDB8L's Phase2 Parameter to Row_0_Output_3.
//   10. Click on Row_0_Output_0 and connect Row_0_Output_0 to GlobalOutEven_4.
//   11. Select GlobalOutEven_4 for P0[4] in the Pinout.
//   12. Click on Row_0_Output_3 and connect Row_0_Output_3 to GlobalOutOdd_3.
//   13. Select GlobalOutOdd_3 for P1[3] in the Pinout.

//
// CONFIGURATION DETAILS:
//
//  1. The clock selected should be 30 times the required period.
//  2. The UM's instance name must be shortened to PWMDB8L.
//
```

```
// PROJECT SETTINGS:
//
//     IMO setting (SysClk)  = 24MHz     System clock is set to 24MHz
//     VC1=SysClk/1  = 16 (default)
//
// USER MODULE PARAMETER SETTINGS:
//
//  ------------------------------------------------------------------------------
//  UM         Parameter         Value                Comments
//  ------------------------------------------------------------------------------
//  PWMDB8L    Name              PWMDB8L               UM's instance name
//             Clock             VC1
//             Enable            High
//             Period            0                    The Code changes it.
//             PulseWidth        0                    The Code changes it.
//             InterruptType     Terminal Count
//             PWMOutput         Row_0_Output_1
//             DeadTime          0                    The Code changes it.
//             Phase1            Row_0_Output_0
//             Phase2            Row_0_Output_3
//             DeadBandKill      Low
//             DeadBandKill_Mode SyncRestartKill
//             ClockSync         SyncSysClk
//             InvertDeadBandKill Normal
//             InvertEnable      Normal
//
//  ------------------------------------------------------------------------------

/* Code begins here */

#include <m8c.h>        // part specific constants and macros
#include "PSoCAPI.h"    // PSoC API definitions for all User Modules

#define PWM_PERIOD     29
#define PWM_PULSEWIDTH 14
#define PWM_DEATHTIME  2

void main(void)
{
    // M8C_EnableGInt ;              // Uncomment this line to enable Global Interrupts
    PWMDB8L_WritePeriod(PWM_PERIOD);         // Set period to 30 clocks
    PWMDB8L_WritePulseWidth(PWM_PULSEWIDTH); // Set pulse width to generate a 50% duty
    //cycle
    PWMDB8L_WriteDeadTime(PWM_DEATHTIME);     // Set dead time to 20% -> (15*0.2)-1
    PWMDB8L_Start();
    // Insert your main routine code here.
}
```

Configuration Registers

The PWMDB8L User Module is personalized and parameterized through 8 registers. The following tables shows the register values as constants and the parameters as named bit-fields with brief descriptions.Symbolic names for these registers are defined in the user module instance's C and assembly language interface files (the ".h" and ".inc" files).

Table 2. PWMDB8L_FUNC_REG

Bit	7	6	5	4	3	2	1	0
Value	InvertDead BandKill	0	1	DeadBandKillMode[1:0]		0	1	1

InvertDeadBandKill parameter allows the user to invert the incoming DeadBandKill signal. DeadBandKillMode sets one of three Kill modes, SyncRestartKill, DisableKill, or AsyncKill. These parameters can be set by the Device Editor.

Table 3. PWMDB8L_INPUT_REG

Bit	7	6	5	4	3	2	1	0
Value	DeadBandKill[3:0]				Clock [3:0]			

DeadBandKill parameter is selected from one of a number of 16 sources. When it is asserted high, Phase1 and Phase2 outputs are driven low. The user module "DeadBandKill" parameter setting in the Device Editor determines its value. Similarly, the user module "Clock" parameter setting determines the corresponding value.

Table 4. PWMDB8L_OUTPUT_REG

Bit	7	6	5	4	3	2	1	0
Value	ClockSync		1	Phase2[1:0]		1	Phase1[1:0]	

The user module "ClockSync" parameter in the Device Editor determines the value of the ClockSync bits. Phase1 and Phase2 parameters in the Device Editor may be routed to one of four global output buses.

Table 5. PWMDB8L_COUNTER_REG

Bit	7	6	5	4	3	2	1	0
Value	Count							

Count is the PWMDB8L down counter. It can be read using the PWMDB8L API.

Table 6. PWMDB8L_PERIOD_REG

Bit	7	6	5	4	3	2	1	0
Value	Period							

PWMDB8L_PERIOD_REG is the write only register. Period field sets the period of the count. The actual number of clocks counted is Period+1. It can be set in the Device Editor and the PWMDB8L API.

Table 7. PWMDB8L_PULSE_WIDTH_REG

Bit	7	6	5	4	3	2	1	0
Value	PulseWidth							

PWMDB8L_PULSE_WIDTH_REG is a read/write register. It functions as a Compare register. It can be set in the Device Editor and the PWMDB8L API.

Table 8. PWMDB8L_CONTROL0_REG

Bit	7	6	5	4	3	2	1	0
Value	Start[3:0]				PWMEdgeAlign	InterruptType	SWTrigger	Enable

Start[3:0] is the selection of “Start” trigger source input selection, a 16:1 mux from 16 possible digital input source. The InterruptType bit sets the interrupt trigger type. These parameters are set in the Device Editor only. The PWMEdgeAlign bit is the PWM output edge-alignment selection bit. The SWTrigger bit is the software trigger enable bit. These parameters are set in the Device Editor and the PWMDB8L API. Enable indicates that the PWMDB8L is enabled when set and disabled when clear. The register can be modified by using the PWMDB8L API.

Table 9. PWMDB8L_CONTROL1_REG

Bit	7	6	5	4	3	2	1	0
Value	MULTI_SHOT[3:0]				InvertStart	DeadTime[2:0]		

The MULTI_SHOT[3:0] is the multi-shot counter register. It can be modified by using the PWMDB8L API. The InvertStart bit allows the user to invert the incoming DeadBandKill signal. It can be set in the Device Editor. The DeadTime is used for the deadband width control, it could be 0/1/2/4/8/16/32/64 block clock cycles. 0 means there is no deadband protection. It can be set in the Device Editor and the PWMDB8L API.

Version History

Version	Originator	Description
1.0	DHA	Initial version
1.10	HPHA	Corrected method of clearing posted interrupts.

Note PSoC Designer 5.1 introduces a Version History in all user module datasheets. This section documents high level descriptions of the differences between the current and previous user module versions.