AN69091

Edge Align Feature of CY254xx and MoBL® Clocks

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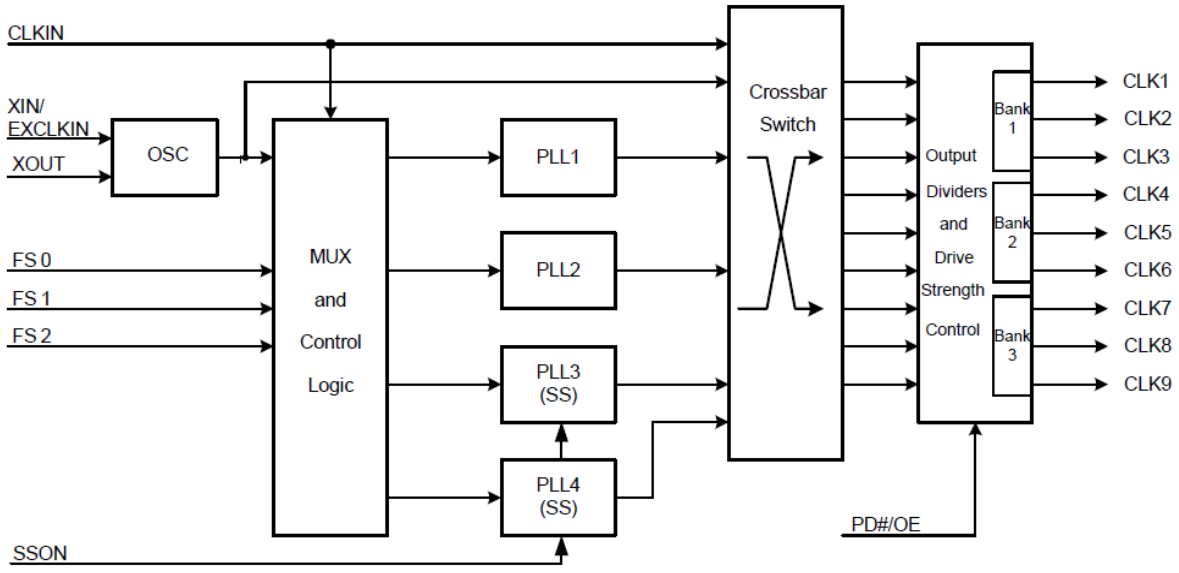
Associated Part Family: CY254x (x: 4/5/6/7/8), CY254xx (xx:04), MoBL® (M3000, M4000, M6000, M8000)
Related Application Notes: AN49107

AN69091 discusses the Edge Align feature in Cypress's programmable clock family, CY254x, CY254xx, and MoBL® clocks. Today's technology products operate at gigahertz (GHz) frequency and therefore need complex clock-tree architecture. This requires clock skew adjustment in the system. To address such applications, Cypress has added the Edge Align feature in CY254x, CY254xx, and MoBL clock family.

1 Introduction

CY254x, CY254xx, and MoBL clocks are multiple-PLL clock generators with a rich set of programmable features, such as spread spectrum, multifunction pins, output drive strength, serial interface, different I/O Voltage, and so on. It supports a maximum of four PLLs with nine CMOS clock outputs. An example logic diagram of one of these IC's is shown in Figure 1. FS0, FS1 and FS2 are frequency select pins whereas SSON pin is for controlling the output clock with Spread Spectrum. For more details of the device, refer to the device datasheet on www.cypress.com. MoBL clocks are optimized version of CY254xx family for low-power applications. Hence, a user can select CY254xx or MoBL devices depending on the power consumption requirement in its application. CY254xx and CY254x are used interchangeably throughout this document.

Figure 1. An Example of Logic Block Diagram of an IC (CY254x)



2 Timing Budget and Clock Skew

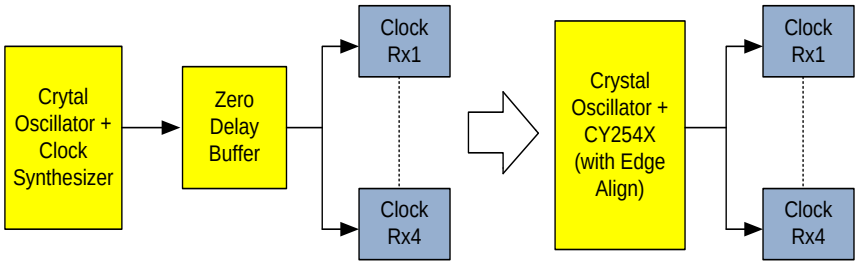
Many electronic systems need a clock to drive FPGA, Transceivers, ASIC, EPROM, I/O control, and so on. For synchronous communication devices an accurate clock is the prime requirement for interoperability at desired speed and throughput. Accuracy of clock is defined by different parameters such as cycle to cycle jitter, period jitter, clock skew, and so on. For proper functionality of the system, all of these parameters should fall within Timing Budget and there should be enough margins for system to operate at optimum speed. Timing Budget considers all possible parameters that can affect system performance. The detailed information about Timing Budget is available in Chapter-III of Perfect Timing-II.

Clock skew is the one of the most important parameter to be considered in Timing Budget. Clock skew is defined as the variation in the arrival time of two clock signals specified to occur at the same time. Skew can be of two types depending upon the arrival of clock signal. It can be advanced or delayed in reference to other clock signal. Clock skew can severely affect the Timing Margin of the system and therefore its speed. Apart from the output to output skew of device, even device to device skew needs to be considered in calculating Timing budget of the system. Normally, less than 10 percent of Timing budget is allotted to skew. To understand different types of skew, please see Chapter-II of Perfect Timing-II. This Application Note focuses on the output to output clock skew.

3 Edge Align Feature

Most of the clock synthesizers available in the market do not support phase-aligned (low-skew) multiple clock outputs. Hence, designers use zero delay buffer (ZDB) with clock synthesizer to get multiple clock copies with low skew. To address this overhead, Cypress has added the Edge Align Feature in multi clock output clock synthesizer family, CY254xx/MoBL clocks.

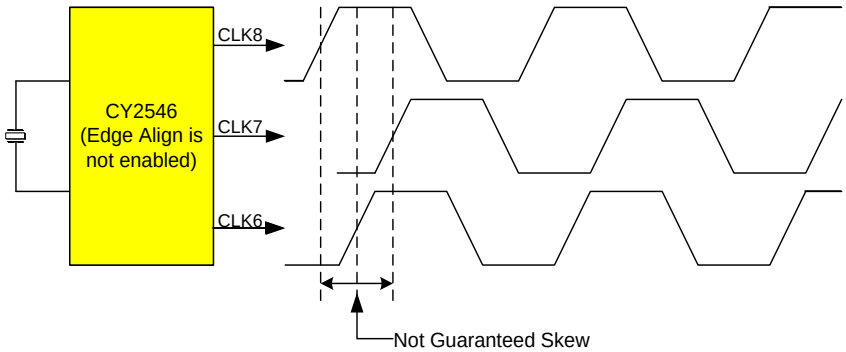
Figure 2. Existing Solution versus CY254XX/MoBL Solution



The Edge Align feature ensures a consistent phase relationship across multiple clock outputs.

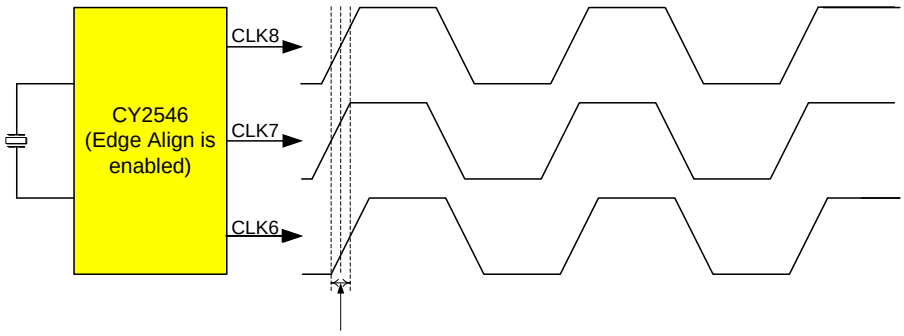
In clock synthesizer, phase relationship between different clock outputs is not guaranteed even though they are derived from the same PLL block. This is because the clock output dividers may not be synchronized. The Edge Align block synchronizes the selected clock output dividers on the rising edge. The outputs may be the same frequency or different frequencies. For the same frequency clock outputs, falling edges will also be aligned.

Figure 3. Same Frequency Clock Outputs When Edge Align is Not Enabled



Alignment indicates basic phase alignment. The output-to-output skew is not zero, and a maximum skew can be as low as 200 ps between certain outputs (outputs from same PLL) measured at the output pins of the device.

Figure 4. Same Frequency Clock Outputs with Edge Align



3.1 Edge Align Feature Access

Cypress provides factory and field programmable option for CY254xx and MoBL clock devices. Factory programmed devices are available in both the configuration, with and without Edge Align feature. Currently only Factory programmed devices support Edge Align Feature. For factory programmed device with Edge Align feature, please contact local Cypress FAE (Field Application Engineer) or create a Technical Support case on www.cypress.com.

See Conditions for the guidelines that must be followed while using Edge Align feature.

3.2 Conditions

To use the Edge Align feature, the following rules must be followed:

- CY254xx/MoBL clock has multiple PLLs, but Edge Align outputs must be driven from the same PLL. Conversely, because there is no synchronization between PLLs, outputs coming from multiple PLLs cannot be Edge-Aligned.
- Each output path has two dividers in series: a pre-scalar and a linear divider. The output frequency is equal to the PLL frequency divided by the output dividers. The PLL frequency range is 100 MHz to 400 MHz.
  - Pre-scalar divider for each aligned output must be set to divide-by-one.
  - Linear divider for each aligned output must be set to divide-by-2, -4, -6, or -12 only.
- Edge Align is not maintained if frequency select (FS) pins are toggled during operation. If the state of any FS pin (see Logic Block Diagram: Figure 1) changes, the device must be powered down and back up to ensure Edge Align.
- Edge Align feature cannot be set through I^2C interface. It has to be pre-programmed at Factory.
- Different output frequencies can be Edge Align, but they must be "related frequencies". Related frequencies are a set of frequencies that are integer multiples of any one of them. For example, a 20-MHz clock, a 40-MHz clock, and a 60-MHz clock are an integer multiple of 20 MHz and they all can be derived from one PLL running at 240 MHz.
- These conditions limit the possible Edge Align configurations for different devices. Sample combination of Edge Align clock outputs are mentioned in Table 1 for different devices. Possible PLL source is mentioned in parenthesis.

Table 1. Sample Combination of Edge Aligned Clock Outputs for CY254xx and MoBL Clocks (*)

Sample Combination of Edge Align Clock Outputs		
For CY2544, CY2546, CY2548, CY25404		
Four Outputs	**Three Outputs**	**Two Outputs**
CLK1-CLK4 (PLL1)	CLK1-CLK3 (PLL1)	CLK1-CLK2 (PLL1, PLL3, PLL4)
CLK5-CLK8 (PLL2)	CLK2-CLK4 (PLL1)	CLK2-CLK3 (PLL1)
CLK6-CLK9 (PLL3, PLL4)	CLK5-CLK7 (PLL2)	CLK3-CLK4 (PLL1)
	CLK6-CLK8 (PLL2, PLL3, PLL4)	CLK5-CLK6 (PLL2)
	CLK7-CLK9 (PLL3, PLL4)	CLK6-CLK7 (PLL2, PLL3, PLL4)
		CLK7-CLK8 (PLL2, PLL3, PLL4)
		CLK8-CLK9 (PLL3, PLL4)
Sample Combination of Edge Align Clock Outputs		
For CY2545, CY2547, M3000, M6000, M4000, M8000		
Four Outputs	**Three Outputs**	**Two Outputs**
CLK4-CLK7 (PLL2)	CLK1-CLK3 (PLL1)	CLK1-CLK2 (PLL1, PLL3, PLL4)
CLK5-CLK8 (PLL3, PLL4)	CLK4-CLK6 (PLL2)	CLK2-CLK3 (PLL1)
	CLK5-CLK7 (PLL2, PLL3, PLL4)	CLK4-CLK5 (PLL2)
	CLK6-CLK8 (PLL3, PLL4)	CLK5-CLK6 (PLL2, PLL3, PLL4)
		CLK6-CLK7 (PLL2, PLL3, PLL4)
		CLK7-CLK8 (PLL3, PLL4)

***Note:** Other combinations of Edge-aligned clock outputs are also possible. Please create a support case on www.cypress.com/support to know the feasibility of edge aligned clock outputs for your set of clock output combination.

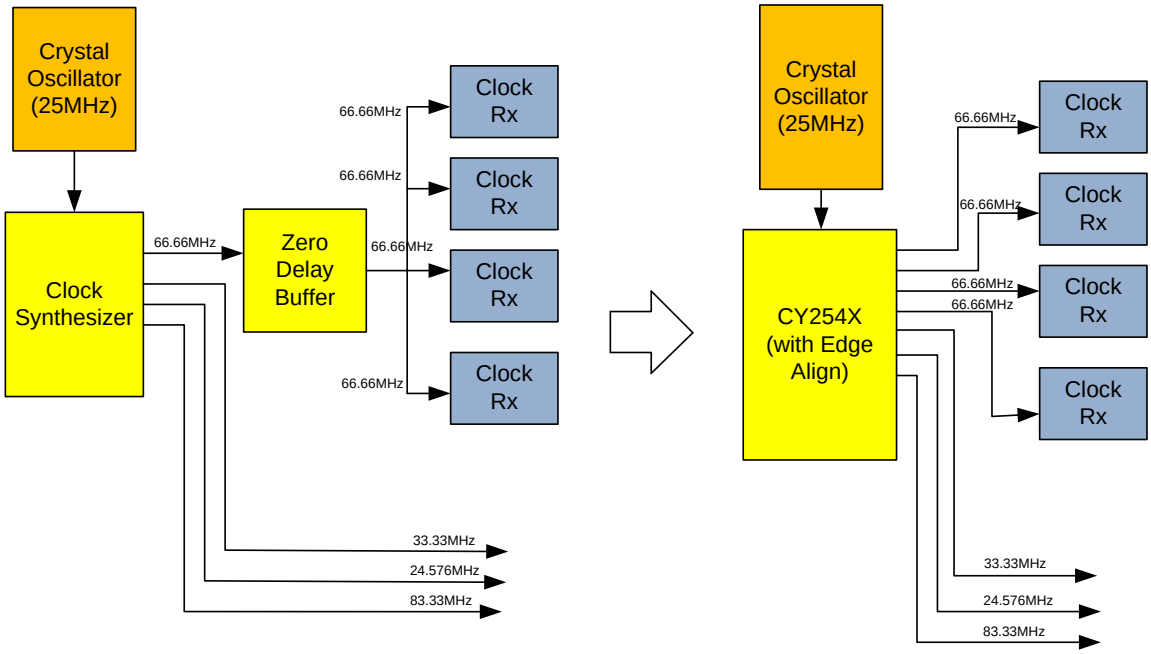
4 Examples and Applications

The Edge Align feature is value-added feature for applications that require low skew between different clocks. Example 1 and Example 2 discuss how the need of extra low skew buffer can be avoided using this feature. To explain the use of CY254x in an Application, CY2545 is used as an example to show Application 1 (Multi-Function Printer) whereas CY2546 is used as an example to show Application 2 (Femtocell). However, they can be used interchangeably in these applications.

4.1 Example 1

To generate four copies of a single-frequency clock output and three other unrelated frequency clock outputs, the designers traditionally use one crystal oscillator and one clock synthesizer with a four-output zero delay buffer as shown in Figure 5. The Edge Align feature of the CY254x/MoBL family enables it to meet this requirement with one crystal oscillator.

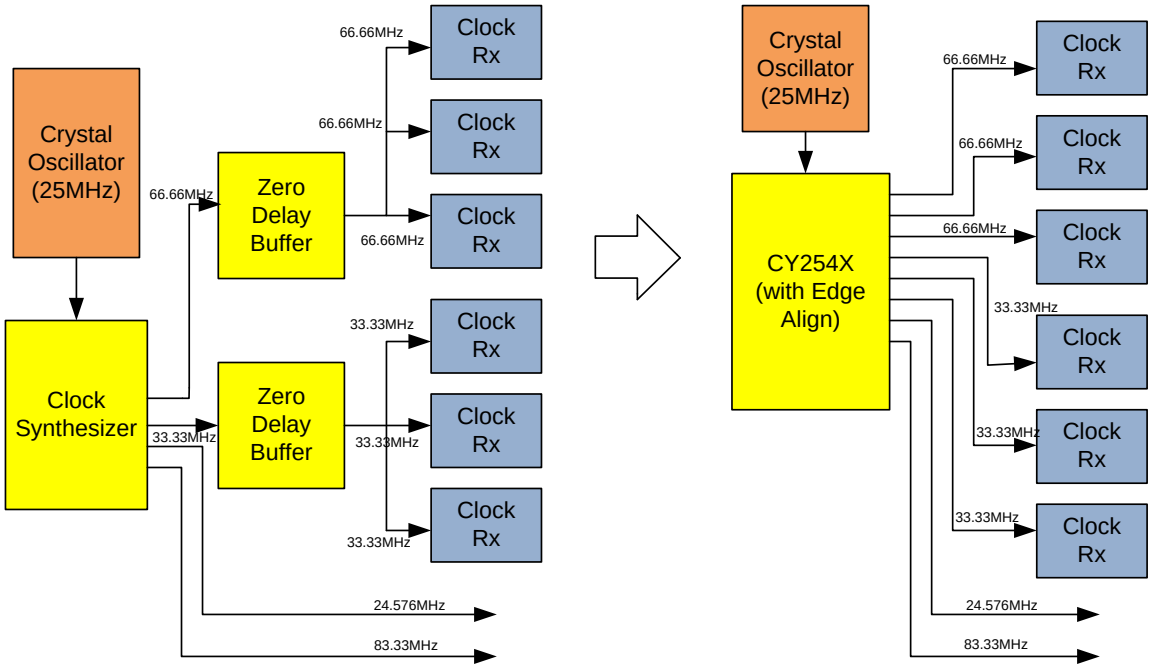
Figure 5. Existing Solution versus CY254x/MoBL Solution



4.2 Example 2

To generate three copies of two different frequencies and two other unrelated frequency clock outputs, the designers traditionally used one crystal oscillator, two ZDBs, and one clock generator as shown in Figure 6. The Edge Align feature of the CY254x/MoBL family enables it to meet this requirement with one crystal oscillator.

Figure 6. Existing Solution versus CY254x/MoBL Solution

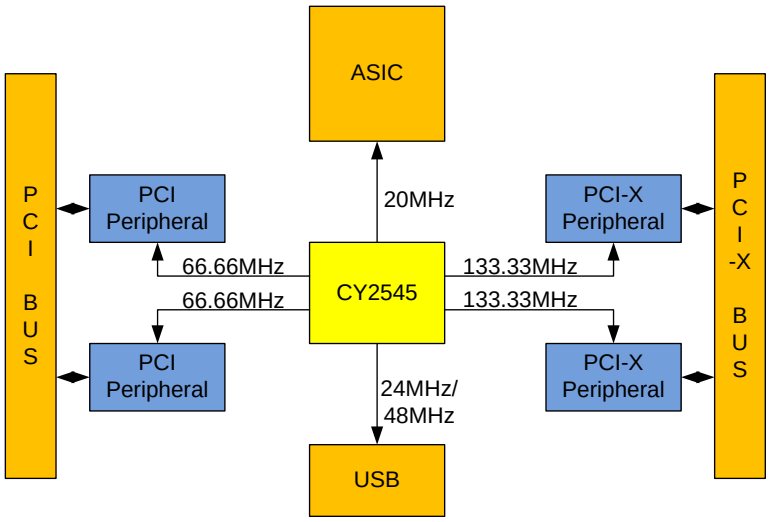


4.3 Application 1

4.3.1 Multi-Function Printer

Today's printer is capable of doing scanning, copying, faxing, and many other tasks along with printing. These features have added more complexity in printer architecture. Modern printers have multiple PCI buses to interface different standard PCI peripherals. Figure 7 gives quick view about two PCI buses and its peripheral with clocking requirement. CY2545 can generate multiple copies of low skew clock for PCI peripherals. Apart from this it can also meet the clocking requirement of other interface like USB and ASIC.

Figure 7. Typical Multi-Function Printer Application Along with Few Other Interfaces



Two 133.33MHz and 66.66MHz clocks are edge aligned.

4.4 Application 2

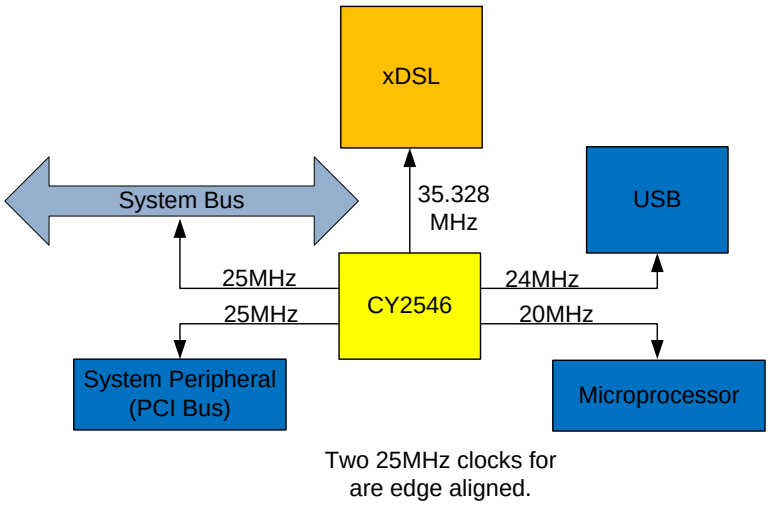
4.4.1 Femtocell

A femtocell improves signal quality in indoor environment and provides high speed wireless access to mobile-Internet users.

It uses existing DSL landline to connect to wireless network.

3G and 4G Femtocell has USB, PCI bus, PCI Peripherals, microprocessor, DSL device, and so on. System peripherals need to be synchronized with the system bus and they require low skew clocks. Multiple copies of low skew clock can be generated using CY2546; two low skew 25 MHz clocks are shown in Figure 8. Apart from this CY2546 can also meet clock requirement of microprocessor, USB and DSL device.

Figure 8. Femtocell Application



5 Summary

The Edge Align feature of CY254xx and MoBL clocks reduces the need for extra ZDBs and saves board space. CY254xx/MoBL clock synthesizer can address specific clock requirements in different applications without the need of extra clock chip as explained in this document.

Document History

Document Title: AN69091 - Edge Align Feature of CY254xx and MoBL® Clocks

Document Number: 001-69091

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3234665	BASH	04/19/2011	New application note
*A	3303004	BASH	10/14/2011	Rewrote whole Application Note
*B	3843531	PURU	12/17/2012	Updated Abstract. Updated Introduction (Updated contents in the section and added Figure 1). Updated Timing Budget and Clock Skew (Updated contents). Updated Edge Align Feature (Updated contents). Updated Examples and Applications (Updated contents). Updated in new template.
*C	4368380	CINM	05/02/2014	No technical updates. Completing Sunset Review.
*D	5747876	TAVA	05/24/2017	Updated template

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