JD Instruments LLC
14800 Central Ave SE
Albuquerque NM 87123
(505) 255-9182

TID-RLAT Test Report for Cypress 4Mb SRAMs (CYRS1049DV33)

Fab Lot 4126444

Date: 23 Apr 2012 Revision: A

Purchase Order: Cypress 2150257

Prepared By: _____ 23 Apr 2012
JD Instruments Date

Executive Summary

Radiation Lot Acceptance Testing (RLAT) for Total Ionizing Dose (TID) was performed on 4Mb SRAMs (CYRS1049DV33), fab lot 4126444. These parts showed very little change in measured parameters at any radiation level. All parameters stayed well within spec sheet limits up to 350K rad(Si) and the lot passed RLAT analysis using KTL statistics with Probability of Survival (Ps) of 99% and Confidence Level of 90%. In addition, no memory failures were detected in any devices, even at the maximum radiation level. All irradiation and testing was performed in accordance with MIL-STD 883H Method 1019.8 Condition A.

1.0 PART DESCRIPTION

Total Ionizing Dose (TID) Testing was performed by JD Instruments on one lot of 4Mb SRAMs (CYRS1049DV33). A total of 14 devices were used for this testing. Twelve devices were irradiated and two devices were reserved as control/reference. All parts were serialized by the manufacturer.

These devices have the architecture shown in Figure 1. This part is a pure static RAM with a power down function to insure low current consumption when it is not enabled.

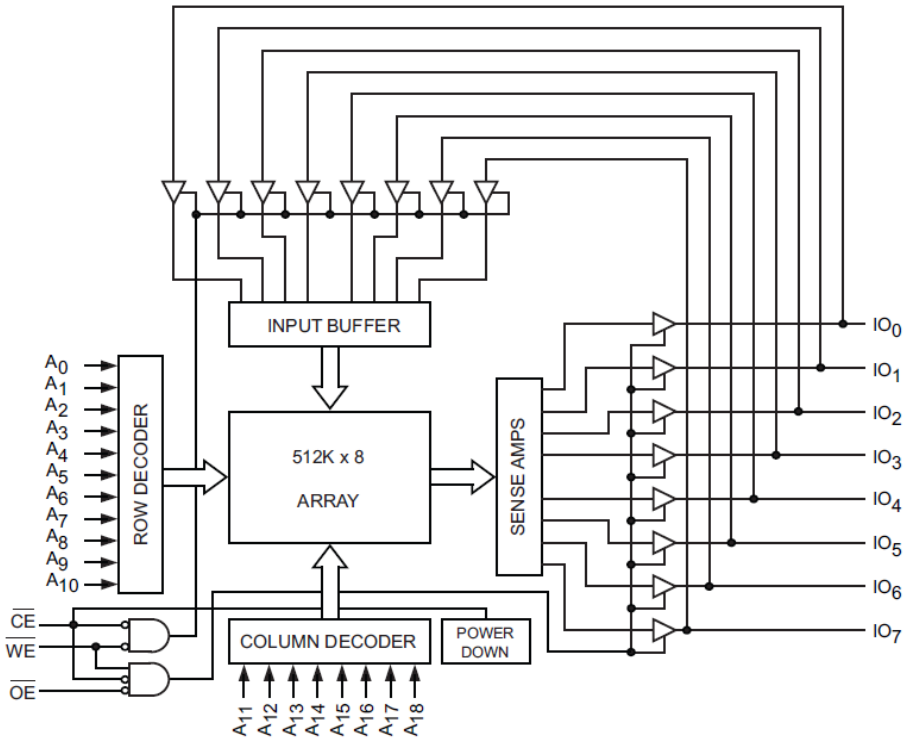

Figure 1. Functional Diagram for CYRS1049DV33

Devices were provided in 36 pin ceramic flat packages with pinout as shown in figure 2.

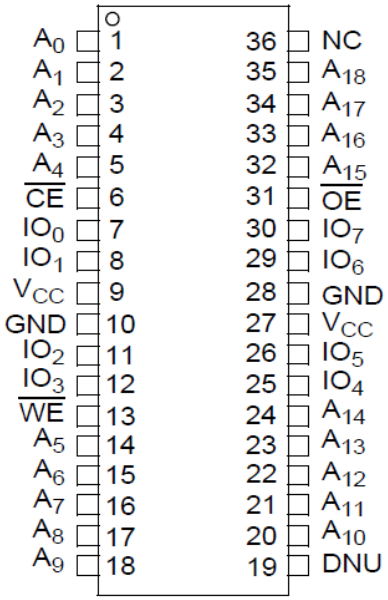

Figure 2. 36 Pin Flat Package Pinout

Four devices were mounted to each bias board prior to being exposed to radiation. These devices were arranged in a 2 X 2 matrix to minimize dose rate variation across the pattern. Figure 3 shows this pattern along with measured dose rates. Dose rates were measured using a calibrated meter as detailed in Attachment A. Measurements indicated less than +/-1% variation in dose rate across the exposure pattern.

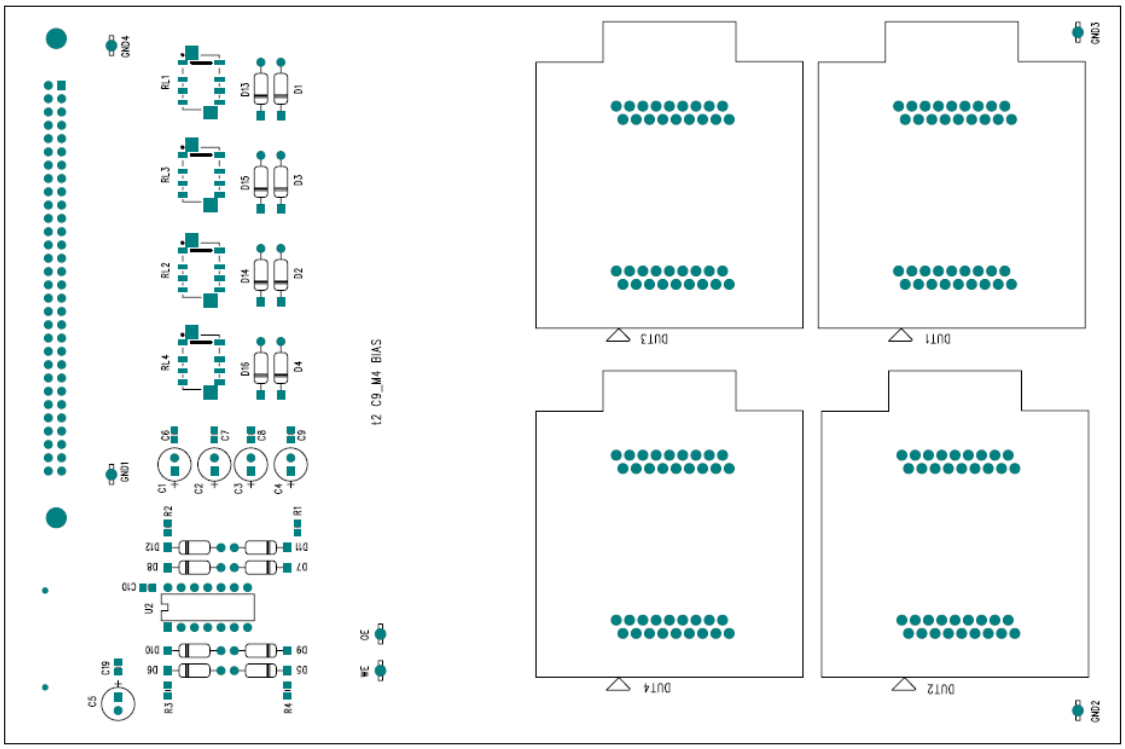

Figure 3. DUT Pattern and Dose Rate

Tests was performed using an Algorithmic Test Vector (ATV) system from JD Instruments as shown in figure 4. This is a portable system containing many of the features found in larger main-frame test systems. For this application it is particularly useful in that it collects data in both primitive error logs and also records summary results in spreadsheet form, simplifying on-site understanding of results as the test proceeds.

Figure 4. ATV Test System used for TID Testing

All irradiations and tests were performed on these parts in static bias condition with Checkerboard pattern loaded in memory and their maximum rated Vdd of 3.6V. Later functional and parametric testing was performed with devices biased to their nominal voltages of Vdd=3.3V. Data retention was tested by lowering the Vdd to 2.0V.

All tests were performed at room temperature which was ~21^{0}C (70^{0}F). Devices were irradiated inside lead/aluminum boxes as shown in figure 5. Testing was performed "in-situ" while the parts were inside the lead/aluminum boxes after the co60 source had been lowered. Testing began within ~1 minute following the end of each radiation step. All testing was completed and parts were again under irradiation within ~½ hour.

Figure 5. RLAT Devices being Irradiated in Lead/Aluminum Boxes at Co60 Facility

Circuit schematics for the bias and test boards are presented in Appendix B.

Irradiations were performed to cumulative doses of 100K, 200K and 350K rad(Si). After parametric measurements were made on all devices at the 350K rad(Si) level they were packed in dry ice and shipped to DPACI for AC characterization. Temperature of devices shipped in dry ice was -77^{0}C when packed and -66.8 ^{0}C when unpacked at DPACI (Note: shipping limit is < -60^{0}C). Accept/reject analysis is based on measurements made at the 350K rad(Si) level.

Irradiation exposures were performed in a cobalt-60 (Co60) room irradiator located on Kirtland AFB. All testing was done in accordance with MIL-STD 883H Method 1019.8 Condition A. Testing was performed by H. Jake Tausch of JD Instruments and Helmut Puchner of Cypress Semiconductor.

These parts showed very little change in measured parameters at any radiation. All parameters stayed well within spec sheet limits up to 350K rad(Si).

2.0 Lot Acceptance Technique

Parameters were measured and recorded in an excel format spread sheet. The measured values at each radiation step were analyzed using the Radiation Lot Acceptance Test (RLAT) "variables method" (see MIL-HDBK-814, Appendix Section 50, especially Table IXB).

In the RLAT variables method the average (Avg) and standard deviation (Std) of each parameter are calculated for the group of parts being irradiated. A value is then calculated and compared to the part limits using this average and standard deviation along with a one sided tolerance factor, KTL.

For parameters where the limit is higher than measured values the lot is acceptable if

$$Avg + KTL * Std < Limit \qquad \text{(eq. 1)}$$

For parameters where the limit is lower than measured values the lot is acceptable if

$$Avg - KTL * Std > Limit \qquad \text{(eq. 2)}$$

Values for KTL vary depending on sample size, Probability of Survival (Ps) and confidence level. For this test, with a radiation sample size of 12, Ps of 0.99 and a confidence level of 0.9, the value for KTL was 3.372 (MIL-HDBK-814, Table IXB).

Figure 6 shows test results for one of the parameters that changed with radiation. This is a plot of Isb (CB) (Stand-by power supply current when memory is loaded with a checkerboard pattern) vs radiation and is illustrative of how parametric data is presented in the rest of this report. Note that checkerboard was the pattern loaded into memory while the parts were being irradiated.

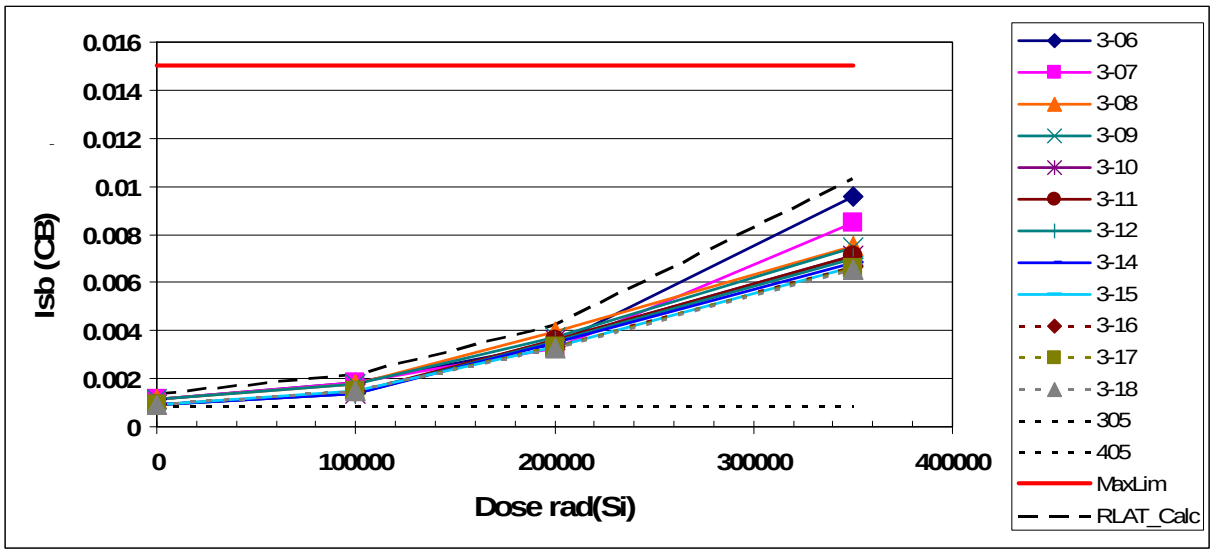

Figure 6. Isb(CB) Variation with Radiation

First note that the limit is plotted as a solid, bold red line, 15mA in this case. Second, note that the reference devices (SNs 305 and 405) are plotted as dotted lines with no symbols. Since the reference devices were not irradiated then their value should remain the same across the plot. Measurements of the reference devices provide an indication of repeatability of the test for the parameter being plotted. Each irradiated part is plotted as a separate solid or dashed line with varying symbols. The RLAT calculation for this set of parts is shown as a bold dashed line.

An RLAT value was calculated at each radiation step using the first equation described above. Specifically:

RLAT_CALC = Avg + 3.532 * StdDev

The reference devices were not included in RLAT calculations.

The plot shows a gradual increase in supply current for cumulative doses up to 350K rad(Si). The lot passed RLAT analysis for this parameter.

3.0 Measured Parameters and Results

The following parameters were measured and used for acceptance. Pass/Fail limits for each parameter are listed with each parameter.

ON-SITE TESTS

1. Functional Write/Read over entire device (no bit failures)
2. Data Retention over entire memory (no bit failures)
   a. Write with Vdd = 3.3V
   b. Lower Vdd to 2V for 1 Sec
   c. Read with Vdd= 3.3V
3. Isb
   a. Checkerboard (15mA)

b. Checkerboard* (15mA)
c. Retention (CB) (15mA)

4. Input Leakage Current – IiL/Iih (1uA)
5. Output Leakage Current (Tri-Stated) – Iozl/Iozh (1uA)
6. Output High Voltage - Voh (min) (2.4V)
7. Output Low Voltage - Vol (max) (0.4V)
8. Vih (min) for proper operation (Less than 2.0V)
9. Vil (max) for proper operation (Greater than 0.8V)

PRE-/POST Irradiation Tests at DPACI

1. Taal – Address low to data valid (12nS)
2. Taah – Address high to data valid (12nS)
3. Tacel – CE* low to data valid (12nS)
4. Taceh – CE* high to data invalid (12nS)
5. Tdoel – OE* low to data valid (6nS)
6. Tdoeh – OE* high to data invalid (6nS)
7. Icc@83MHz – Power Supply Current when DUT is Operated (enabled) at 83MHz

4.0 RLAT Analysis Results

No memory bits on any device ever failed during this testing, either during functional or retention testing, and are therefore not discussed further. Results of the other parameters are presented below.

4.1 Isb – Checkerboard, Checkerboard(Not) and Retention

Isb(CB) was shown previously and passed RLAT analysis. It is repeated here for ease of comparison to other patterns.

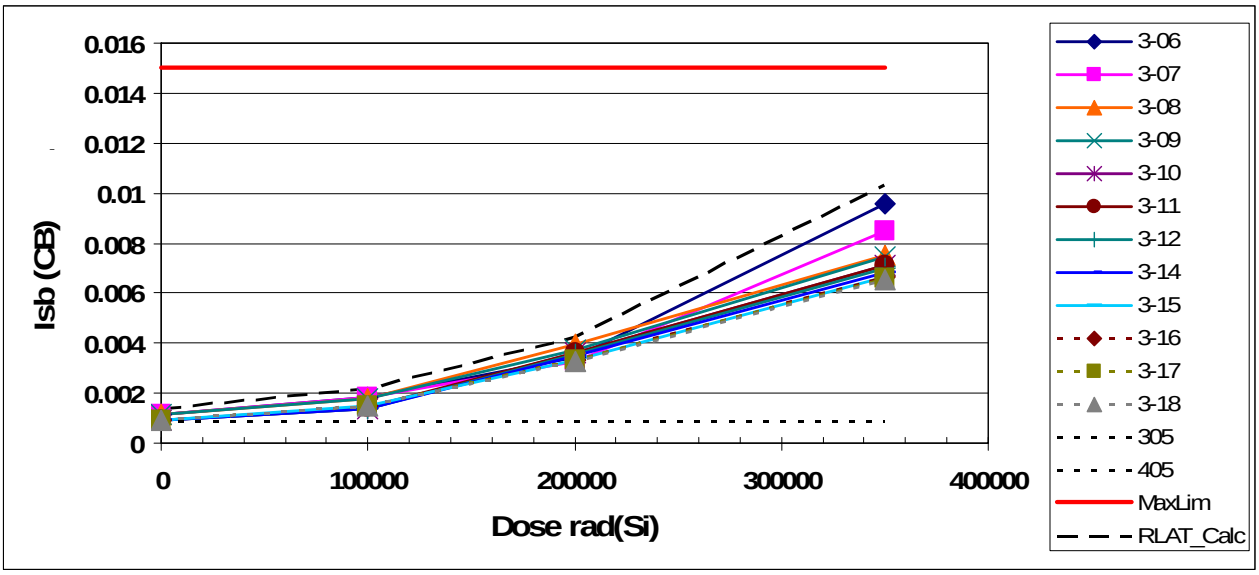

Figure 7. Isb(CB) Variation with Radiation

Figure 8 shows Isb vs. radiation when memory is loaded with the complementary pattern (CB*). Note that this current increase is slightly smaller than for the CB pattern. This difference in increase shows that there is a slight pattern dependence in the radiation sensitivity for these parts. The increase for either pattern is well below the parameter limit.

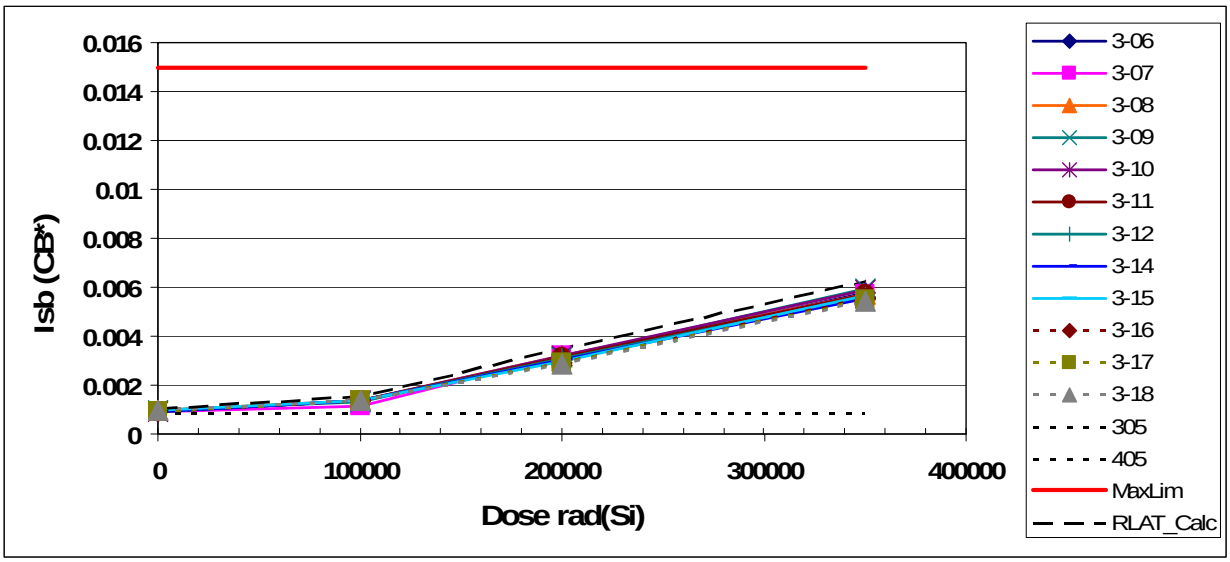

Figure 8. Isb(CB*) Variation with Radiation

Figure 9 shows Idd-Retention vs. radiation. This was measured by loading memory with the complementary checkerboard pattern (CB*) and reducing Vdd to 2.0V to put the part in retention conditions. Note that this current is almost identical to that seen when the same pattern is loaded into memory and Vdd is at it's normal operating level. The increase in current is well below the parameter limit.

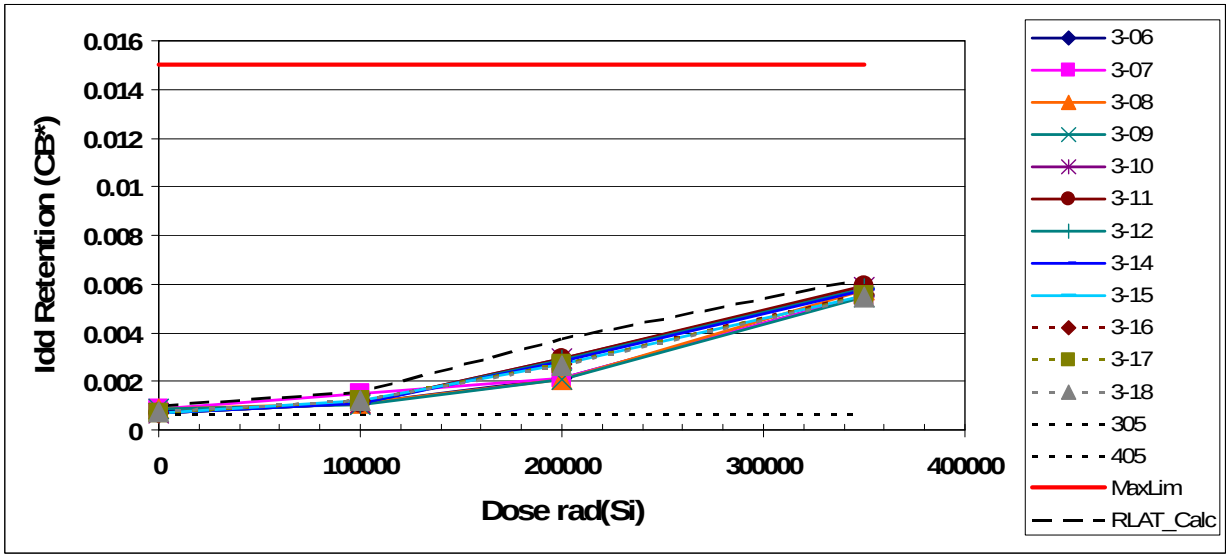

Figure 9. Idd-retention(CB*) Variation with Radiation

4.2 Vih and ViL

Figures 10 and 11 show measurements and RLAT analysis for Vih and Vil testing.

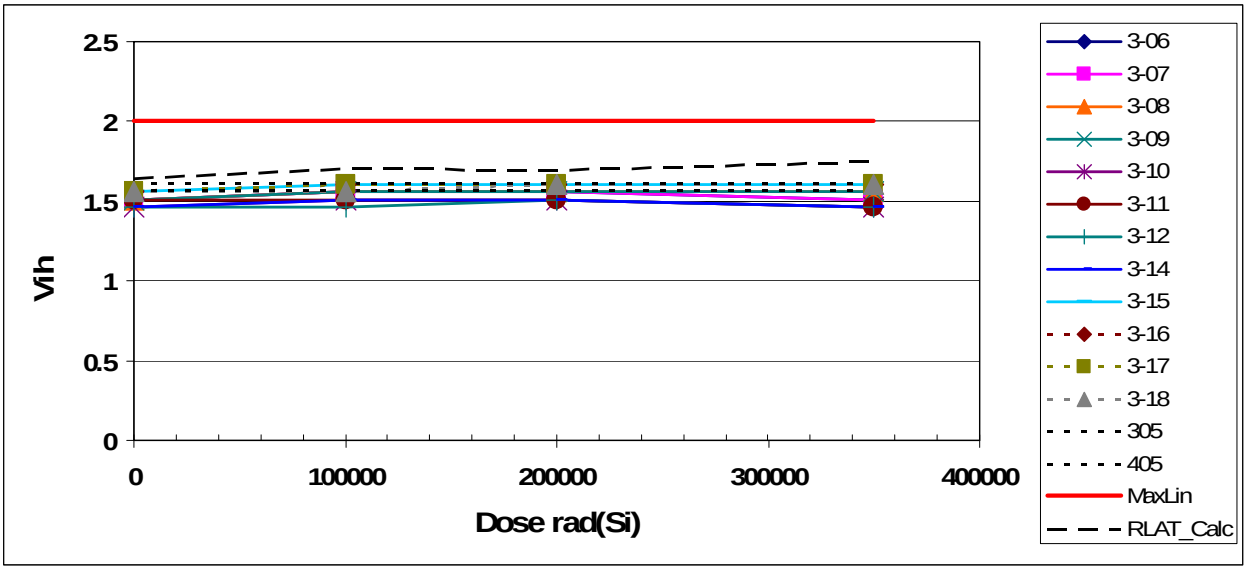

Figure 10. RLAT Results for Vih

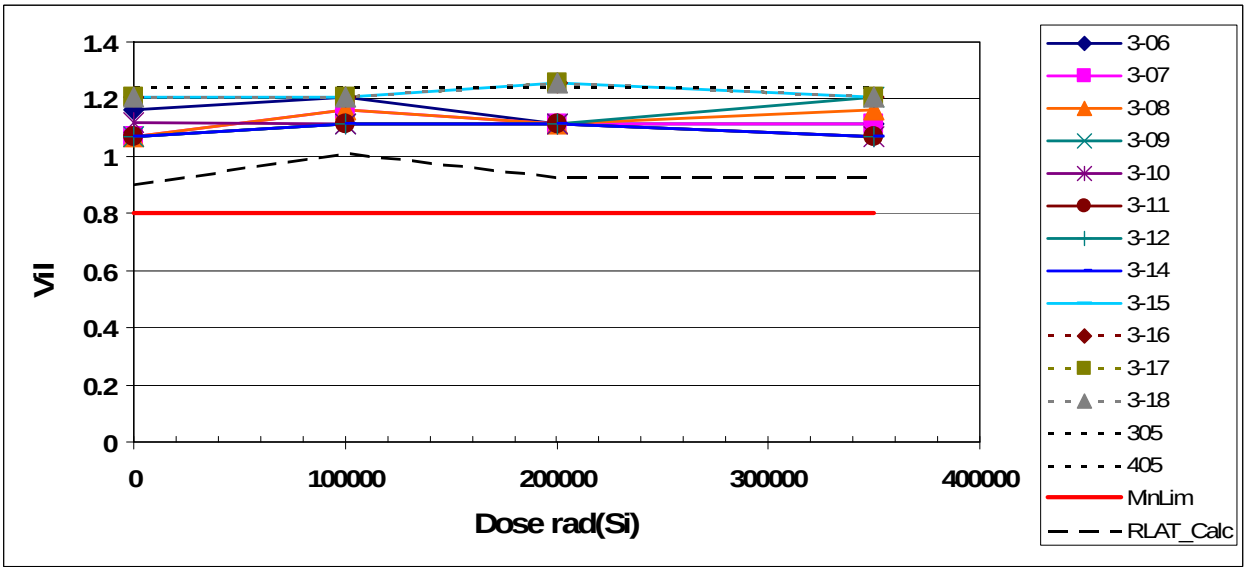

Figure 11. RLAT Results for ViL

These parameter are measured by varying logic high and logic low voltages in a binary search sequence to determine the voltage where the parts pass functional testing. The smallest step was ~25mV so there is some granularity in the results. There was no detectable change in this parameter with increasing radiation and the lot passes RLAT analysis for both parameters.

4.3 Voh and Vol

Voh and Vol were measured with load currents specified in the data sheet (Ioh = -4mA, Iol = 8mA). These parameters did not show any change with radiation Both parameters easily pass RLAT analysis.

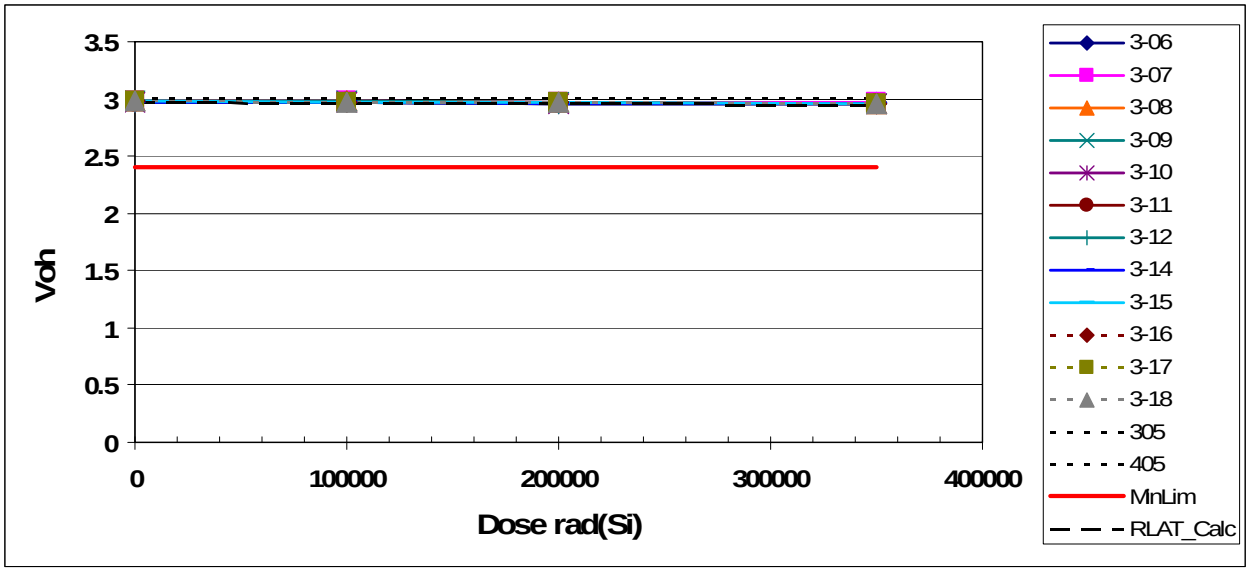

Figure 12. RLAT Results for Voh

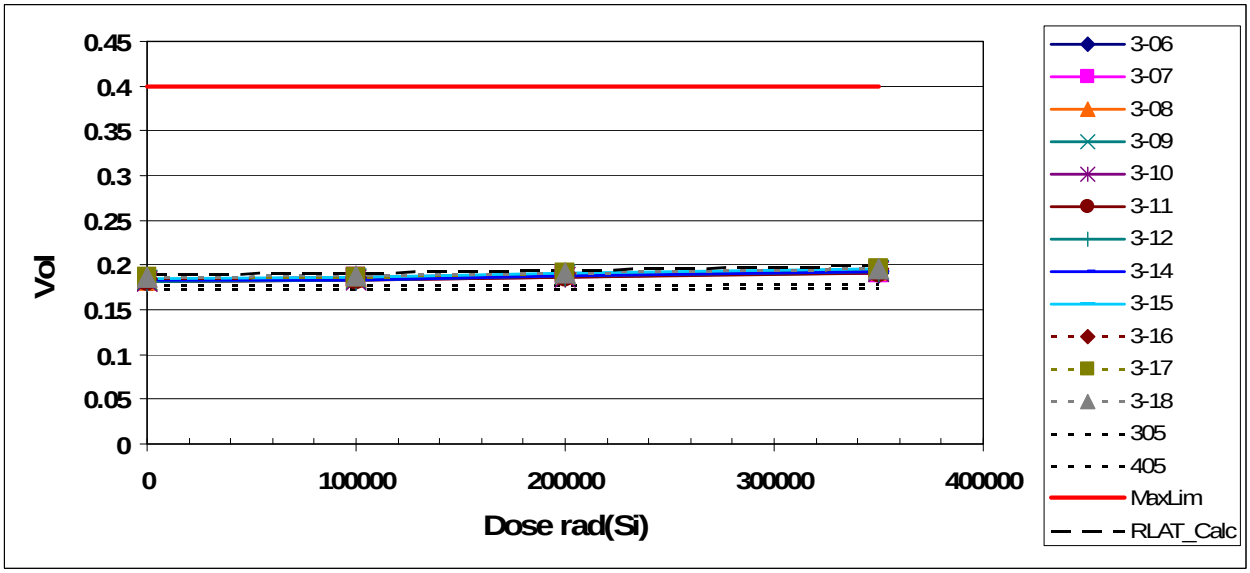

Figure 13. RLAT Results for Vol

4.4 Iih and IiL

Iih and Iil are the input leakage currents when the inputs are biased to a logic high and logic low. Both have a limit of 1uA. There was a slight increase in Iih, but both parameters easily pass RLAT analysis.

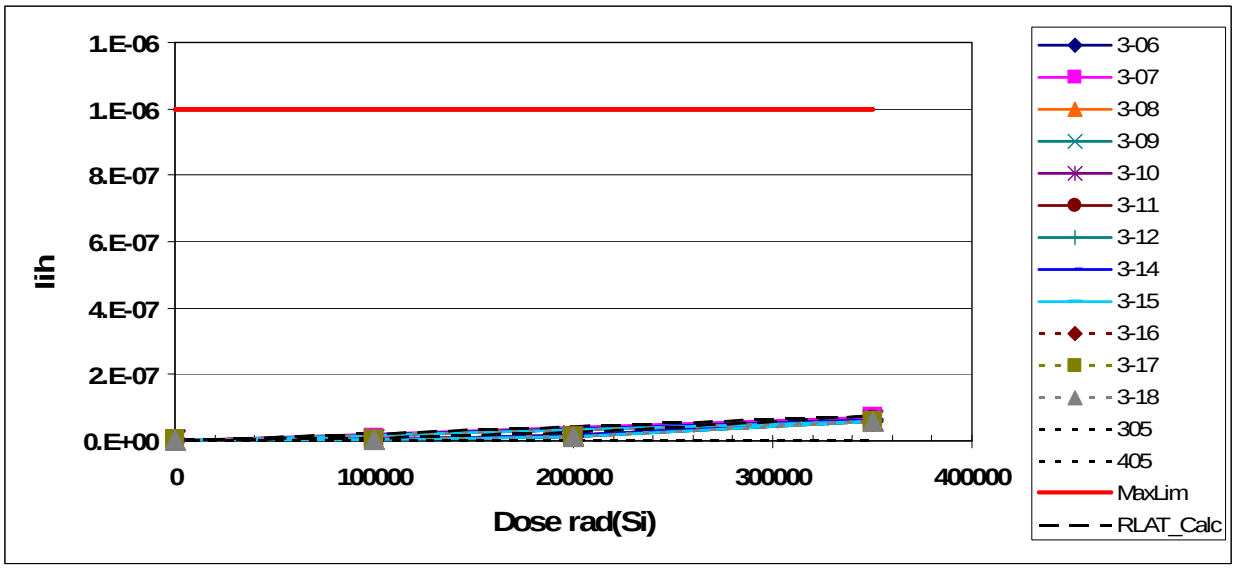

Figure 14. RLAT Results for Iih

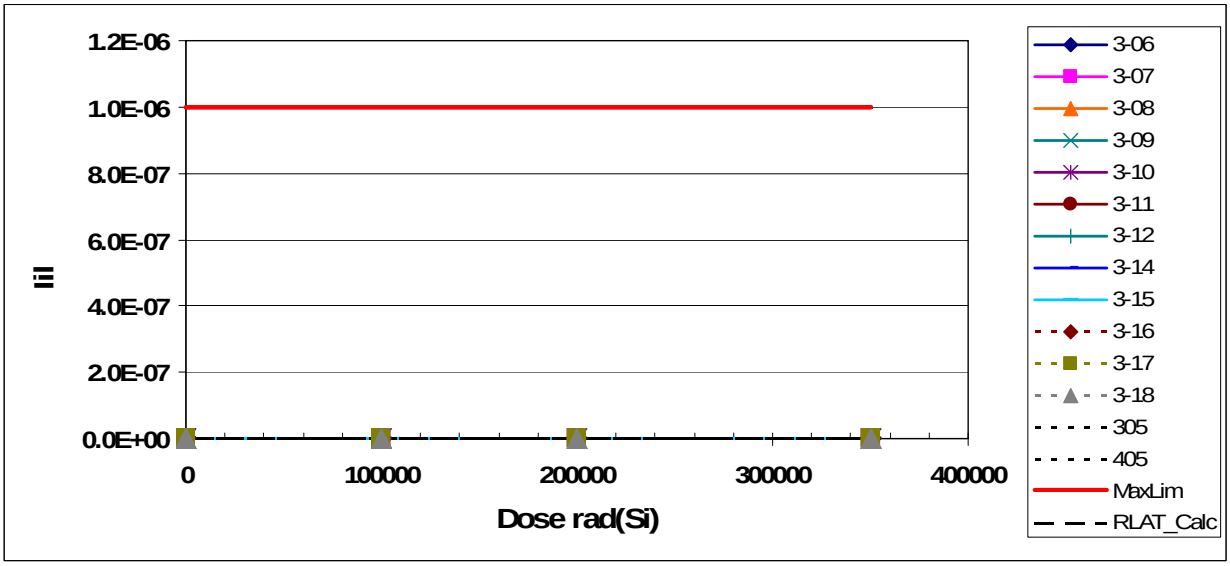

Figure 15. RLAT Results for IiL

4.6 Iozh and IozL

Iozh and Iozl are the output leakage currents when devices are tri-stated and voltages equal to logic high and logic low are applied to the outputs. Limits are 1uA for both parameters. As shown in Figures 16 and 17 both parameters easily pass RLAT analysis. There was a slight increase in Iozh at 300K rad(Si), but not enough to significantly affect the analysis.

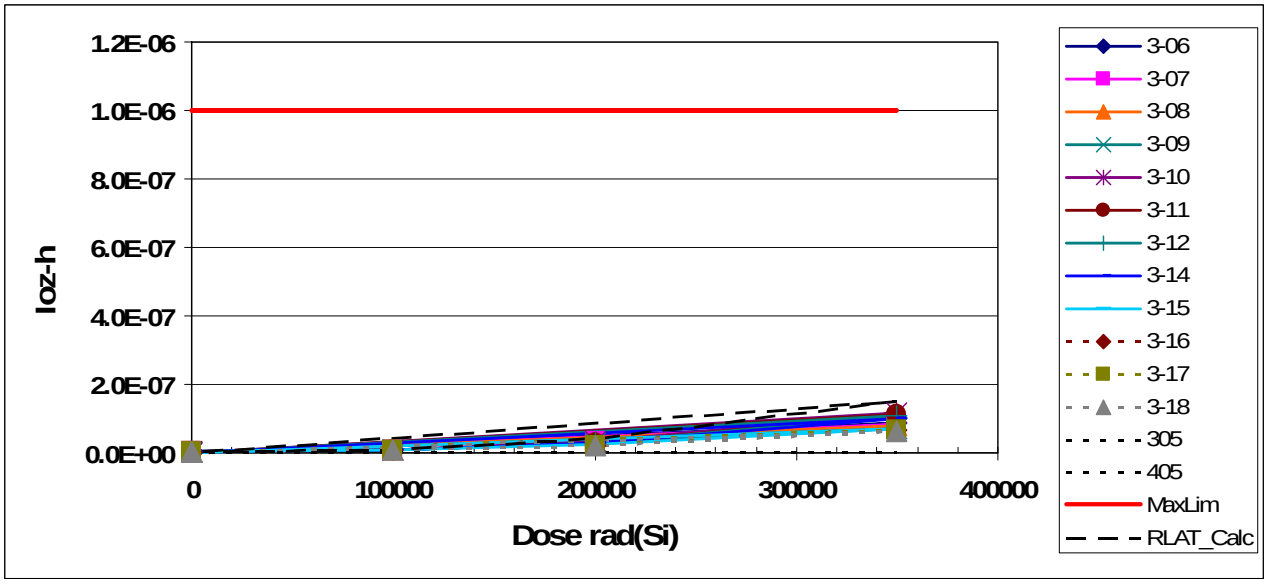

Figure 16. RLAT Results for Iozh

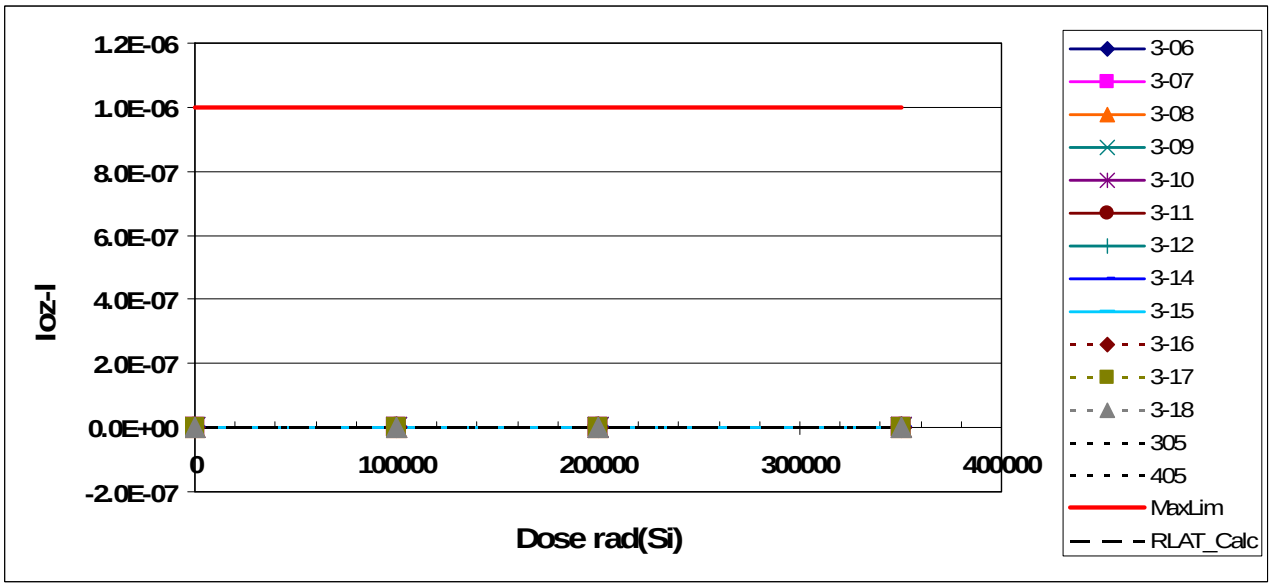

Figure 17. Results for IozL

4.7 AC Timing Measurements

A variety of timing measurements were made on these parts at DPACI, pre- and post-radiation. These parameters are shown below in figures 18 thru 23. Note that none of the timing parameters showed any change over radiation and all parameters easily passed RLAT analysis.

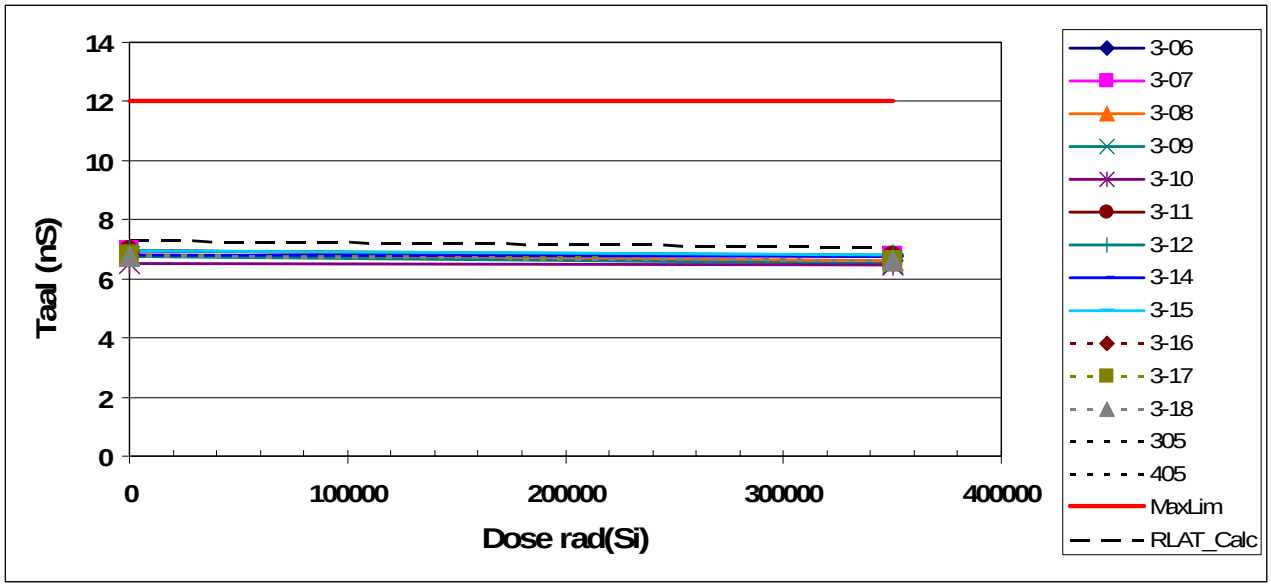

Figure 18. Address Low to Data Valid Access Time

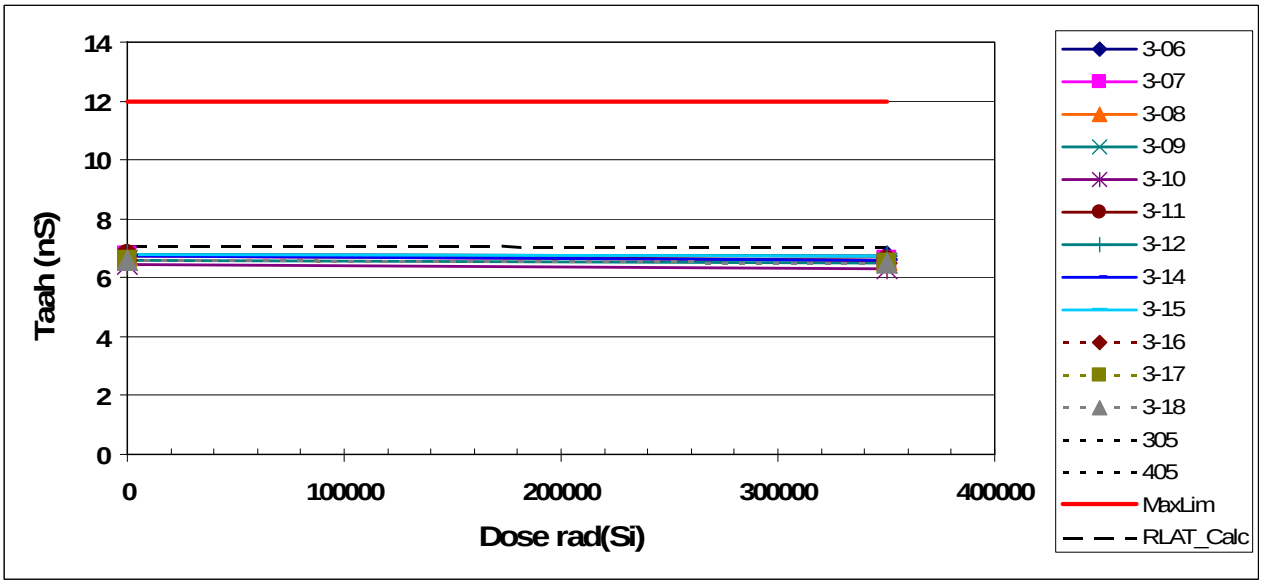

Figure 19. Address High to Data Valid Access Time

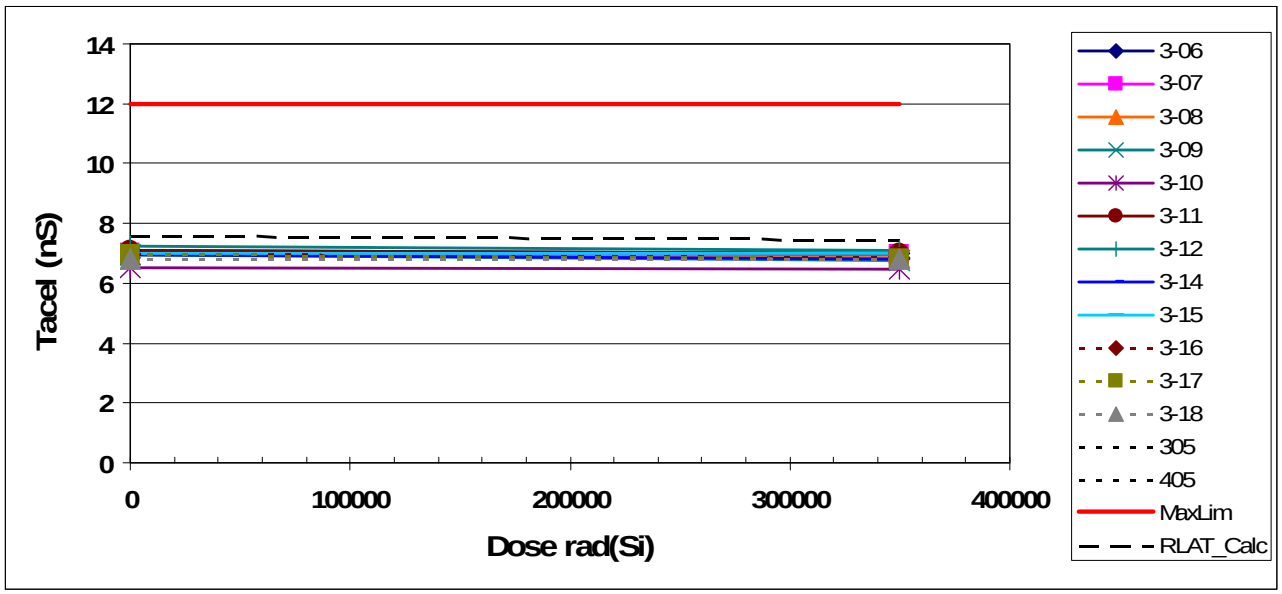

Figure 20. CE* Low to Data Valid Access Time

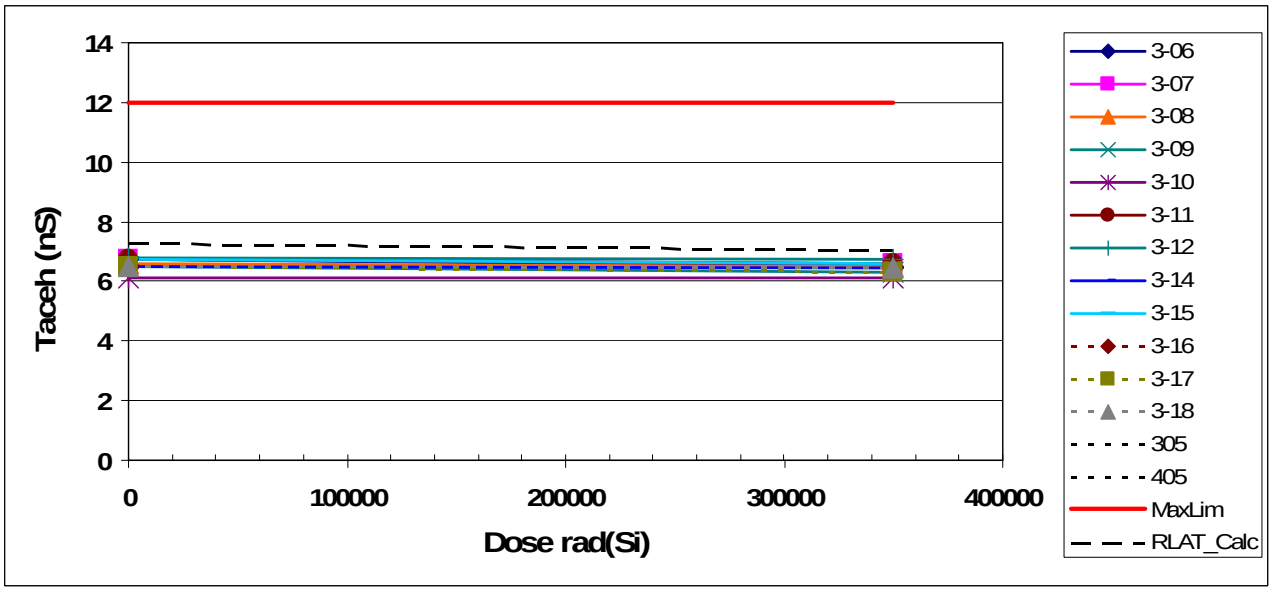

Figure 21. CE* High to Data Invalid Time

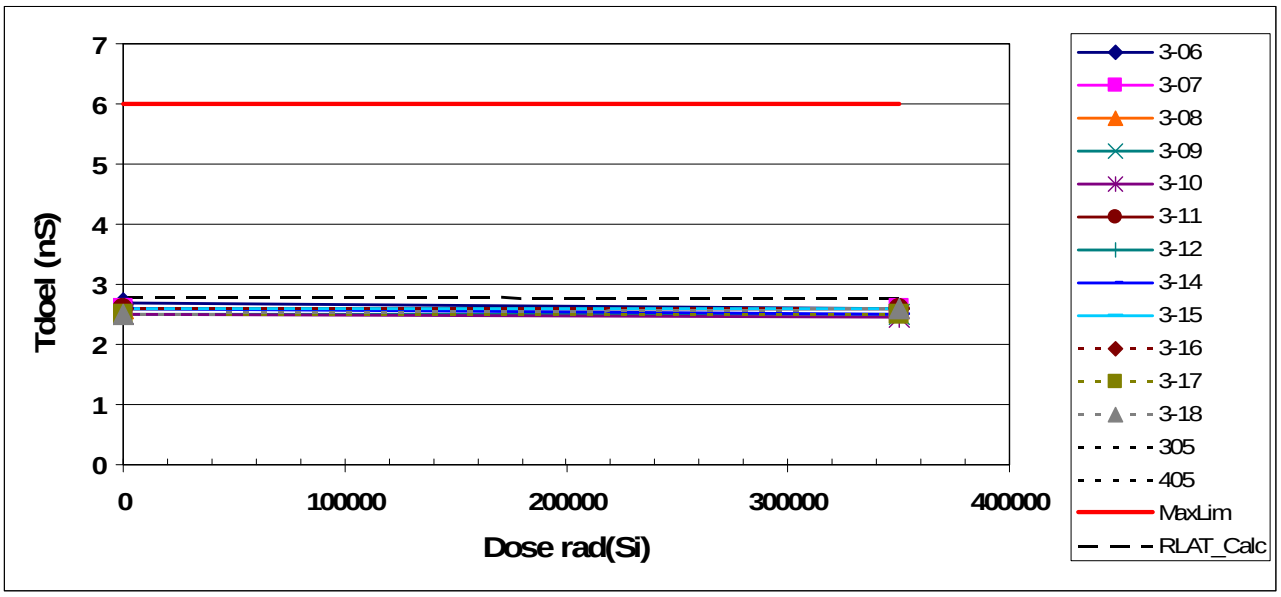

Figure 22. OE* Low to Data Valid Access Time

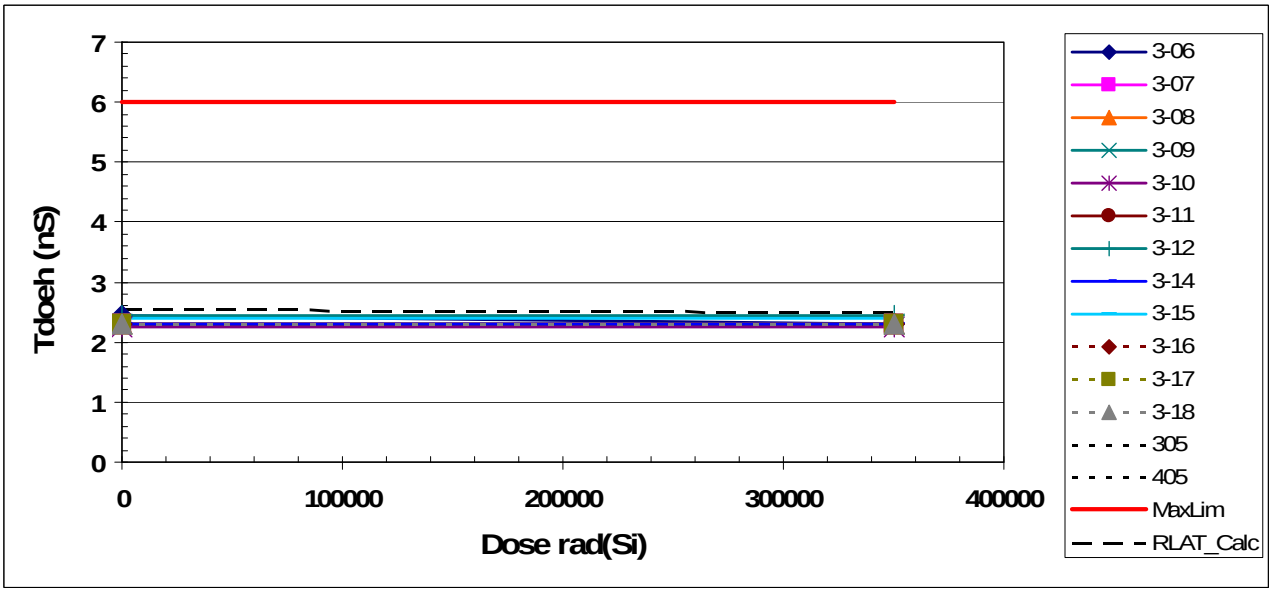

Figure 23. OE* High to Data Invalid Time

4.8 Idd@83MHz

Figure 24 shows the pre- and post-radiation operating current (Idd) when the devices are run at 83MHz. Note that there is a slight increase in current with radiation. This increase is consistent with that seen in stand-by currents as shown earlier. The increase doesn't appear as pronounced here because of the much higher starting (pre-rad) currents.

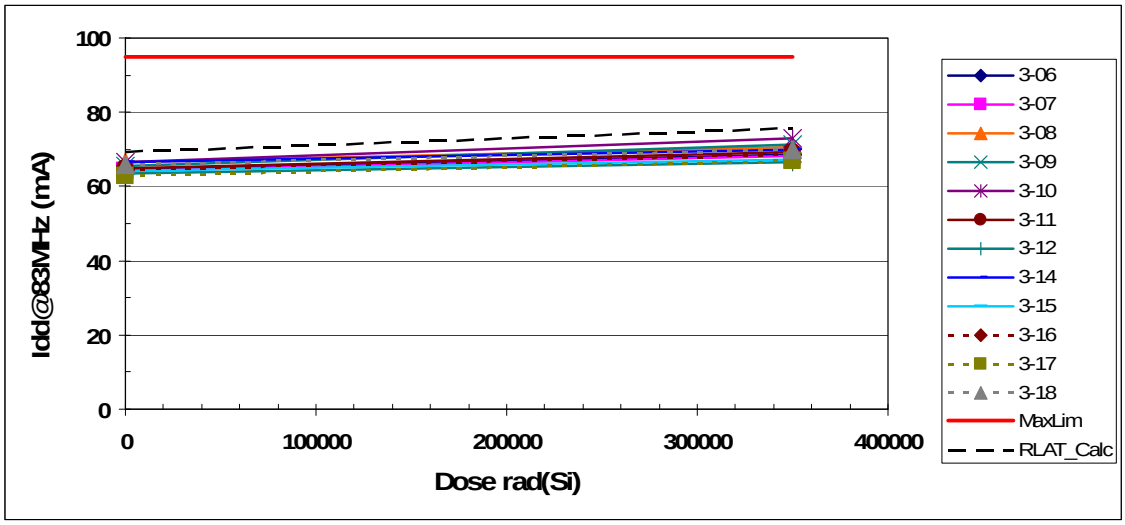

Figure 24. Idd When DUT is Operated at 83MHz, Enabled

5.0 Conclusions

This fab lot of CYRS1543AV18 devices showed no appreciable radiation induced change up to 350K rad(Si). The lot passed RLAT analysis on all included parameters after the application of 99/90 KTL statistics.

Appendix A. Calibration Information

A.1 Test Equipment - Test stimulus and parametric measurements were provided by an Algorithmic Test Vector (ATV) and a Parametric Work Station (PWS), both manufactured by JD Instruments. Both units have calibration traceable to NIST.

A.2 Radiation Source – See letter below.

DEPARTMENT OF THE AIR FORCE

AIR FORCE RESEARCH LABORATORY (AFMC)

29 March, 2012

MEMORANDUM FOR JD Instruments

FROM: AFRL/RVSE
Bldg 914
3550 Aberdeen Ave SE
Kirtland AFB NM 87117

SUBJECT: Calculating the Dose Rate at the Air Force Research Laboratory Cobalt-60 Irradiator

1. The TID test for JDI Jake Tausch on (March 29, 2012) was irradiated, measured and calculated using a calibrated/certified ion chamber. The instrumentation that was used was manufactured by Radcal Corporation, in Monrovia, California. The Control Unit for the ion chamber is a 2025, serial number 2898, and an ion chamber used for the measurement was a 20X6-0.18, serial number 22193. These units were calibrated together and certified on May 24, 2011, due date calibration is May, 2012. Certification records can be provided upon request.

2. There were 4 parts in sockets on each board to total 12 parts that were irradiated. Radiation measurements were taken with an ion chamber at 2 positions where the DUTs (Device Uunder Test) would be located which were within an acceptable 2 percent variance of one another. The dose rate was measured at 90 Rad(Si)/s which was corrected for temperature/barometric pressure, probe amplification, and for deposited dose in Silicon. TID was stepped at 100, 200 and 450KRad respectively. The source is a panoramic irradiator and hosed in a large volume area where back scatter is not possible due to the distances to any interactive materials, however in order to maintain MIL-STD-883 the measurements and tests were attained inside a Pb/Al box.

3. If there are any questions concerning the calculated exposure for this test, please contact the Radiation Safety Officers; Mr. Richard Netzer, AFRL/RVSE at 505-846-6889 (Richard.netzer@kirtland.af.mil) or Mr. William Kemp, SAIC, at 505-314-3542 (William.t.kemp@saic.com).

RICHARD NETZER, GS-12, USAF
Laboratory Manager, EF Section
Space Electronics Branch, AFRL/RVSEF

Appendix B. Board Circuit Schematics

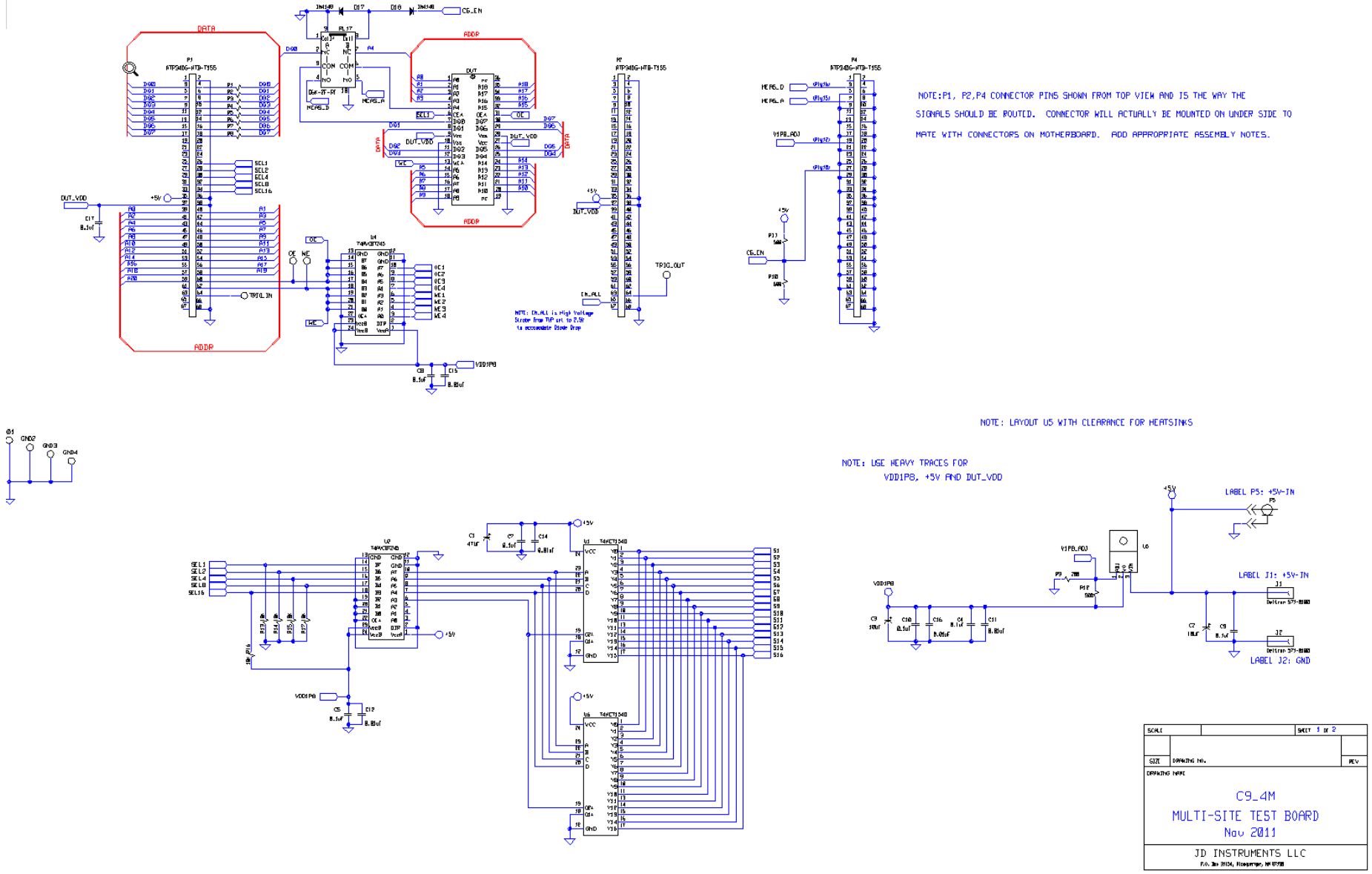

Figure B1. Test Board, Schematic 1 of 2

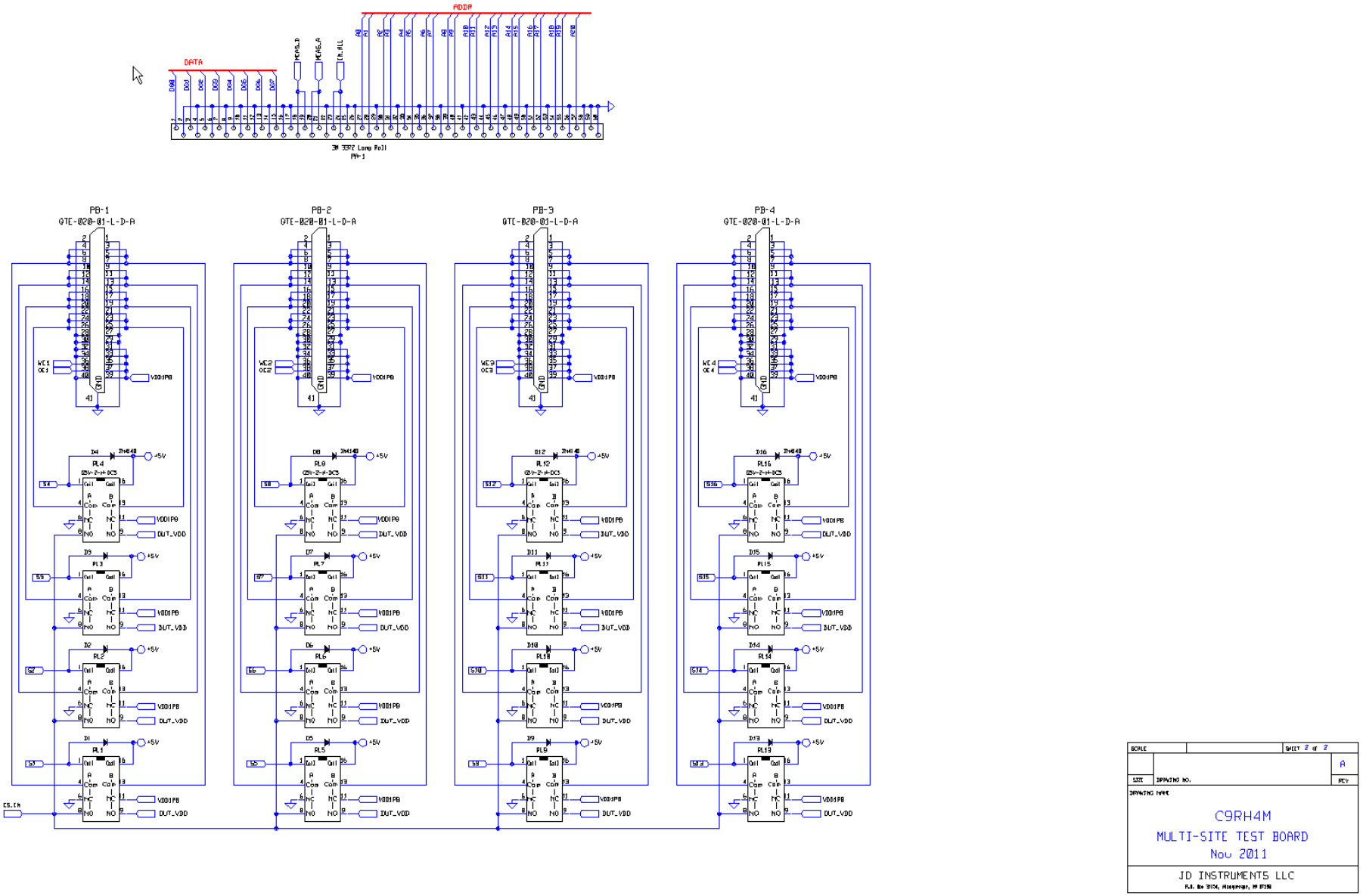

Figure B2. Test Board, Schematic 2 of 2

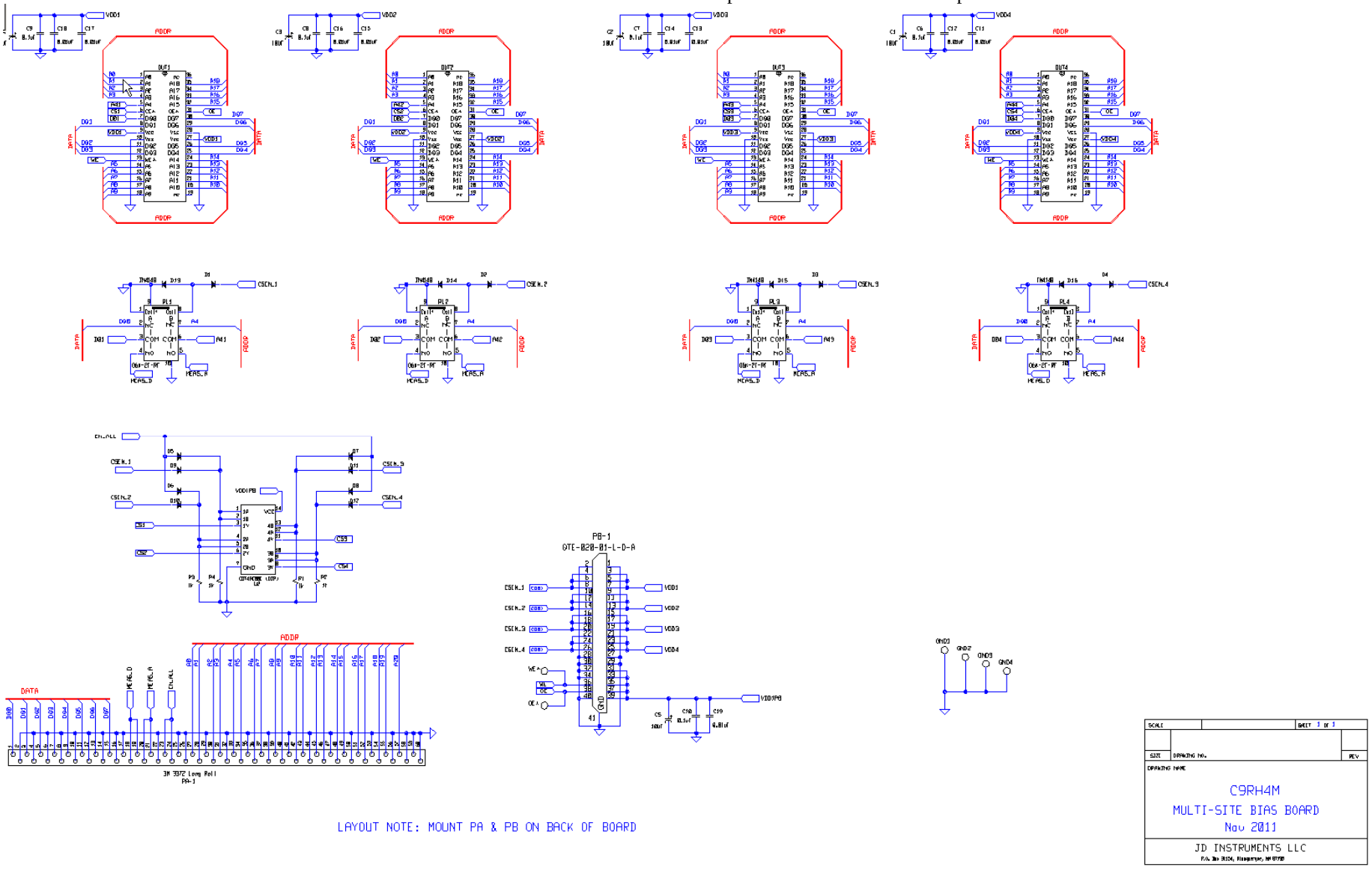

Figure B3. Bias Board Schematic