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WHITE PAPER

Abstract

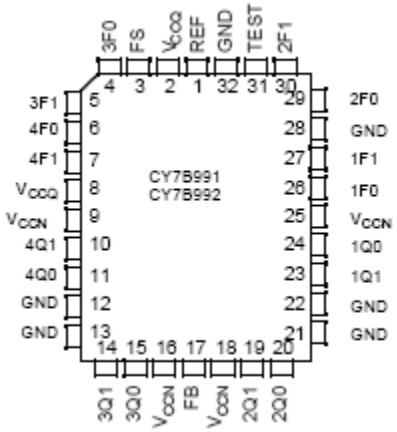
This document discusses the test mode capabilities of the RoboClock™ and RoboClock II™ family. It begins with an introduction to these devices and then discusses how to use the test mode features. The RoboClock II test mode disables the PLL, which allows you to debug your system design. Using the test mode function can improve your design and give you additional stability.

RoboClock™ and RoboClock II™ Test Mode

Introduction

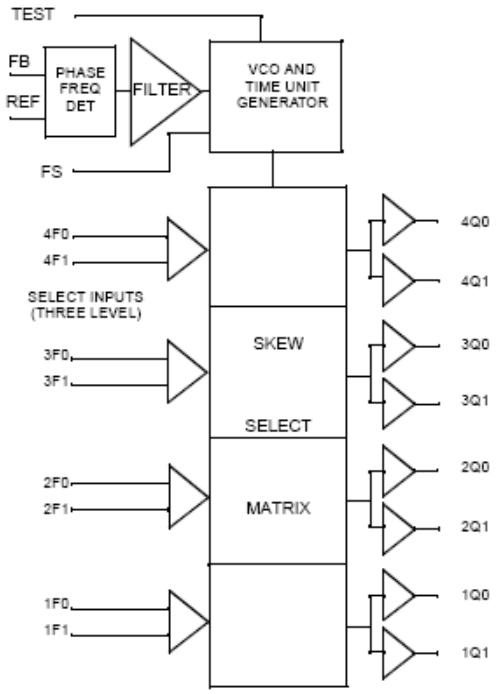
The RoboClock family consists of seven parts: two RoboClocks (CY7B991/2), a 3.3 V RoboClock (CY7B991V), a high speed RoboClock+ (CY7B9911), a 3.3 V high-speed Roboclock+ (CY7B9911V), and two RoboClock Jr.™ devices (CY7B9910/20). The CY7B991/10/11 has TTL outputs, CY7B991V/11V LVTTL outputs and the CY7B992/20 has CMOS (0 to VCC) outputs. Each device drives 50 Ω terminated transmission lines. Figure 1 shows the PLCC and LCC pin configurations for the RoboClock and RoboClock+ devices.

Figure 1. PLCC and LCC Pin Configuration



The block diagram shown in Figure 2 uses a PLL architecture. Connecting an output to the feedback (FB) input of the device causes the PLL to synchronize and align this output both in phase and in frequency with the reference (REF) input. This results in very low input to output delay and allows a system to connect RoboClock devices in parallel for clock distribution while maintaining very low skew among clocks from different devices.

Figure 2. RoboClock Block Diagram



RoboClock contains eight outputs grouped in four sets of two. Two function select lines (xF0, xF1) control the functionality of each pair of outputs (xQ0, xQ1). The outputs of an output pair operate identically.

Each pair of three-level function select inputs allows you to hardwire the operation of each output pair to one of nine delay or functional configurations. Each function select input pin can be connected to V_{CC} (HIGH), left unconnected (MID), or connected to ground (LOW). Table 1 shows the programmable skew configurations available on each output pair. The function select configurations in this table assume that the output connected to FB is set for 'zero' skew.

Table 1 also shows the range of t_U over which an output may be skewed with respect to the REF input. t_U is a function of the frequency at which the 1Q0 output is operating. RoboClock offers frequency coverage with three ranges from 15 MHz to 80 MHz (100 MHz for the CY7B9911 and 110 MHz for the CY7B9911V) with the use of the three-level frequency select (FS) input.

Table 2 shows the operating frequency range for each of the three levels of FS. The appropriate FS level selection must be made such that the anticipated operating frequency of the 1Q0 output is within the specified limits. There may be two acceptable levels for the FS pin when operating at certain frequencies. The appropriate connection of the FS pin, in this case, is based on the value of the time unit, t_U, required for the application. Table 2 also shows an equation that can be used to calculate t_U and the approximate operating frequency where t_U is equal to 1 ns.

Table 1. Programmable Skew Configurations

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	**1F0, 2F0, 3F0, 4F0**	**1Q0, 1Q1, 2Q0, 2Q1**	**3Q0, 3Q1**	**4Q0, 4Q1**
LOW	LOW	–4 t_U	Divide by 2	Divide by 2
LOW	MID	–3 t_U	–6 t_U	–6 t_U
LOW	HIGH	–2 t_U	–4 t_U	–4 t_U
MID	LOW	–1 t_U	–2 t_U	–2 t_U
MID	MID	0 t_U	0 t_U	0 t_U
MID	HIGH	+1 t_U	+2 t_U	+2 t_U
HIGH	LOW	+2 t_U	+4 t_U	+4 t_U
HIGH	MID	+3 t_U	+6 t_U	+6 t_U
HIGH	HIGH	+4 t_U	Divide by 4	Inverted

Table 2. Frequency Range Select and t_U Calculation

FS	f1Q0 (MHz)		(Insert from 001-23760) where N=	Approximate Frequency At Which t_U = 1.0 ns
	Min	Max		
LOW	15	30	44	22.7 MHz
MID	25	50	26	38.5 MHz
HIGH	40	80	16	62.5 MHz

For example, according to Table 2, a system using RoboClock with a clock speed of 33 MHz leaves the FS pin unconnected. The programmable time unit, t_U, based on this operating frequency, is

$$t_U = \frac{1}{f_{1Q0} \times N} = \frac{1}{33MHz \times 26} = (1.17ns)$$

Equation 1

In other words, you can adjust the position with which the rising and falling edges of the outputs move with respect to the corresponding REF input edge with a resolution of 1.17 ns when operating the device at 33 MHz. At 25 MHz, the t_U could be either 0.91 ns or 1.54 ns depending on whether the FS pin is tied LOW or left unconnected, respectively.

Test Mode Features

In some situations you may need to stop the PLL of the device. For instance, in many board-level testing applications you may need to supply a clock input to the system that does not meet the REF input requirements of RoboClock. This scenario can occur in bed-of-nails testing or single-step microprocessor execution. The test input of RoboClock allows operation in single-step mode.

The test input is a three-level input. In normal system operation, this pin is connected to ground, allowing RoboClock to operate as previously explained. (For testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100-Ω resistor. This will allow an external tester to change the state of these pins.)

If the test input is forced to its MID or HIGH state, the device operates with its internal PLL disconnected. The test input must be forced to less than 1 V (0.13 × Vcc for the low voltage (LV) parts) to ensure its LOW level, to $V_{CC}/2 \pm 500$ mV (Vcc/2 ± 100 mV for the LV parts) to insure its MID level, and to V_{CC} – 1 V (0.87 × Vcc for the LV parts) to ensure its HIGH level.

When RoboClock is put in test mode, after a few REF cycles, input levels supplied to REF will appear at all outputs after a 15-ns to 80-ns delay. The circuit effectively becomes a long chain of delay elements.

The level on the test input affects the length of time it takes for the REF signal to propagate through each delay element. When the test input is forced HIGH, each delay element will be selected to have its shortest delay

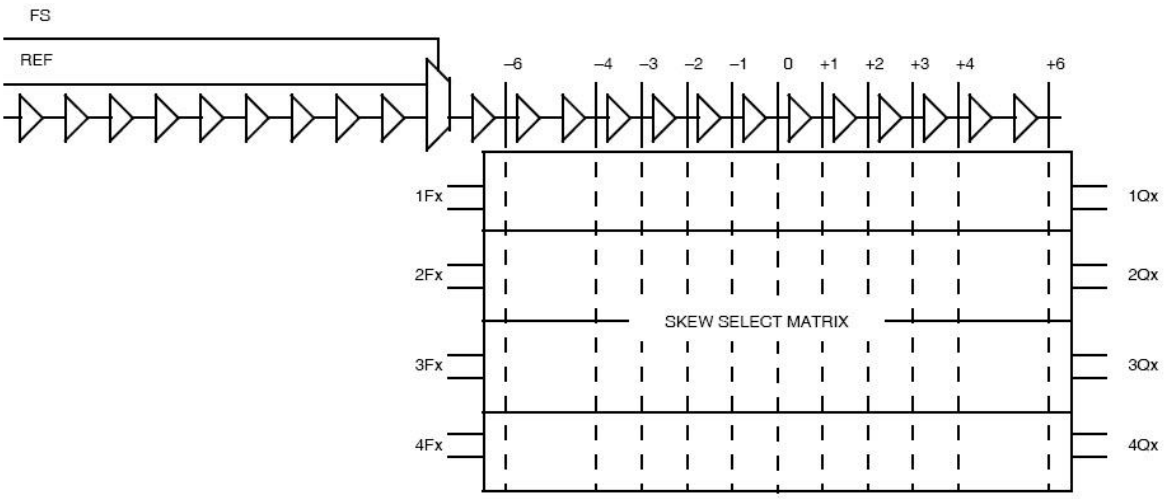
(< 700 ps). This is known as “contracted” mode. When the test input is forced to its mid state, the delay through each element will be as long as possible (> 1.5 ns). This is referred to as “extended” mode.

The level placed on the FS pin also determines the operation of RoboClock when it is in Test mode. The FS input is used to control the number of delay elements that the REF input will propagate through, as shown in Figure 3. When FS is held HIGH, REF will pass through only the last 13 delay stages. When FS is placed in the MID or LOW position, REF will propagate through all 22 delay elements.

Unlike normal operation (test tied LOW), FB will not have any effect on the operation of the outputs. All outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Outputs that have the divide-by-two output configuration selected will change state at every second REF input, and outputs that have the divide-by-four option selected will change state at every fourth REF input. An output selected for inverted operation will drive the opposite sense of the REF input.

Figure 3. RoboClock Test Mode



A counter reset is available for the divided outputs. To reset the counters, the 3F0 and 4F0 function selects must be placed in their MID position and a clock applied to the REF input. If the 3Qx or 4Qx outputs are then selected for a divided function (3Fx = LOW, LOW, HIGH, HIGH or 4Fx = LOW, LOW) then the 4Qx or 3Qx outputs will be in their HIGH state. The first REF clock causes these outputs selected for divided operation to transition LOW, and subsequent REF clocks cause these outputs to continue their normal output divided output pattern.

Introduction to RoboClock II

The CY7B993V and CY7B994V, known as RoboClock II, are the next generation in the well-known Cypress family of programmable skew clock buffers (PSCB). RoboClock differs from most zero-delay buffers in that it offers the user the ability to skew outputs relative in time to each other. This ‘skew-ability’ enables the system designer to offset trace length differences in a synchronous system or work around set-up and hold time differences.

These second generation devices have the added flexibility of frequency multiplication and division. This, for example, would enable the designer to take a 25-MHz clock and multiply it up to 150 MHz while also generating 30 MHz and 50 MHz clocks from the same source. The devices have 18 outputs with the capability to drive multiple loads. They also offer very low output skew and jitter.

The combined skew and frequency programmability make RoboClock II the most flexible clock buffer available in the market today. The parts have several other features which separate them from the competition. One of these is a flexible test mode. The test feature is the subject of this note. For more information on the RoboClock II family of clock buffers, see the datasheet section of www.cypress.com. There are also several application notes available from our website.

RoboClock II Test Mode

In some situations you may need to disable the RoboClock II phase-locked loop. For instance, in many board-level testing applications you may need to supply a clock input to the system that may not meet the REF input requirements of RoboClock II. This scenario can occur in bed-of-nails testing or single-step microprocessor execution.

The OUTPUT_MODE pin is a three level input. In normal system operation, this pin is set HIGH or LOW. For testing purposes, this three level input can have a removable jumper to ground or V_{CC}. This will allow an external tester to change the state of these pins.

If the OUTPUT_MODE pin is forced to its MID state, the device will operate with its internal phase-locked loop disconnected. The OUTPUT_MODE pin must be forced between 0.47*V_{CC} and 0.53*V_{CC} to ensure that it's set at the MID level. However, there is some flexibility around these settings and the MID level boundaries for typical silicon are compared to the data sheet limits in shown in Figure 4. If the pin is left floating, internal resistors will set it to the MID level.

When RoboClock II is put in test mode, input levels supplied to the reference input will be used in place of the PLL output. The signal applied to the reference input will pass through the internal logic of the device and the output of any given bank will be a divided version of the REF input. The actual divide ratio is dependent on the device being used (CY7B993V or CY7B994V), the FS setting and the divide setting on the output bank. Figure 5 illustrates the path the reference signal will pass through to reach the output.

Figure 4. Voltage Levels for the OUTPUT_MODE Input

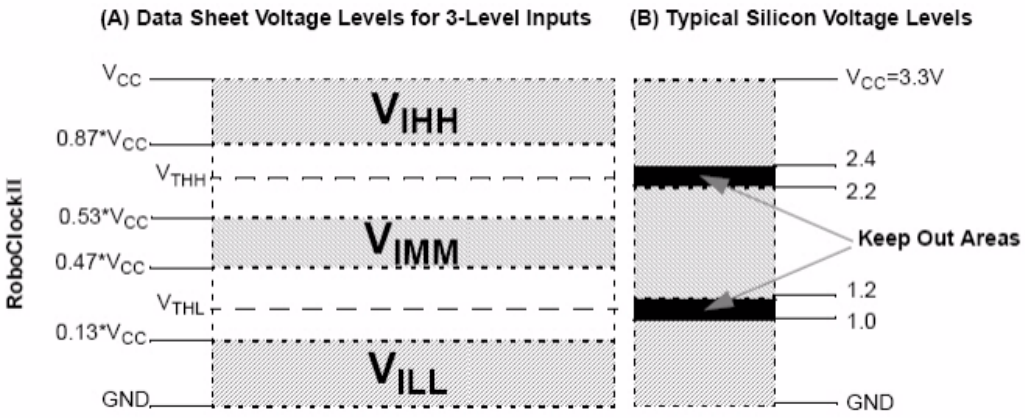
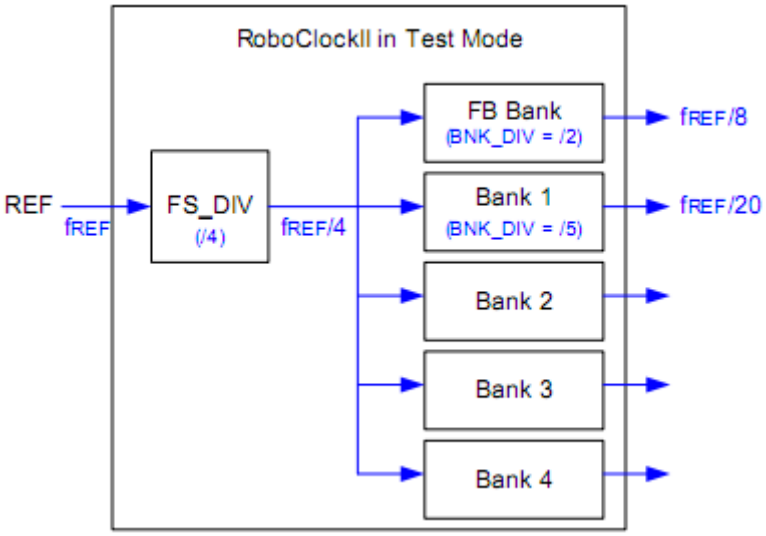


Figure 5. Clock Path in Test Mode



The effect of the internal divide ratio FS_DIV must be coupled with the programmed divide ratio for the particular output bank. For example, if the designer had a CY7B994V operating with FS HIGH, the internal divide ratio is 4 according to Table 3. If one of the banks was configured for divide-by-5, the output frequency in test mode would be $f_{REF}/(4*5) = f_{REF}/20$. For a 20-MHz input, the output of this bank would be 1 MHz in test mode.

The following equation can be used to determine the output frequency for any given configuration:

$$f_{OUT} = \frac{f_{REF}}{FS\_DIV \times BNK\_DIV}$$

Equation 2

Where:

f_{OUT} = output frequency of a given bank

f_{REF} = reference input frequency to RoboClock II

FS_DIV = the internal divide ratio for the FS setting (see Table 3)

BNK_DIV = the output bank divide ratio, determined by the DS and FBDS pins.

Table 3. Internal Divide Ratios (FS_DIV) in Test Mode

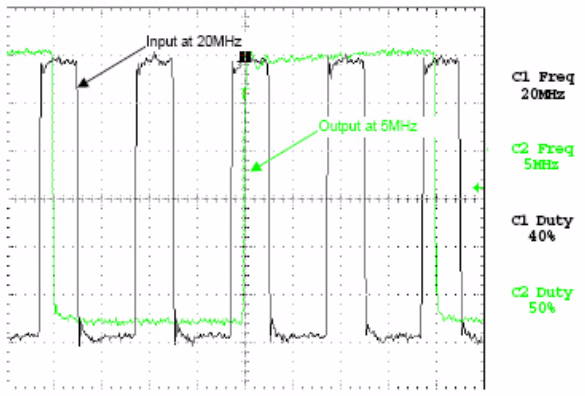
FS	CY7B993V	CY7B994V
LOW	32	16
MID	16	8
HIGH	8	4

There is no lower limit for the REF frequency in factory test mode. This is because in test mode the internal PLL is bypassed and the input levels supplied to REF directly control the internal logic. The input signal applied to REF will drive the internal state machine. The following scope waveform in Figure 6, shows a RoboClock II with the minimum divide ration of 4 (994 V with FS = HIGH and output configured to divide by 1).

Important Note In test mode, the selected FB input must be tied LOW.

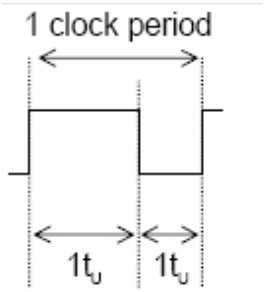
All functions of the device are still operational in test mode except the internal PLL and the output bank disables. All outputs will be 50% duty cycle in test mode regardless of the REF input duty cycle. This is illustrated in Figure 6 where the REF input has a 40% duty cycle and the outputs are still 50%.

Figure 6. RoboClock II Output in Test Mode.



The normal skew capability of RoboClock II is still available in test mode. However, the skew granularity calculation is slightly different. When in test mode, a one REF input period will translate to 2tU for skewed outputs. The positive width of the reference clock cycle is equal to the first time unit and the negative pulse width is equal to the second time unit. Thus, if the reference clock duty cycle is 50%, then half a clock period will be equal to 1tU. The skew functionality is shown in Figure 7.

Figure 7. Test Mode Skew Functionality



The OUTPUT_MODE pin is designed to be a static pin. Dynamically toggling this input from LOW to HIGH may temporarily cause the device to go into factory test mode, when passing through the MID state, and you may have to allow up to t_{LOCK} before the part resumes normal operation.

Factory Test Reset

When in factory test mode, the device can be reset to a deterministic state by driving the DIS4 input HIGH. When the DIS4 input is driven HIGH in factory test mode, all clock outputs will go to High Z; after the selected reference clock pin has 5 positive transitions, all the internal finite state machines (FSM) will be set to a deterministic state. The deterministic state of the state machines will depend on the configurations of the divide selects, skew selects, and frequency select input. All clock outputs will stay in high-impedance mode and all FSMs will stay in the deterministic state until DIS4 is deasserted. When DIS4 is deasserted (with OUTPUT_MODE still at MID), the device will re-enter factory test mode.

Summary

The RoboClock II test mode function gives users the option to test and debug their system in ways that might not be possible using the device in normal PLL operation. Bypassing the PLL and routing the reference input to the outputs permits input pulses and frequencies outside the datasheet-specified operation range, giving the system designer flexibility during testing and debug.

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