Cypress Board Level Reliability Test for Surface Mount Packages

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1.0 Introduction

Cypress has always been driven for improvements and excellence in every product being manufactured. Accompanying this are changes in material and processes that have significantly enhanced the quality and reliability of the devices, starting from wafer to finished products. To measure its characteristics, these products undergo rigorous tests composed of extreme environmental conditions that can brought about degradation on the product's functionality. This process is known as a Qualification Test.

Currently, the tests included for this process are based on both customer and industry requirements such as JEDEC, Mil Std, and AEC-Q100. These tests may be constituted by one or combinations of different accelerating stress factors such as temperature, pressure, humidity, and bias voltage. Most of these stresses are considered package level stresses. Another set of stresses are also dedicated for the solder interconnect level or board level reliability stresses.

Package level or 1st level reliability stress tests are dedicated to the robustness of the packaging materials and design to withstand extreme environmental conditions and does not consider its solder interconnect reliability when it is board mounted. While on the other hand, for the board level or 2nd level reliability tests, stresses are concentrated on the solder joint interconnect performance of the surface mount package when it is board mounted. This is composed of Board Level Temperature Cycle Test (BLTCT), Board Level Drop Test (BLDT), Board Level Bend Test (BLBT), and Board Level Vibration Test (BLVT). The “Board Level” term is used to emphasize that samples are board mounted while being tested. These tests consist of different mechanical and thermal shocks/stresses that simulate and/or accelerate the scenario experienced by the device during field applications. Among these are drop impact, vibration, and bending and thermal fatigues.

On the customer's standpoint, 2nd level tests are as important as 1st level tests. More customers are updating their requirements to consider 2nd level tests during qualifications. In doing these tests, customers can expand their market by satisfying the demands for high reliability and high risk electronic applications at minimum cost which will keep them in the lead of competition while ensuring a defect-free finished product.

2.0 Board Level Reliability Stress Tests

There are various Board Level Reliability tests available for electronic IC packaging and manufacturing but there are some which are specifically designed for surface mount devices. These tests are very essential in assessing the design for reliability of solder joint interconnects of device packages, as documented in IPC-D-279.

Board Level Temperature Cycling (IPC-9701/ED-4702A)

The purpose of this test is similar to the package-level temperature cycling where in bonded interfaces of different materials are assessed for reliability. Thermal cycling induces thermomechanical stresses caused by difference of thermal expansion between the printed circuit board (PCB) and the device package interconnects. The embrittlement effect of solder joints – comprised of compounding dislocation that leads to crack initiation and growth, (represented by fatigue ductility coefficient m) enhances the probability of its catastrophic failure.

Based on the solder attachment fatigue model Engelmaier-Wild (from IPC-D-279), the fatigue ductility exponent m, is calculated based on the formula:

$$\frac{1}{m} = 0.442 + 6x10^{-4} \bullet T_{SJ} - 1.74x10^{-2} \bullet \ell n \left(1 + \frac{360 \text{ minutes}}{t_D}\right)$$

where t_p is the half cycle dwell time (minutes) and the mean solder joint temperature, T_{SJ} (^oC) is given as:

$$T_{SJ} = \frac{1}{4} [T(max,comp.) + T(max,sub.) + T(min,comp.) + T(min,sub.)]$$

where:

T(max/min, comp) – actual max/min temp of component during the test
T(max/min, sub) – actual max/min temp of PCB or Substrate during the test

Board Level Bend Test (JESD22-B113/IPC-9702)

The purpose of this is to characterize the device package upon application of various cyclic mechanical loading during board mounting assembly and actual use. This repetitive or cyclic loading may induce flexing of boards that affects the solder joint interconnects of board mounted units. For this test, mechanical fatigue is the driving force for failure. One application that simulates this scenario is on the key press action of different handheld devices such as mobile phones, remote control devices, portable mp3/mp4 players, Laptops, and even the modern push button start engine for automobiles. This test is considered accelerated since the cyclic load applied is continuous, using a universal testing equipment (UTM) until the criteria for test end is achieved, unlike normal applications, where certain time interval is experienced after the load that allows relaxation of internal dislocations produced on the stressed solder joint material.

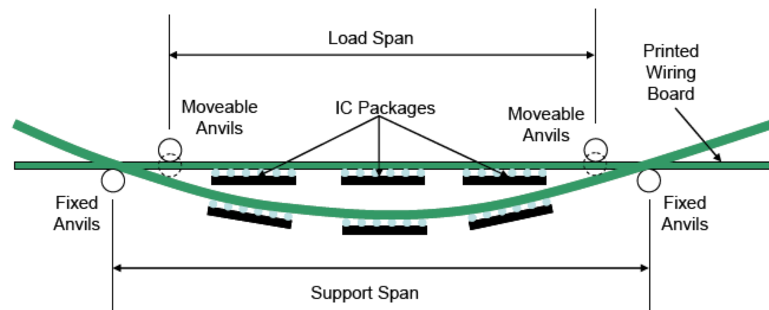


Illustration of board mounted units experiencing bend test

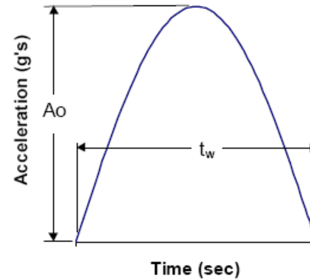
Board Level Drop Test (JESD22-B111/ED-4702A)

Similar to Board Level Bend Test, this test also aims to characterize the device package on various shock/impact stress levels experienced during board mount assembly and field applications. The most common scenario for this is accidentally dropping portable devices, and heavy duty electrical equipment used for critical applications that involve harsh and dynamic movements such as in automotive, aerospace and military.

The test method is composed of free-fall dropping the board mounted unit using a drop table and conditioned striking surface at specified height that corresponds to a shock of 1500G's at 0.5 millisec duration. To approximate drop height, the following calculation is used at rebound coefficient equal to 1.0 (no rebound):

$$A(t) = A_o \sin\left(\frac{\pi t}{t_w}\right)$$

$$\sqrt{2gH} = \frac{2A_o}{C}\frac{t_w}{\pi}$$



where:

H – drop height (cm)
A – acceleration (G's)
t – any given time
t_w – half-sine pulse (millisec)
g – acceleration due to gravity (981 cm/sec^2)
C – rebound coefficient (1.0)

Board Level Vibration Test (JESD22-B103)

According to JESD22-B113, "This method is intended to evaluate component(s) for use in electrical equipment. It is intended to determine the ability of the component(s) to withstand moderate to severe vibration as a result of motion produced by transportation or field operation. Vibration of this type may disturb operating characteristics, particularly if the repetitive stress causes fatigue. This is a destructive test intended for component qualification. It is normally applicable to cavity-type packages." Though this specification did not consider it as board level, it serves as a good reference for this type of test.

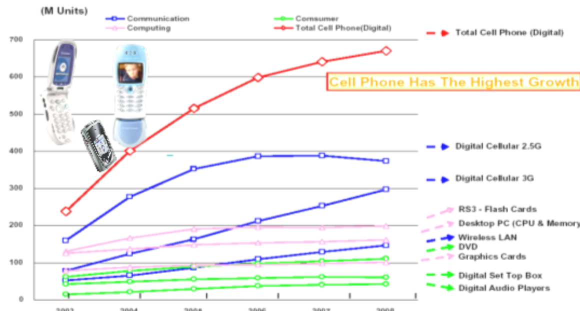
Service condition	Peak acceleration (G)	Displacement pk-pk (in / mm)	Cross-over frequency (Hz)	Min. / Max. frequency (Hz)
1	20	0.060 / 1.5	80	20 / 2000
2	10	0.040 / 1.0	70	10 / 1000
3	3	0.030 / 0.75	45	5 / 500
4	1	0.020 / 0.5	31	5 / 500
5	0.3	0.010 / 0.25	24	5 / 500
6	0.1	0.005 / 0.125	20	5 / 500
7	0.01	0.001 / 0.039	14	5 / 500
8	0.001	0.0005 / 0.0127	6.2	5 / 500

Component test level conditions for Vibration Test (JESD22-B113)

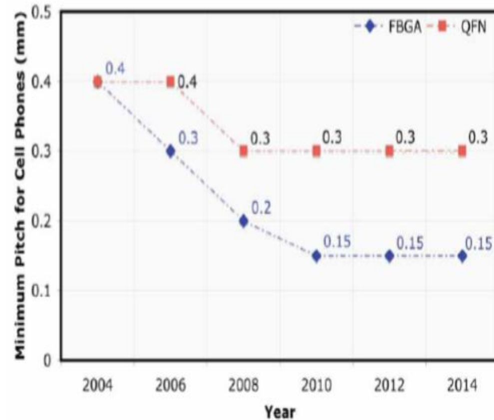
3.0 Roadmap

Previous visit from Taiwan-based material and IC electronics testing facility, Integrated Service Technology (IST) showed the current trend and roadmap for 2nd level reliability testing. One of the

concerns of doing 2nd level reliability test was the current trend in shrinkage of package footprint as well terminations such that solder interconnect becomes very critical during board mounting assembly.



Source: Dataquest (2004)



■Cellular and portable product will face high demand and environmental pressure.
■SIP and WLCSP is facing highly challenge in 2nd level reliability due to fine pitch and lead free requirement.
■Low k flip chip + lead free interconnect will face new material development challenge from 2nd level reliability requirement

Industry standard specifications were also available as baseline of most electronic manufacturing companies. (See table below)

Standard	Spec #	Title
JEDEC	JESD22-B111	Board Level Drop Test Method pf Components for Handheld Electronic Products
JEDEC	JESD22-B113	Board Level Cyclic Test Method for Interconnect Reliability Characterization of Components for Handheld Electronic Products
IPC	IPC 9701	Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments
IPC	IPC 9702	Monotonic Bend Characterization of Board-Level Interconnects
JEITA	ED-4702A	Mechanical Stress Test Methods for Semiconductor Surface Mounting Devices

4.0 Test Conditions

Based on mentioned specifications above, the industry standard specifications are the best references for this type of tests. Below is a table of recommended test conditions for each board level reliability test.

Board Level Temperature Test Requirements (ED-4702A and IPC-9701)

Factor	Requirements		
	ED-4702A		IPC 9701
Temperature condition (Top – operating temp)	TCA: -30°C ←→ +80°C		TC1: 0°C ←→ +100°C (preferred)
	TCB: -25°C ←→ +125°C		TC2: -25°C ←→ +100°C
	TCC: -40°C ←→ +125°C		TC3: -40°C ←→ +125°C
	TCD: -65°C ←→ +125°C		TC4: -55°C ←→ +125°C
	TCE: Top_{min} ←→ Top_{max} (usually 25°C←→70°C)		TC5: -55°C ←→ +100°C
Duration	5 years equivalent	10 years equivalent	Test until 50% (or 63.2% preferably) cumulative failures on samples or
	TCA: 1217 cyc	TCA: 2433 cyc	200 cycles
	TCB: 435 cyc	TCB: 869 cyc	500 cycles
	TCC: 365 cyc	TCC: 730 cyc	1000 cycles (preferred for TC2, TC3 & TC4)
	TCD: 277 cyc	TCD: 553 cyc	3000 cycles
	TCE: 1825 cyc	TCE: 3650 cyc	6000 cycles (preferred for TC1)

Low Temp Dwell	7 minutes (min)	10 minutes
Temp Tolerance	(+0/-10°C)	+0/-10°C (+0/-5°C)
High Temp Dwell	7 minutes (min)	10 minutes
Temp Tolerance	+10/-0°C (for TCA & TCE) +15/-0°C (for TCB, TCC, & TCD)	+10/-0°C (+5/0°C)
Temp ramp rate	1.5 minutes from low to high temps	≤ 20°C per minute
Sample size	Not indicated	33 component samples (32 for non-rework, 10 for rework, and 1 for cross-section)
Board Thickness	0.6 – 2.4mm	2.35mm – 3.15mm (for >40mm package size)
Package/Die Condition	Daisy-Chain	Daisy-chain
Test Monitoring	Continuous for daisy chain, sampling frequency for actual device	Continuous using event detector or data acquisition system
Failure definition	Not indicated	1000 Ohms, 10 events, 1 microsec duration for event detector, 20% resistance increase, 5 readings per scan for Data logger

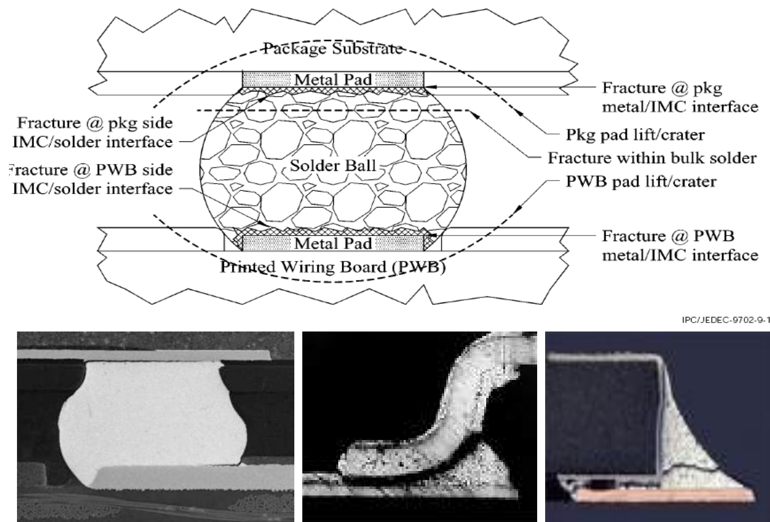
Board Level Bend Test Requirements (IPC-9702 and JESD22-B113)

Factor	Requirements	
	IPC-9702	JESD22-B113
Anvil/roller radius	3mm	3mm
Anvil/roller length	> board width	> board width
Anvil/roller support span	Not indicated	110mm
Anvil/roller load span	Not indicated	75mm
Load anvil/roller vertical displacement	Not indicated	2-4mm
Temp	23 ± 2°C	Room temp
Board thickness (a = package size)	(a <15mm) – 1mm	1mm nominal
	(15 < a < 40mm) – 1.55mm	
	(a > 40mm) – 2.35mm	
Sample size per board (a = package size)	(a < 15mm) - 15 units (3x5)	9 units (3x3) – Applied for 15x15mm max package size only
	(a > 15mm) – 4 units (2x2)	
Symmetry	Symmetrical on midspan of board's longitudinal axis	Symmetrical on midspan of board's longitudinal axis
Package-to-package spacing (a = length of package side parallel to spacing distance)	5mm (from edge of package)	20mm (center-to-center of package)
Package-to-anvil spacing	10mm (from edge of package to center of roller)	Not indicated
Package-to-board spacing	8mm (from edge of package to edge of board)	Not indicated
Package Orientation	Package orthogonal to board and bend fixture	Not indicated
Connector location	Outside of anvil/rollers span	Outside of anvil/rollers span
Failure criteria	20% increase in daisy-chain net resistance	First event of intermittent discontinuity w/ resistance peak greater than threshold value (1000 ohms or 5 times of initial resistance) followed by 9 additional confirmation within 10% of the cycles from first event
Strain Measurement Detector and Continuity Monitoring	500 Hz, 16 bits resolution	30 Hz per channel, capable of 36 channels
Endpoint	Not indicated	60% failures or 200,000 cycles

Board Level Drop Test Requirements (JESD22-B111)

Factor	Requirements	
	ED-4702A	JESD22-B111
Board thickness	0.6 – 2.4mm	1mm
Samples per board and # of boards	Not indicated	15 units (3x5) – 4 boards per side 5 units (2x2) – 4 boards per side
Event Detector	Not indicated	Capable of detecting electrical discontinuity of resistance greater than 1000 Ohms for 1 microsec
Package Size	Not indicated	Maximum of 15x15mm
Board stackup	Not indicated	1+6+1, OSP
Board size	Not indicated	132x77mm
Base Plate standoff	Not indicated	10mm
Drop Condition	30-150cm drop height	1500Gs, 0.5 millisec duration, half-sine pulse (condition B from JESD22-B110)
		Alternative: 2900Gs, 0.3 millisec duration, half-sine pulse (condition B from JESD22-B110)
Orientation	X, y and Z axes	Package oriented on –z axis (device facing down)
Failure Criteria	Not indicated	For event detector: 1st event of intermittent discontinuity followed by 3 additional events after 5 successive drops For data acquisition: 1st indication of resistance 100 Ohms or 20% increase in resistance (for >85 Ohms initial) followed by 3 additional events after 5 successive drops
# of drops	2 per orientation or 10-200 times	30 times or until 80% of samples failed

Typical solder interconnect failures encountered are illustrated below:



5.0 Cypress Board Level Reliability Test Results

Cypress conducted a board level reliability test last 2005 to gather data for 13 selected packages with different leadfinish/solder ball materials. Below is the summary of the test. The test was conducted by Advanced Semiconductor Engineering (ASE) Taiwan.

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Data Collection Matrix – Completed 2005

Package	Die Size	Lead or Solder Ball Finish	Solder paste	Board Level TCT		Drop Test	Bend Test	Shock/ Vibration Test
				Clam Shell Reworked	**Clam Shell Unreworked**			
SSOP 56L		Sn Pb	SnAgCu	5705 cyc	5964 cyc	1st fail 6 drops	50688 cyc	No failures
		NiPdAu	SnAgCu	Passed 6000 cyc	Passed 6000 cyc	Passed 100 Drops	43468 cyc	No failures
		Pure Tin	SnAgCu	Passed 6000 cyc	2289 cyc	Passed 100 Drops	9942 cyc	No failures
TSSOP 28L		Sn Pb	SnAgCu	5727 cyc	3517 cyc	Passed 100 Drops	2232 cyc	No failures
		Pure Tin	SnAgCu	Passed 6000 cyc	Passed 6000 cyc	Passed 100 Drops	2228 cyc	No failures
TSOPII 44L		Sn Pb	SnAgCu	3584 cyc	1426 cyc	Passed 100 Drops	1438 cyc	No failures
		NiPdAu	SnAgCu	Passed 6000 cyc	3478 cyc	1st fail 28 drops	8878 cyc	No failures
		Pure Tin	SnAgCu	2014 cyc	1228 cyc	1st fail 82 drops	2760 cyc	No failures
SOJ 44L		Sn Pb	SnAgCu	4533 cyc	4370 cyc	Passed 100 Drops	65954 cyc	No failures
		NiPdAu	SnAgCu	Passed 6000 cyc	4208 cyc	1st fail 71 drops	83484 cyc	No failures
TQFP 176L		Sn Pb	SnAgCu	4801 cyc	5177 cyc	Passed 100 Drops	66 cyc	No failures
		Pure Tin (Grp 2 & 3)	SnAgCu	2622 cyc	1387 cyc	1st fail 29 drops	162 cyc	No failures
QFN 56L		Sn Pb	SnAgCu	2449 cyc	1097 cyc	Passed 100 Drops	11166 cyc	No failures
		Pure Tin	SnAgCu	Passed 6000 cyc	2730 cyc	Passed 100 Drops	13772 cyc	No failures
		NiPdAu	SnAgCu	3307 cyc	3072 cyc	Passed 100 Drops	12828 cyc	No failures
L2 BGA 31x31		Sn Pb	SnAgCu	Passed 6000 cyc	5963 cyc	1st fail 68 drops	4828 cyc	No failures
		SnAgCu	SnAgCu	Passed 6000 cyc	Passed 6000 cyc	1st fail 85 drops	1672 cyc	No failures
PBGA 35x35		Sn Pb	SnAgCu	4997 cyc	Passed 6000 cyc	1st fail 93 drops	44152 cyc	No failures
		SnAgCu	SnAgCu	Passed 6000 cyc	Passed 6000 cyc	1st fail 4 drops	44190 cyc	No failures
FBGA 23x23		Sn Pb	SnAgCu	4497 cyc	2692 cyc	Passed 100 Drops	116 cyc	No failures
		SnAgCu	SnAgCu	Passed 6000 cyc	Passed 6000 cyc	1st fail 50 drops	60 cyc	No failures
FBGA 15x17		Sn Pb	SnAgCu	3374 cyc	3616 cyc	1st fail 38 drops	1302 cyc	No failures
		SnAgCu	SnAgCu	2358 cyc	1026 cyc	1st fail 24 drops	1724 cyc	No failures
FBGA 14x22		Sn Pb	SnAgCu	1963 cyc	1633 cyc	1st fail 77 drops	6458 cyc	No failures
		SnAgCu	SnAgCu	1964 cyc	1026 cyc	1st fail 6 drops	2252 cyc	No failures
FBGA 6x8		Sn Pb	SnAgCu	3092 cyc	3753 cyc	1st fail 34 drops	108136 cyc	No failures
		SnAgCu (Grp 2 & 3)	SnAgCu	Passed 6000 cyc	2289 cyc	1st fail 27 drops	1576 cyc	No failures
FBGA 7x8.5		Sn Pb	SnAgCu	1968 cyc	1270 cyc	Passed 100 Drops	30656 cyc	No failures
		SnAgCu (Grp 2 & 3)	SnAgCu	4589 cyc	2289 cyc	Passed 100 Drops	4400 cyc	No failures

Cypress conducted additional board level temperature cycle testing per the IPC Standard 9701 from 2010 to present. Below is the summary of the latest test results. The test was conducted by Integrated Service Technology (IST) Taiwan.

Temperature Cycle Data Collection Matrix: 2010-2012

Package	Die Size (mils)	Lead or Solder Ball Finish	Solder paste	Board Level TCT / Condition, 0 to 100C (cycles)					
				Single Side			Clam Shell		
				First Fail	Characteristic Life	Weibull Shape Parameter	First Fail	Characteristic Life	Weibull Shape Parameter
165 FBGA 15x17x1.4mm	263 x 699	Sn62Pb36 Ag2	Sn63 Pb37	2488	8579	3.04	1425	3595	4.55
165 FBGA 15x17x1.4mm	330 x 362	Sn95.5Ag4 Cu0.5	Sn96.5 Ag3 Cu0.5	2118	4659	3.63	1397	2530	5.90
165 FBGA 15x17x1.4mm	330 x 362	Sn62Pb36 Ag2	Sn63 Pb37	NA	NA	NA	2942	4497	9.15
56L QFN 8X8mm	187 x 177	NiPdAu	Sn96.5 Ag3 Cu0.5	2172	3987	4.17	NA	NA	NA
56L QFN 8X8mm	187 x 177	NiPdAu	Sn63 Pb37	2524	25555	1.68	920	4900	2.18
121 FBGA 10 x10mm	186 x 208	Sn98.5Ag1 Cu0.5	Sn96.5 Ag3 Cu0.5	1516	2751	5.27	1070	1941	6.46
68L 8 x 8mm	168 x 206	NiPdAu	Sn96.5 Ag3 Cu0.5	3657	6119	6.3	2667	6115	5.2

Questions regarding board level reliability stresses, materials and data should be directed to Cypress Semiconductor by creating a new quality documentation request in the customer “My Case” support system.