AN46860

Schematic Review Checklist for West Bridge® Astoria™

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Related Application Notes: AN49081 AN64465

West Bridge® Astoria™ is a USB and mass storage peripheral control device that contains three main ports: processor interface (P-port), mass storage support (S-port), and USB interface (U-port). This application note discusses the hardware recommendations and guidelines to design a system using Astoria.

1 Introduction

The West Bridge Astoria device is a peripheral controller that supports high-speed USB and mass storage access. This controller provides access from a processor interface and a high-speed USB (HS-USB) interface to peripherals including SD, MMC/MMC+, CE-ATA, SDIO, SLC, and MLC NAND. It supports interleaving accesses between the processor interface, HS-USB, and peripherals. This enables an external processor and an external USB Host to transfer data simultaneously to each other and to the mass storage peripherals. The following sections cover the hardware considerations for designing Astoria into a system.

2 P-Port

1. If operating in the asynchronous mode, CLK is tied LOW through a 10-kΩ resistor. In the synchronous mode, CLK is connected to the incoming signal from the processor interface.
2. In PCRAM and ADM mode, ADV# is tied to a signal on the processor interface that conforms to the timing specified in the CYWB022XX Family: West Bridge: Astoria USB and Mass Storage Peripheral Controller datasheet. If the signal is not available in PCRAM mode, ADV# can be tied to CE# as described in the application note AN13553 - Using Processor Chip Enable as Address Valid Input to Antioch®. However, unlike Antioch, Astoria requires that the ADDR lines be held after ADV deassertion, according to the tADVH parameter in the datasheet.
3. The DRQ status register and DRQ mask register indicate the available endpoints for transfer. They must be accessed even if a DMA or burst operation is not being implemented on the P-port interface. Use the DRQ# or INT# signal to indicate to the processor that at least one of the bits in the DRQ status register is set. If INT# is used, an extra read of the P-port interrupt register is done before the DRQ status register is read. In PNAND mode, R/B is used as an indication of end-point availability and is treated differently in LNA and non-LNA modes.
4. Ensure that the TEST[2:0], A7, A3, and A2 settings are correct for the various P-port interface configurations.
5. It is required that TEST0 be pulled down by default. For test purposes, it is recommended that it be pulled down through its own resistor and that a non-populated resistor pad be added to the board, allowing it to be pulled up if needed.

   Table 1 lists the TEST[2:0] and register settings for P-port interface configurations.

Table 1. P-Port Interface Configuration Options

TEST [2:0]	VMTYPE Field in CY_AN_MEM_P0_VM_SET Register	Interface
000	101	Non-ADM PCRAM
000	111	SRAM
010	X	Extended Interface Mode

Table 2 lists the TEST[2:0] and address pin settings for the extended interface modes.

Table 2. Extended Interface Modes

TEST [2:0]	A7	A3	A2	Interface
010	1	0	0	PNAND Mode—Small Block Device
010	0	0	0	PNAND Mode—Large Block Device
010	1	0	1	Address/Data Bus Multiplexing (ADM)
010	1	1	0	SPI Mode

6. When using extended P-port modes, SCL and SDA (A5 and A6) require external pull-ups. These pull-ups must be separate from other I/Os, even if unused, and cannot be routed to a single pull-up resistor. Shorting these lines results in the bootloader sensing the clock output on its data input line. This causes Astoria to continuously attempt to boot from a nonexistent EEPROM, thereby disallowing firmware load/boot from the processor port. The pull-up resistors' values are determined by the supply voltage, clock speed, and bus capacitance. A typical value for the I^2C pull-up is 2 kΩ. This value is adjusted based on the trace length and board layout conditions. The pull-ups on SDA and SCL are required even if I^2C EEPROM is not used. A low-value resistor can cause overshoot, and a high-value resistor can cause a timing violation, depending on the capacitance on the bus.
7. DACK# is used in conjunction with DRQ#. If INT# is used to indicate that at least one bit is set in the DRQ# register, then DACK# remains unused. DACK# is not required for Astoria to function.
8. INT#, DRQ#, and DACK# are in the GVVDQ power domain. Therefore, pull up the input pin DACK# to GVDDQ using a 10-kΩ resistor, if it is not used.
9. All unused inputs and input or output pins on the P-port are tied to a valid logic level (HIGH for lowest leakage) through a 10-kΩ resistor. Use a single resistor for all unused pins. When pulling HIGH, the unused pins are tied to the appropriate power domain, in this case, PVDDQ or GVDDQ.
10. Refer to the "Pin Assignments" table in the datasheet for more details on the pin configurations for each P-port interface mode and their corresponding power domains.
11. The INT# and DRQ# signals float when Astoria is in the standby state. These signals are active low. As a result, connect a pull-up resistor to these signals to prevent the P-port processor from receiving any false interrupts.
12. In the PNAND interface mode, an external pull-up is not required for the R/B# signal. The R/B# signal is not an open drain or a collector output.
13. The WAKEUP pin should be connected to an externally controllable output (processor GPIO) with a pull-up resistor attached.

3 S-Port

1. Use SD_D[3]/SD2_D[3] or GPIO[0]/GPIO[1] to detect cards on Astoria. If SD_D[3]/SD2_D[3] is used, then it must be pulled down using a 470-kΩ resistor.
2. Treat the SD_CLK signal as a high-speed signal switching at a maximum of 48 MHz to determine the appropriate signal integrity precautions.
3. If you are designing an application supporting SD/MMC and CE-ATA, follow the trace length restrictions.

   Table 3 lists acceptable frequencies for Astoria, and the maximum trace lengths corresponding to the frequencies for SD cards that cannot operate in high-speed mode.

Table 3. Frequency Versus Trace Length (SD Default Mode)

SDFREQ (MHz)	Maximum Trace Length (in.)
24.00	1.94
21.82	7.55
20.00	13.17
18.46	18.78
17.14	24.4

Table 4 lists the acceptable frequencies for Astoria and the corresponding maximum trace lengths for SD cards that are capable of operating in high-speed mode.

Refer to the “Pin Assignments” table in the datasheet for details on pin configurations for each pin in each S-port configuration and their corresponding power domains.

Table 4. Frequency Versus Trace Length (SD High-Speed Mode)

SDFREQ (MHz)	Maximum Trace Length (in)
48.00	8.18
40.00	20.66
34.29	33.13
30.00	45.61
26.67	58.08

4. All unused inputs and input/output pins on the S-port are tied to a valid logic level (HIGH for lowest leakage) through a 10-kΩ resistor. Use a single resistor for all unused pins. When pulling HIGH, the unused pins are tied to the appropriate power domain, in this case, SSVDDQ, SNVDDQ, or GVDDQ.
5. The pull-up resistor (Rp) used for NAND_R/B# varies from 1 kΩ to 10 kΩ based on the timing requirements and the manufacturer of the NAND device.
6. The SD_POW signal floats when Astoria is in the standby state. If this signal is used to control power to the SD card through an external switch, a pull-up or pull-down resistor must be connected on SD_POW such that the switch remains ON and power to the card is retained during the standby condition.
7. The SD_CMD and used SD_DAT lines each require 10-kΩ to 100-kΩ pull-ups, as specified in the SD Physical Layer Specification. Cypress recommends the use of 10-kΩ resistors.

4 U-Port

1. To avoid an impedance mismatch, lay out the USB differential signals (D+ and D-) with constant spacing and on one plane. Avoid vias and stubs. It is prudent to lay out the signals before laying out the rest of the board.
2. Minimize the trace lengths between the D+ and D– pins on Astoria and the USB connector.
3. If unused, leave the SWD+/SWD– lines floating or pulled low. A high on these lines may cause the USB to overlook detection in the system.

For further information, refer to the Cypress application note, AN70707 – EZ-USB® FX3™/FX3S™ Hardware Design Guidelines and Schematic Checklist.

5 Clocks

1. Ensure that the XTALSLC[1:0] pin levels correspond to the frequency of the signal at XTALIN and XTALOUT.
2. Leave the XTALOUT floating if an external clock source is used.
3. Clock or crystal characteristics must conform to the requirements specified in the datasheet.
4. The design must adhere to the power supply noise specifications for the PLL specified in the datasheet.
5. XVDDQ is the select pin for crystal and clock. XVDDQ must be 3.3 V when using a crystal. XVDDQ must be 1.8 V when using a clock source as an input.

Table 5, Table 6, and Table 7 list the clock selection input settings for the available packages.

Table 5. 100-Pin FVBGA Clock Selection

XTALSLC[1]	XTALSLC[0]	Clock Frequency	Crystal Support
0	0	19.2 MHz	Yes
0	1	24 MHz	Yes
1	0	48 MHz	No
1	1	26 MHz	Yes

Table 6. 81-Pin SP WLCSP Clock Selection

XTALSLC	Clock Frequency	Crystal Support
0	19.2 MHz	No
1	26 MHz	No

Table 7. 81-Pin Lite SP WLCSP Clock Selection

XTALSLC	Clock Frequency	Crystal Support
NA	26 MHz	Yes

6. The Astoria on-chip oscillator circuit requires an external crystal that uses 12-pF load capacitors. Other values of load capacitance in the schematic indicate a crystal outside the Astoria specification for which functionality and crystal lifetime are not guaranteed.

6 Decoupling for Power Supplies

1. VDD requires 2.2-µF and 0.1-µF decoupling.
2. Although AVDDQ is tied to the same supply as VDD, route it separately with 0.01-µF and 0.1-µF capacitors.
3. UVDDQ requires 2.2-µF and 0.1-µF decoupling.
4. GVDDQ, PVDDQ, SSVDDQ, SNVDDQ, and XVDDQ do not have any specific decoupling requirements. Combine them with the decoupling for other supplies at the same level. If in doubt, use 2.2 µF and 0.1 µF.

7 Miscellaneous

All unused output-only pins may be left floating, but do not leave unused input-only and input/output pins floating. Tie the unused input-only and input/output pins to a valid logic level using a single 10-kΩ pull-up resistor. There is a negligible difference when the unused input-only pins are tied HIGH or LOW. For lowest leakage, tie unused input/output pins HIGH.

If standby mode is not used in your design, WAKEUP should be tied HIGH through its own 10-kΩ resistor or through a 10-kΩ resistor shared only with input-only pins. Tying this pin HIGH through a resistor shared with I/O pins can lead to unstable operation.

To prevent a floating GPIO input from resetting the West Bridge inadvertently, it is recommended to place a pull-up on the RESET input line.

Ensure that all unused pins handled in this manner are tied to their corresponding power domain. For example, an unused GPIO[1] is tied HIGH to GVDDQ through a 10-kΩ pull-up, which is shared with other unused signals in the GVDDQ power domain.

Astoria is not hardware backward compatible to Antioch. So, if the system is designed in Antioch, it requires a PCB change when replaced by Astoria.

8 Reference Documents

- AN13553 – Using Processor Chip Enable as Address Valid Input to Antioch
- AN70707 – EZ-USB® FX3™/FX3S™ Hardware Design Guidelines and Schematic Checklist.
- AN42961 – Using a USB Switch with West Bridge Antioch

9 Summary

USB Hi-Speed operation demands careful hardware design to preserve Astoria signal integrity. By following the guidelines in this application note, Astoria-based design has a good chance of first-pass success.

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**	2516790	PRKU	06/16/2008	New application note.
*A	2620808	OSG/AESA	12/12/2008	Numbered the paragraphs for better readability and added another point in both P-port and S-port sections. Changed title to “Schematic Review Checklist for West Bridge® Astoria™”.
*B	2742382	ODC	07/22/2009	Added information on Wakeup pin in the P-Port section.
*C	2912408	ODC	04/13/2010	Added note specifically disallowing the shorting of the SDA and SCL lines.
*D	3087467	ODC	11/16/2010	Added an item in both the Clocks and S-Port sections.
*E	3143367	ODC	01/17/2011	Changed software version to Astoria 1.2.1 SDK In the P-Port section, added item 5 and modified the item on PCRAM and ADM mode In the S-Port section, modified item on SD_CMD and SD_DAT Updated Miscellaneous section Added the Reference Documents section
*F	3172743	ODC	02/14/2011	Added Table 6 and Table 7 and also updated Table 5 in Clocks section. Updated Miscellaneous section.
*G	3629651	AASI	05/28/2012	Ported to current Cypress template. No technical change. Completing sunset review.
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