WHITE PAPER

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Electro-static Discharge (ESD) Tutorial

This note is intended to be a tutorial on the nature and causes of ESD, the magnitude of the problem, factors affecting it, tests for ESD tolerance, handling of devices to protect against ESD events including standards used by Cypress, standards for ESD measurement and system aspects of ESD.

CONTENTS:

1 What is ESD and how is it caused ?

The charge at the surface of any material is generally neutral, i.e. neither positive nor negative, unless some energy is imparted to the surface causing an imbalance of electrons to occur producing a local charge (negative or positive depending on the material). In a conducting material, the electrons have high mobility and the charge will recombine preserving a balanced surface potential. However, in a non-conducting material, a large local charge can build up in the material until it is discharged via an external path; this is electro-static discharge and can be in the thousands of volts.

1.1 How does charge buildup ?

Charge builds up through energy being imparted to the material, this can happen either via mechanical means (other materials and surfaces in direct contact, rubbing or sliding against other materials) or through charge induced through external high fields. Note that the charge will eventually leak away but does so very slowly for insulating materials and very quickly for conducting materials.

This form of charge generation is called triboelectricity (literally, rubbing electricity). Materials can take on either positive or negative charges depending on their molecular structure. Many experiments have been performed to classify materials according to their triboelectric properties and these are generally listed in the form of a triboelectric series starting with the material with the greatest positive voltage buildup (shortage of electrons) to the material with the greatest negative voltage buildup (excess of electrons). One such Table is shown below:

CHARGE	MATERIAL
More Positive (+++)	Dry Air
	Bakelite
	Glass
	Mica
	Human Hair
	Silk
	Nylon
	Wool
	Fur
	Paper, cotton, wood
	Rayons
	Polyester
More Negative (---)	Celluloid, Silicon, Teflon

These tables are generally composites of many tables published and are not precise with respect to ranking. What can be said is that the further apart materials are on the triboelectric scale, the greater the charge difference between them and the discharge potential.

1.2 How does charge equalize ?

In a conductor charge recombines quickly within the material resulting in a uniform charge level across the surface, in an insulator this takes a lot longer and the locally high charge will discharge either via a contact discharge or through arcing depending on the electro-static field gradient. This energy is what can cause damage to materials if not properly managed. As an example (ref. 1), Charge induced by someone walking on a vinyl (insulating) floor wearing leather shoes can take several minutes to decay from a walking-generated voltage of 500V whereas the charge lifetime is on the order of 10 to 20 seconds for a conductive floor.

2 How high can the ESD voltage get ?

ESD voltages can easily reach thousands of volts. In dry air, voltages of over 25kV have been recorded generated by human beings wearing nylon clothes and rubbing against polyester materials (in a car for instance). Wearing cotton clothes and sitting on a vinyl seat can generate

10kV. For poor conductors such as normal clothing materials, this charge will stick around until discharged, generally to ground. Of course, it is not necessary for a human being to be part of the charge build-up, objects rubbing against each other in a dry atmosphere can also build up charges of this magnitude.

2.1 Material ohmic properties

Materials that are conductive will "self-recombine" quickly in response to a tribo-electricity generating event, restoring surface charge to its neutral state. This also limits ESD voltage build-up in the first place since there is a current flow which reduces the peak voltage. Materials are broadly classified[1] into different ESD handling categories as below depending on their sheet resistivity in ohms per square.

Sheet Resistivity (ρ in ohms/square)	Classification
$> 10^{12}$	Insulator; Static-generating material
$10^{9} < > 10^{12}$	Anti-static; slowly dissipative
$10^{6} < > 10^{9}$	Anti-static; dissipative of charge
$< 10^{6}$	Conductor; rapid charge recombination

2.2 Anti-static and dissipative materials

Materials used in manufacturing environments are mostly of the Anti-static and dissipative kind; this limits ESD voltage build-up while restricting the flow of very high currents between a point charged to thousands of volts and ground that might happen if the impedances were very low; peak currents for such an event can cause considerable damage.

As an example of the effectiveness of anti-static materials (ref.1, adapted from 3M Static Products Documentation), the following table shows the typical range of static voltage generated in low-humidity conditions by walking on various floor coverings:

Floor Covering Material	**Voltage built up by walking**
Regular nylon	> 10 kV
Acrylic and polyester	> 7 kV
Vinyl asbestos tile	> 4 kV
Anti-static nylon	< 4 kV
High pressure Laminate	> 2kV
"Compu-Carpet"; anti-static	< 2 kV

2.3 Human beings and charge generation

Human beings are very good at charge generation because they are relative insulators and are mobile and touch a lot of surfaces generating a lot of static electricity. Every time we walk, we generate some electricity which is then discharged to ground. Discharge of less than 1500-2000 V are generally not felt by a person(ref. 1). In a literal step function, charge can build up every step by just walking (ref. 2) and the equation is $\Delta V/\Delta t = n.\Delta q/C$ where n is the number of steps/second (generally about 2) and C is the person's capacitance (typically less than 150pF). For a typical case on an insulating floor, an experiment (ref. 2) showed a ΔV increase of 300V per human step reaching about 3 kV in 10 seconds (some charge leakage occurs).

The peak voltage is limited to about 30 to 35 kV because, above approximately about 25 kV, the charge will start to bleed off via a corona effect (next time you see someone who is glowing, see what they're walking in and on). Human capacitance will not drop below 30 to 40 pF (ref. 1). Since $I = Q/\Delta t$, such high voltages can result in current discharge values of around a hundred amperes (limited by path impedance) for a time period generally in the tens of nanoseconds range.

3 Relative Humidity and ESD

One of the major factors controlling ESD voltage build-up is relative humidity. The rate of infant mortality for ICs goes up during winter and spring seasons (ref. 1). This happens because moisture content in the air creates a relatively conductive (less than 10^9 ohms/square) surface film which acts as dissipative, if this moisture content is reduced then the air by being dry acts as part of the electrostatic build-up by airflow. Very low humidity is thus an ESD hazard.

3.1 Humidity ranges

Relative humidity is defined as the ratio of water vapour in the air as compared to the saturation amount of water vapour at a given temperature. It is a function of geography and climate. As an example of how relative humidity can vary, afternoon humidity in Phoenix is between 17% to 12% in the months of April to June (ref. 3) while it is between 61% to 64% in New Orleans for the same time period. Indoor heating can also drastically reduce humidity levels by drying the air unless it is humidified.

3.2 Impact of Relative Humidity (RH) on ESD

Looking at the Table in Section 3.2 again, this time at 2 different humidity levels shows a large difference.

Floor Covering Material	**Voltage built up by walking in 20% Relative Humidity**	**Voltage built up by walking in 50% Relative Humidity**
Regular nylon	> 10 kV	< 4 kV
Acrylic and polyester	> 7 kV	< 2 kV
Vinyl asbestos tile	> 4 kV	< 3 kV
Anti-static nylon	< 4 kV	< 1.5 kV
High pressure Laminate	> 2kV	< 2.5 kV
“Compu-Carpet”	< 2 kV	< 1.5 kV

Note that the smallest differences are in the materials that were dissipative in the first place as would be expected. ESD susceptibility is thus reduced considerably. Generally equipment is designed to function over the full range of operational humidity conditions. For a manufacturing area, it is helpful to keep relative humidity above 50%.

4 Effect of ESD events on Semiconductor Devices

ESD events generate high voltages and high currents depending on the path the charge takes to go to ground. If not properly bypassed, the voltages cause immediate oxide dielectric breakdown, specially in advanced geometry technologies with thin gate oxides creating a weak spot in the oxide which allows current flow and localized heating, depending on the current flow this could cause permanent damage caused by overheating and melt the silicon creating a permanent short or high leakage sites. High currents can also cause junction or metal failure. In short, ESD failures can be caused by oxide breakdown, junction burnout or metallization failure due to excess current.

Latent ESD failures are worse, this is where an ESD event damages a device but not to the point where it is detected by testing; the device is weakened and its service life and long term reliability is impacted. There is no known systematic way to screen for such a device and the correct strategy to avoid this situation is to have effective ESD protection.

ESD protection devices are included in most Semiconductor devices to provide protection within a defined range of ESD events. It is assumed that the environment is managed to control the magnitude and duration of ESD events to within the range that protection devices can cope with.

5 ESD Management for Semiconductor Devices

ESD Damage is a very significant issue for Sub-micron semiconductors, the cost of protection and susceptibility to ESD events increases as the feature size gets smaller (ref. 5); both Metal

failure current density and oxide breakdown for a 100ns event are severely impacted making ESD controlled environments essential. Neither reliability nor yield can be guaranteed without stringent ESD controls.

5.1 The 3 phases of a Semiconductor's life

A semiconductor product goes through at least the following 3 phases. Depending on usage in a sub-system or module, there may be more sub-phases and variations on the following. ESD handling requirements at each are different.

5.1.1 At the Semiconductor manufacturer

The semiconductor component is manufactured and tested, generally in both die and packaged form. This is an ESD Controlled environment with strict controls (Cypress Semiconductor has comprehensive state-of-the-art ESD control specifications which are rigorously implemented). ESD Specifications for event severity (voltage, current, time) exist and precautions for managing ESD events are implemented. Outgoing ESD levels are guaranteed by the manufacturer.

5.1.2 In the System manufacturer's facility

The product is built into the System (or sub-system) at this point after arriving at the system manufacturer's site. This must also be an ESD controlled environment with standards that are appropriately selected and enforced. Lack of proper handling at the semiconductor component level will cause both yield and reliability issues. ESD handling and manufacturing standards exist which define both the equipment requirements and the level of ESD protection.

5.1.3 In the hands of the end customer

Until this point, the component has been protected from ESD events beyond a defined level. When the product is sold to the end customer, there is literally an infinity of possibilities ranging from being used in a device like an iPOD which is in a completely uncontrolled environment to being in a board inside a machine that is rarely touched by human hands (although there are ESD considerations here as well). The ESD standards and requirements here are much tougher than the requirements for semiconductors during manufacturing.

5.2 ESD handling in a controlled environment

ESD Protection in a controlled environment is provided by special handling equipment which restricts the level of ESD stress seen by the semiconductor component. The general principle is to understand that charge buildup is unavoidable and to manage both the magnitude of its buildup and the nature of its discharge. Whatever the IC touches must be able to dissipate charge at a rate sufficient to control its peak value and discharge paths must take current values into account; precautions are taken against charge buildup by ionization as well.

5.3 ESD events in an uncontrolled environment

ESD events in an uncontrolled environment (end-user, retail customer, etc.) can be much more damaging and system design must take ESD protection into account. This is usually done through techniques such as ESD protection devices (external devices), PC board layout techniques that attempt to control ESD, and appropriate grounding and shielding techniques

6 ESD Stress Models for Semiconductors in controlled environments

ESD discharges are very different and no model can attempt to replicate all possible current and voltage waveforms caused by a real event. However, over time, standard models have been developed that attempt to simulate typical conditions in controlled ESD conditions and that serve as a basis for standardized testing and comparison.

6.1 Contact and Field-induced discharge models

Separate ESD Stress models are used to test for contact discharge, such as when a charged human being might touch an integrated circuit causing a discharge to ground or when a device

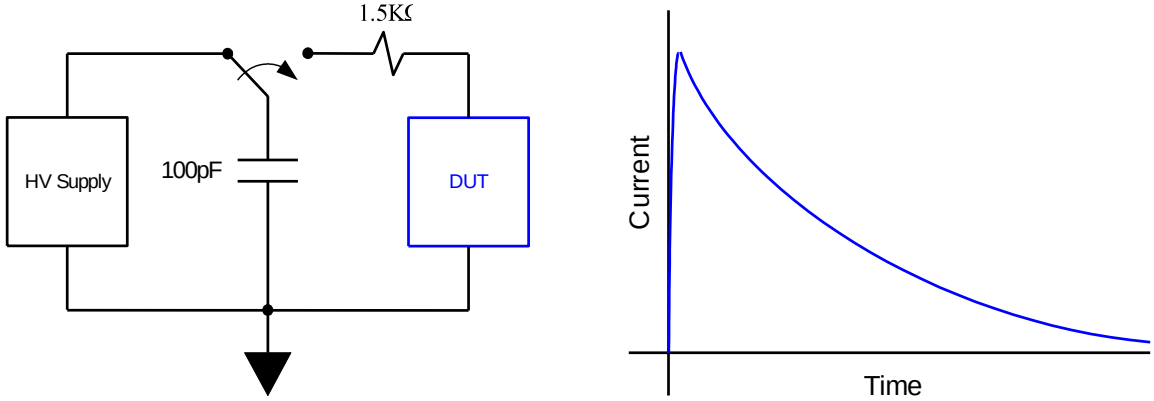
acquires a charge through electrostatic induction or triboelectric process and undergoes a discharge to a grounded surface. The duration and current levels are different for these cases.

6.2 The Human Body Model (HBM) for Contact discharge

The Human Body Model (HBM) type of test was developed a century ago for simulating sparking in mines and ammunition storage areas. It was refined for ESD measurement purposes in the 1960s and 1970s. T. Mazdy of IBM actually found some “fearless volunteers” (ref. 1) who allowed themselves to be charged to a high-voltage power supply and then discharged through a 1 ohm shunt. His studies resulted in the proposal of a simple series R-C network to simulate the discharge from a human body; over time standard values of 1500 ohms for the Resistor and 100 pF for the Capacitor were standardized on.

The HBM model was been standardized as a JEDEC standard and details are available in that document (ref. 6, JESD22-A114D).

The Capacitor is charged up to the voltage to be tested and then discharged through the Resistor in series with the Device Under Test (DUT) as shown in the following figure:



6.2.1 Current and Voltage profile for HBM

While the actual profile will depend on the characteristics of the DUT, Rise time for a low impedance is about 10ns and peak current is simply the peak voltage applied across the 1.5KΩ. Thus, for 1500 V peak, the peak current will be 1 Ampere. Again, in the low impedance case (as would happen with a clamp diode turning on), the duration of the pulse is generally around 1 RC time constant (150 ns) for the current to fall to 37% of its peak value. All pins and combinations of pins are tested this way and the part is tested after HBM to see if any failure modes have developed.

There are JEDEC classifications for devices based on what level of HBM voltage they pass as follows (ref. 6):

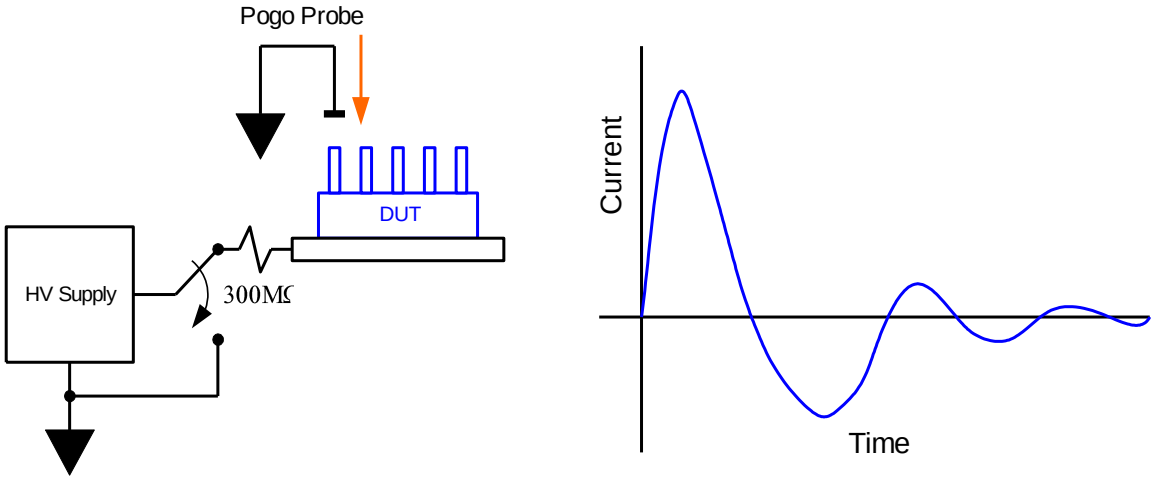
Classification	Requirement
Class 0	Part fails after exposure to an ESD pulse of 250V or less
Class 1A	Passes 250V, fails 500V
Class 1B	Passes 500V, fails 1000V
Class 1C	Passes 1000V, fails 2000V
Class 2	Passes 2000V, fails 4000V
Class 3A	Passes 4000V, fails 8000V
Class 3B	Passes 8000V

Note that while common HBM levels are 1.5 to 2kV, there are many devices (e.g. GaAs RF circuits) that have HBM lower than 500V which are manufactured in very high quantities in everyday products. The key to managing stress here are the ESD handling procedures which

must be suitable for the type of devices being manufactured. And there must be ESD handling procedures in place otherwise most devices will fail in end-user systems.

6.3 The Charged Device Model (CDM)for Field-induced discharge

The CDM test attempts to simulate an ESD event where a device is charged up to a high voltage either through some frictional (triboelectric) process or through electrostatic induction via being in the proximity of a high field and then touches a grounded surface. This test is used to simulate mechanical device handling where devices slide down shipping tubes or test handlers and build up a charge which is subsequently discharged to ground. This is both a more severe test in the sense that mechanical handling is inevitable during assembly and test of most ICs and it would be difficult to get around this test. The following diagram shows a schematic of the test:



The device is charged electrostatically through a dielectric then connected to ground. A probe is used to record the current waveform through the discharge path.

6.3.1 Current and Voltage profile for CDM

CDM currents are much higher than for HBM because there is no current limiting resistor in the path to limit the discharge. Device characteristics determine exact discharge characteristics but, for 500V test voltage, the current waveform rise-time is generally around 400 picoseconds with the peak current around 6 Amperes for a duration of 1.5 to 2 nanoseconds. For 1000V test voltage, the peak current magnitude is around 12 Amperes (the times are about the same).

Recommended levels for CDM testing are 100, 200, 500, 1000, and 2000V. 500V CDM is generally considered fine with good ESD handling procedures.

The CDM test is a JEDEC standard (ref. 7, JESD22-C101C).

6.4 Other Models

Another model that is used in the industry is the Machine Model (MM), it attempts to simulate direct charged device grounding through a capacitive path. Studies (ref. 5) have shown that it is highly correlated to the HBM test and MM behavior can be predicted from HBM levels.

6.5 Actual ESD Failure data and correlation to models

We have seen that ESD levels in uncontrolled environments can reach 30 kV and depend on a host of variables including ground paths, system exposure to ESD voltages, field induced voltages etc. The question is if devices with higher HBM voltages show fewer ESD related returns. Such a study was done in 2007 (ref. 5) by an Industry Council on ESD levels with data from 15 major semiconductor companies (including Intel, Samsung, TI, Freescale, and Renesas). A total of 21 Billion units were considered with specified HBM levels as follows:

HBM Pass level (Volts)	Percentage of 21 Billion population
Pass 500, Fail 1000	24% (4.8 Billion)
Pass 1000, Fail 1500	28% (5.7 billion)
Pass 1500, Fail 2000	4% (0.7 billion)
Pass 2000	44% (9.3 billion)

Field return rates for parts in these categories were then compiled. The results showed that all devices were roughly equal for ESD related returns (less than 1 ppm for this cause over the population) and that the devices which were only guaranteed to pass 500V had the lowest ESD-related return rate (followed by the 2 kV passing parts, then the 1kV passing, and then the 1.5 kV). The conclusion from this (ref. 5) was that field failure rate due to ESD stress is independent of HBM levels over a threshold of 500V.

The Industry Council on ESD (ref. 5) concluded that 500V HBM, based on the returns data, when combined with basic ESD control methods, adequately meets ESD requirements.

6.6 ESD Control in a controlled environment

ESD control is the key to preventing ESD damage to ICs in an ESD controlled environment such as during manufacturing and until shipping out. This is necessary because ESD damage cannot be cured, it can only be prevented. ESD control has evolved as a discipline over the last few decades and the basic principles are to prevent charge build-up beyond control levels and to allow charge to dissipate in a controlled manner.

ESD control starts with examining all phases of handling ICs, both manually and mechanically and providing dissipative paths to contain and discharge static fields. Examples are having dissipative flooring, operators wearing resistive wrist straps connected to designated ESD ground points, workbenches, packaging materials, and garments that are dissipative, ionizing apparatus, ESD meters to monitor fields, and generally considering all sources of charge build-up. Several companies, such as 3M, make anti-static materials and equipment used by the Semiconductor and manufacturing industries.

6.6.1 ANSI/ESD S20.20-2007 for HBM levels > 100V

The American National Standards Institute (ANSI) has published a standard developed by the ESD Association for the development of an ESD control program (ref. 8) for protection of electric and electronic parts; it is designed to provide a safe environment for activities (including manufacturing, handling, and testing) involving components that are “susceptible to damage by electrostatic discharges greater than or equal to 100 volts Human Body Model (HBM)”.

Fundamental principles are providing adequate grounding for materials that conduct charge (dissipative/conductive materials) and ionization systems to neutralize charge in any necessary non-conductors. Anti-static (low charging, dissipative) packaging is also required for transport of materials.

6.6.2 JEDEC Standard 625-A

The JEDEC organization published an earlier standard for “Requirements for handling Electrostatic-Discharge-Sensitive (ESDS) Devices”; JEDEC Standard No. 625-A. This standard is also widely used in industry and says that “ESDS devices with human body model sensitivities of less than +/- 200 volts may need additional protective measures beyond those specified in this standard”.

S20.20 and JEDEC 625-A are major standards in the industry and, provided that ESD handling procedures are in compliance with these, ESD integrity can be assured for HBM levels > 500V.

Cypress complies with both ANSI/ESD S20.20-2007 and JEDEC Standard 625-A.

6.7 Cypress ESD Specifications

Cypress ESD specifications are for devices to pass 2200 V HBM and 500V CDM testing. Cypress ESD handling is rigorous and is based on the S20.20 and JEDEC 625-A standards. Cypress complies with ANSI/ESD S20.20 in its assembly and manufacturing areas and will guarantee ESD integrity for PSoC3 shipments.

Note that ESD handling precautions must be taken in product manufacturing otherwise failures will result with any HBM level. System ESD levels are not a function of HBM and CDM levels and ESD protection at the system level must be provided if compliance with IEC 61000-4-2 is to be guaranteed. No HBM or CDM specification will protect against System ESD events.

Cypress will assure outgoing shipment of product with no ESD damage with specifications of 500V HBM for any case where that is specified.

7 ESD Stress model in an uncontrolled environment

Once a system is manufactured using ICs and other electronic components, it is sold to the end user where ESD control is not guaranteed or mandated. Examples of products such as cell phones and PCs can be subjected to all kinds of ESD stress. This is a System level ESD environment where no assumptions can be made about user handling. The environment is uncontrolled and charging levels beyond 10 kV are possible (ref. 5). ESD stresses at the system level (IEC standard) are very different, and much tougher, and there is no strict correlation between IC level ESD protection and System level ESD robustness.

At the System level, the designer has to think in terms of protection of components on a PC Board and not rely on IC level protection which is greatly inadequate; pulse energies can be orders of magnitude higher in System ESD events. Generally, means such as Transient Voltage Suppression (TVS) diodes are used to protect components by shunting ESD pulses to power supply rails.

Case studies have been performed (ref. 5) to study correlation of HBM pass levels to System level ESD (IEC Standard 61000-4-2) testing; as with the study on returns, no correlation was found between HBM level and System ESD performance with devices having 500V performance in systems that passed IEC System level tests and devices with 2 kV HBM performance failing IEC level tests. The conclusion here was that System level ESD is uncorrelated to HBM levels above 500V.

7.1 The IEC 61000-4-2 model

The IEC 61000-4-2 model specifies a stress test for “electrical and electronic equipment subjected to static electricity discharges, from operators, and to adjacent objects” (ref. 9). No assumptions are made about the environment or ESD control.

Stresses are much higher than for the HBM and CDM model and the protection provided by HBM and CDM circuitry cannot be relied on to survive System ESD stress.

7.1.1 Contact and Arc discharge models

At a system level, discharge can occur via a spark ending on a product or as contact discharge. Both models are specified in IEC 61000-4-2.

7.1.2 Current and Voltage profile for IEC 61000-4-2

The Contact discharge model for IEC specifies an 8kV initial stress with a peak current of 30 Amperes for a time of less than 1 nanosecond, the current then declines to 16A at 30 nanoseconds and to 8A at 60 nanoseconds. External surge absorber diodes are commonly used to protect ICs from this pulse; however (ref. 5) it must be ensured that the clamp level of the external protection diode is not so high that the device being protected sustains damage anyway; this is because the Contact discharge waveform persists for a time approximately equal to that of the HBM stress (circa 150 nanoseconds).

The Arc discharge model requires the device to withstand a 15 kV discharge but, because of the large differences in arcing possibilities, no current waveform is specified.

7.1.3 External protection

Searching for “ESD protection diodes” will show a large variety of products which are guaranteed to pass IEC 61000-4-2 stress. It is important to understand what voltage they clamp to when undergoing an ESD stress to see what the impact might be on the protected device. Sometimes series resistors are required to protect the IC. For device inputs that users can touch, typically communication peripherals such as USB, Ethernet, Firewire, RS-232, Cell phone interfaces, PC Video connectors, etc. these diodes (often called Transient Voltage Suppressors, or TVS diodes) are required.

8 ESD Protection of Systems

Reference 1 (see reference list) addresses Design for ESD Immunity very comprehensively. There is a huge variation in systems and stresses they might encounter, including the fact that electro-magnetic interference might also be created by ESD events (high currents running through conductors to ground). Some important principles can be cited in spite of the huge variation possible.

8.1 General principles

Basic principles are to understand the nature of ESD stresses and to anticipate sources of ESD voltage and manage the discharge of associated energy. Note that in a system in the field, it is entirely possible to have an ESD event while the system is powered and operational (unlike HBM and CDM testing which is done in the unpowered state).

8.1.1 Grounding

This is critical for ESD events. Grounding strategy is affected by enclosures and how they are grounded as well. A Board enclosed in a shielded enclosure is protected from contact discharge events but the system must be designed properly to avoid inductive charging, ESD is a very high bandwidth event (300 MHz to 1 GHz region) and inductive RF effects must also be considered.

It is not always desirable to have the System board be connected to a chassis if the chassis ground has a lot of current and noise and there is the potential for ground loops. In this case, since ESD is basically an RF event, a virtual ground to the chassis can be provided by using a high voltage capacitor of a few nano-farads (example, 4.7 nF 250 VAC in parallel with 1 Meg-ohm resistor); this capacitor will virtually connect the two grounds for the duration of the ESD event (impedance about 0.1 ohm for 300 MHz).

8.1.1.1 PC Board layout and design

The PC Board design is the area where the biggest ESD protection opportunities exist and, conversely, a poorly designed PC Board will be more susceptible to ESD events. Some key design techniques (ref. 1 and other references cited within it) are:
- Provide a solid (as much as possible) ground plane in the PCB; the idea is to provide minimum impedance to ground (no long traces to a ground point).
- Decoupling capacitors should be located very close to the ICs.
- Use a ground ring around the edge of the PCB and keep critical traces away from the board edges.
- Shield (assuming the shield can be connected to the same ground as the PCB) incoming cables. Flat cables with shielding have show orders of magnitude better ESD performance
- Filter incoming lines if possible (while keeping data rates in mind). Capacitors in the 20 to 60 pF range allow signal bandwidths of about 50 MHz (ref. 1).

8.1.2 Software techniques

System ESD events can occur at any time and the resulting disturbance, both electrical and electro-magnetic can result in internal nodes, such as SRAM cells, or flip-flops being disturbed if the impulse is large enough and the System design is not effective at preventing this. This can

cause code or data values to be corrupted inside, say, a Microcontroller. Defensive coding can try to compensate for such possibilities. Basic techniques are:

- Use of Watchdog timer: This can catch stack corruption or PC errors.
- Fill unused memory with NOPs or Software Reset instructions (if available).
- For configurable parts, reconfigure the part frequently in order to reload the configuration (if stored in volatile storage).
- Always use CRC or some form of data packet integrity checking to find transient errors in data streams.
- Use external watchdog circuits as an extra layer of protection where extreme reliability is required.
- Periodic Resetting of the device, to restore configuration and re-initialize registers, is useful when possible.

Note that these techniques are trying to use the chip to guard against an unknown hardware failure in the chip itself, this should thus never be a primary form of defense but only an added supplemental measure (i.e. the system must be designed with ESD events in mind).

9 System ESD protection for PSoC3/5

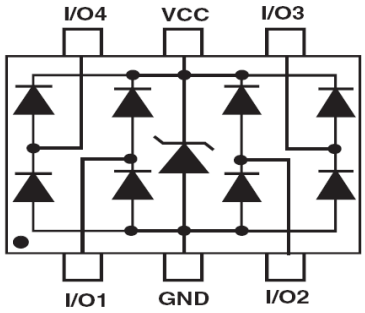
We have seen that ordinary 2 kV HBM will not survive 8 kV System ESD events (besides the voltage levels, the peak current in the former case is 1.3 Amperes peak versus 30 Amperes in the latter). If PSoC3/5 pins are going to need to be exposed to external voltages in a system they need to survive System ESD testing.

9.1 Externally exposed inputs

Inputs that need to survive being plugged and unplugged into a system by a user need to have full 8kV IEC System ESD protection. These inputs are generally communication interfaces such as USB, UARTs, or others depending on the system. They are exposed to uncontrolled ESD environments in a system. Some form of external protection device is required.

9.2 Transient Voltage Suppressors

Transient Voltage Suppressors (TVS) devices are commonly used as protection against System ESD events. They are made by many companies as a web search will show. An example of a TVS device that can protect 4 pins is shown below:



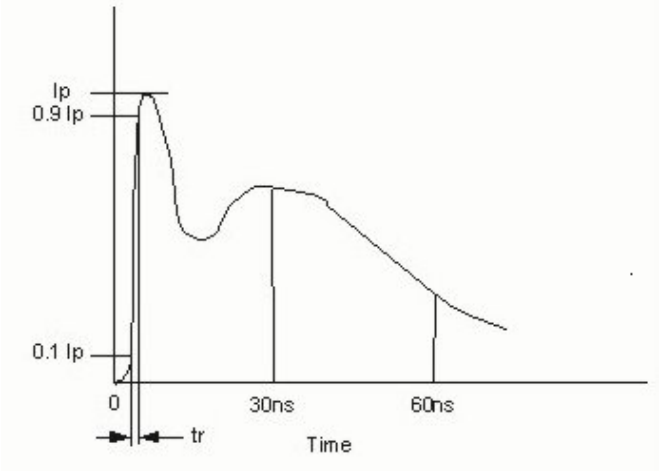
The diodes provide clamping to the rails as well as reverse breakdown protection. They are not intended to operate in the forward current mode except transiently.

When an ESD event occurs the diode will breakdown (Zener voltage breakdown) and conduct significant amounts of current (30 A peak). The voltage across the diode will be equal to its breakdown voltage plus the voltage drop caused by the current flow through its dynamic resistance. The system designer needs to make sure that the voltage drop across the TVS will not damage the protection circuitry of the IC it is supposed to protect.

9.3 Current limiting with External Surge protectors

A simplified example is worked through in this section (ref. 10 has a very good description of this process).

The waveform of the IEC 61000-4-2 8 kV contact discharge waveform looks like the following:



The peak current value is 30 Amperes, tr is about 1 nanosecond, current at 30ns is about 16 Amperes, and the current at 60ns is about 8 Amperes (from ref. 9) for a range of current.

The IEC discharge value can be split into two regions, initial fast ramp and longer tail, the tail region takes over 150 ns to attenuate to lower levels.

As an approximation, the first region (very sharp peak) is similar to CDM and the second region to HBM (ref. 10).

For a device with 500V CDM and 750V HBM, the peak current for the CDM mode is about 6 Amperes and, for 750V HBM, the peak current is 0.5 Amperes.

The key then is to limit the current in the two regions to 6 Amperes for the earlier part and 0.5 Amperes for the second part to prevent the high System ESD test currents from damaging the part.

Region 1 (HBM approximation): Assuming the break is at 30ns, where the current is about 16 Amperes (per the spec.), the voltage across the TVS will be its breakdown voltage plus the drop across its internal resistance, for the values picked the voltage drop is therefore = 6 + 16*1 = 22 volts. Assuming we do not want the pin voltage to rise above 5V and current flow is to be limited to 0.5A, then a series resistance of (22-5)/0.5 = 34 ohms is required between the TVS and the IC. Note that in practice, there will be higher transient voltage so a safety factor should be used depending on what voltage is taken as the peak in the HBM analogue region (ref. 10 suggests 35V).

Region 2 (CDM approximation): This region is somewhat complicated because the actual voltage rise is more than the simple breakdown voltage plus current-times-resistance equation gives. It is suggested that the waveforms observed be used with the CDM current to calculate the value of the peak voltage which is higher than the ratio of peak-current (30A) to 30ns-current (16A); in the example given (ref. 10), the peak voltage value observed was 90V which is about 2.5 times the value obtained by using the breakdown voltage plus the current times the internal resistance of the diode. Using the given example and limiting the current to 6 Amperes (CDM approximation), we get (90-5)/6 = 14 ohms.

Since the device has to survive both regions we take the higher value of resistance i.e. 34 ohms, with a factor of safety we can call this 50 ohms. Thus, for those outputs that need to be protected against external ESD events, a TVS with the characteristics given above and 50 ohm resistors in series with the I/O pins should serve to protect the pins from System ESD events. Note that this analysis is highly simplified and, in practice, should be verified by measurements and observations of the system.

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