



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Migrating from HX2/HX2LP to HX2VL

Author: Anand Srinivasan

**Associated Part Family: CY7C65640A,
CY7C65630/20, CY7C65642/32/34**

Associated Code Examples: None

Related Application Notes: None

AN69235 is intended to help the developer migrate a hub design based on EZ-USB® HX2 (CY7C65640A) and HX2LP (CY7C65630/20) to use the HX2VL (CY7C65642/32/34) hub. It also provides a feature comparison between HX2, HX2LP, and HX2VL to aid in selecting the appropriate part number for migration. Note that HX2 (TetraHub) is now not recommended for new designs.

1 Introduction

The HX2VL family is the next generation of USB high-speed hubs. This family of hubs includes:

- Four-port hubs:
 - CY7C65632 with a single transaction translator (TT)
 - CY7C65642 with four TTs
- Two-port hub: CY7C65634 with a single TT

The HX2VL family is not pin-compatible with HX2/HX2LP and it consumes less power than HX2/HX2LP. This application note highlights the difference between the products, and aids the designer in migrating existing designs to the HX2VL family.

For designs in which downstream devices are all high-speed or just a single full-speed/low-speed device, the performance of single TT and four TTs is the same. For this reason, a single TT hub should be considered for these designs.

Both the HX2LP and HX2 families are 56-pin, QFN packaged parts. The HX2VL family of chips is available in two package options:

- 48-pin TQFP package
- 28-pin QFN package

Both are the same in terms of the core hub functionality. This allows the designer to migrate to an appropriate package based on the requirement. All comments pertaining to HX2VL are applicable to package options. Accordingly, the appropriate part number (CY7C65642 or CY7C65632/34) in the HX2VL family can be chosen for migration.

For more details on HX2VL, refer to the HX2VL datasheet and application note [AN72332 - Guidelines on System Design using Cypress's USB 2.0 Hub \(HX2VL\)](#).

Note In this application note, HX2LP is used to refer to HX2 and HX2LP, except where noted. HX2VL is used to refer to CY7C65642 and CY7C65632/34, except where noted.

2 Hardware Changes

This section presents information on the required changes when using either configuration of the HX2VL chip.

2.1 Changes to the Crystal Specification

When using HX2VL, a primary change required is the crystal. When a crystal is used in the design, the load capacitance of the crystal must change for proper operation. This affects both the load capacitors and the crystal being used. HX2LP uses a crystal with the following specifications:

- 24 MHz \pm 100 ppm
- Parallel resonant
- Fundamental mode
- 500- μ W drive level

HX2 requires a crystal with load capacitors that are between 20 pF and 33 pF (5 percent tolerance). The HX2LP requires a crystal with load capacitors of 12 pF (5 % tolerance).

Following are the specifications for the crystal used with HX2VL:

- 12 MHz \pm 500 ppm
- Parallel resonant
- Fundamental mode
- 600- μ W drive level (maximum)
- 20-pF (5 percent tolerance) load capacitor

These specifications must be considered when selecting both the load capacitors and the crystal. Using a different crystal load capacitance with a crystal specified for 20 pF may affect the frequency shift. The designer should always ensure that the power dissipated by the crystal is within the crystal manufacturer's specifications. Overdriving the crystal may damage it.

HX2VL supports a clock source of 12-, 27-, and 48-MHz oscillators in the 48-pin TQFP package (28-pin QFN part supports only 12 MHz). The frequency tolerance remains the same regardless of the clock source.

2.2 EEPROM

HX2LP supports loading of configuration data from SPI EEPROM. The size of configuration data for HX2LP can be up to 512 bytes.

HX2VL supports loading of configuration data from either I²C EEPROM or SPI EEPROM (only by 48-pin TQFP package). The size of configuration data for HX2VL can be up to 128 bytes. The size and type of EEPROM can be changed based on the requirement.

2.3 Regulator

HX2LP can be powered from a single 3.3-V supply. For a bus-powered design or a self-powered design with a supply other than 3.3 V, this mandates an external regulator.

HX2VL supports a 5-V to 3.3-V internal regulator. For a bus-powered or self-powered design with a 5-V supply, this results in system cost reduction. HX2VL can be powered from a single 3.3-V supply as well. The internal regulator of HX2VL can supply only up to 150 mA. This can be a bottleneck if the output of this regulator is used to supply other components of the design. The regulator configuration can be chosen based on these considerations.

2.4 Pin-strapping

Pin-strapping is the method of configuring HX2VL based on the state of certain pins at power-on reset (POR) or at a strapping period after POR. This is used to configure power management mode (ganged or individual), power enable switch polarity, number of ports, and non-removable port configuration. Through pin-strapping, the 28-pin QFN package supports only power management mode configuration.

3 Features

To understand the trade-offs during migration, [Table 1](#) shows a comparison between HX2, HX2LP, and HX2VL.

Table 1. Feature Comparison between HX2, HX2LP, and HX2VL

Item	HX2	HX2LP	HX2VL (48-pin TQFP Package)	HX2VL (28-pin QFN Package)
Power consumption**	High (460 mA)	Lower than HX2 (231 mA)	Lower than HX2LP (82 mA)	Lower than HX2LP (82 mA)
Bus-powered mode	Not supported	Can support up to three downstream ports	Can support up to four downstream ports	CY7C65632/42 can support up to four downstream ports CY7C65634 can support up to two downstream ports
Power management mode	Yes (EEPROM configuration data)	Yes (EEPROM configuration data)	Yes (pin-strapping GANG pin)	Yes (pin-strapping GANG pin)
Self-powered mode	Yes (SELPWR pin)	Yes (SELPWR pin)	Yes (SELPWR pin)	Yes (SELPWR pin)
VBUS monitoring	Yes (VBUSPOWER pin)	Yes (VBUSPOWER pin)	Yes (RESET# pin)	Yes (RESET# pin)
Multiple TT	Yes	No	Yes for CY7C65642 No for CY7C65632 and CY7C65634	Yes for CY7C65642 No for CY7C65632 and CY7C65634
Number of ports	Yes (EEPROM configuration data)	Yes (EEPROM configuration data)	Yes (pin-strapping SET_PORT_NUMx (x = 1, 2) pins or EEPROM configuration data)	Yes (EEPROM configuration data)
Non-removable port	Yes (EEPROM configuration data)	Yes (EEPROM configuration data)	Yes (pin-strapping FIXED PORTx (x = 1..4) pins or EEPROM configuration data)	Yes (EEPROM configuration data)
Suspend indication	No	No	Yes (GANG pin)	Yes (GANG pin)
EEPROM	SPI	SPI	I ² C and SPI	I ² C
Power enable pin	Yes	Yes	Yes	Yes
LED indicators	Yes	Yes	Yes	No
Modulated indicators	No	Yes	No	No
Power polarity control	No	Yes (EEPROM configuration data)	Yes (pin-strapping PWR_PIN_POL pin)	No
Dual power descriptors	No	Yes	No	No
Multiple string descriptors	No	Yes	No	No

**These are typical values of supply current (I_{cc}) when the device is connected to a high-speed host and all four downstream ports are connected to high-speed peripherals.

4 Summary

This application note discusses the migration of an HX2/HX2LP-based hub design to an HX2VL-based hub design and the considerations associated with the migration.

Document History

Document Title: AN69235 - Migrating from HX2/HX2LP to HX2VL

Document Number: 001-69235

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3237432	AASI	04/21/2011	New application note.
*A	3551005	PDAV	03/15/2012	<p>Included CY7C65634 related information in all instances across the document.</p> <p>Updated Abstract:</p> <p>Updated description.</p> <p>Updated Introduction:</p> <p>Updated description.</p> <p>Updated Hardware Changes:</p> <p>Updated Regulator:</p> <p>Updated description.</p> <p>Updated Features:</p> <p>Updated Table 1:</p> <p>Added values in all columns corresponding to "Power consumption" item.</p> <p>Added a note below the table and referred the note in "Power consumption" item.</p> <p>Replaced "SET_PORT_NUM1 and SET_PORT_NUM2 pins" with "SET_PORT_NUMx (x = 1, 2) pins" in "HX2VL (48-pin TQFP package)" column corresponding to "Number of ports" item.</p> <p>Replaced "SET_PORT_NUM1 and SET_PORT_NUM2 pins" with "FIXED PORTx (x = 1..4) pins" in "HX2VL (48-pin TQFP package)" column corresponding to "Non-removable port" item.</p> <p>Replaced "No" with "Yes" in "HX2VL (28-pin QFN package)" column corresponding to "Power enable pin" item.</p> <p>Updated to new template.</p> <p>Completing Sunset Review.</p>
*B	4764192	PRJI	05/13/2015	<p>Updated Introduction:</p> <p>Removed reference of AN1071 (as it is an obsolete application note).</p> <p>Removed reference of AN69025 (as it is an obsolete application note).</p> <p>Added reference of AN72332 instead of AN69025.</p> <p>Completing Sunset Review.</p>
*C	5792735	RUPA	07/27/2017	Updated Cypress logo and Copyright information.
*D	6199364	HBM	06/06/2018	<p>Updated to new template.</p> <p>Completing Sunset Review.</p>

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Videos](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

EZ-USB is a registered trademark of Cypress Semiconductor Corporation.



Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

© Cypress Semiconductor Corporation, 2011-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.