Application Note Abstract
AN60466 describes the design process to create a dimmable LED driver using the CY8CLEDAC02. Applications for this part include LED replacement lamps, LED ballasts, and LED downlights. Design equations for all key components are given together with a step-by-step guide for using the associated design calculator.

Introduction
The CY8CLEDAC02 can be used to create an offline dimmable LED driver that is compatible with leading edge (or forward phase) and trailing edge (or reverse phase) phase cut wall dimmers. At the heart of the device is a sophisticated digital power controller that uses primary side sensing to implement a fully isolated accurate constant current driver for LEDs. When attached to a standard phase cut wall dimmer, the LED current is a function of the phase cut angle that allows you to dim the LEDs to as low as 2 percent by most standard wall dimmers.

The advantages of a CY8CLEDAC02-based dimmable LED driver include:
- Elimination of opto-isolators
- Elimination of secondary side control circuitry
- Fully isolated AC to DC constant current driver
- Advanced protection features
- Meets Energy Star requirements for LED lighting
- Reduced component count
- Reduced cost

Design Requirements
Appendix 1 shows the final system schematic. To select component values you need the following information:
- LED current, \( I_{OUT} \)
- LED voltage range, \( V_{OUT(\text{Max})} \) and \( V_{OUT(\text{Min})} \)
- Line voltage and range, \( V_{\text{LINE}}, V_{\text{LINE}(\text{Min})}, V_{\text{LINE}(\text{Max})} \)
- Line frequency and range, \( f_{\text{LINE}}, f_{\text{LINE}(\text{Min})}, f_{\text{LINE}(\text{Max})} \)
- Desired system efficiency, \( \eta \)
- Minimum operating frequency for flyback, \( f_{SW(\text{Max,op})} \)

Bulk Capacitor, C3
Life and size are the dominant factors when selecting the primary side bulk capacitor C3.

Capacitor life is largely driven by ripple current and the resulting self-heating. Since the bulk capacitor is the source of energy for the flyback the ripple current is equal to the input current. Consult the capacitor manufacturer’s documentation to determine the expected life of the chosen capacitor.

The physical size of the capacitor must be considered. Larger values of capacitor are usually physically larger and may not fit in the lamp assembly. Most capacitors are available in various sizes for a given value. Larger sizes usually have lower self-heating and dissipate power better, resulting in longer life. If form factor constraints necessitate, the capacitor may be broken up into several smaller value capacitors that are connected in parallel.

The value of the bulk capacitor affects cycle to cycle peak current with leading edge dimmers and start-up inrush current. A larger value of bulk capacitor will reduce cycle to cycle peak current and improve power factor, but may result in a larger system start-up inrush current. Other elements in the system, such as the bridge diodes and input EMI filter components may limit the start-up inrush current.

Temperature rating of the capacitor must be sufficient. Most LED lamp assemblies will subject the driver electronics to a high ambient temperature due to power dissipation from the LEDs. Usually the bulk capacitor must be rated for 105°C or higher.

Voltage rating of the capacitor must also be sufficient. During line surge conditions the peak bulk capacitor voltage is higher than normal peak of line. For 120 V systems the capacitor must be rated to 250 V or higher and for 230 V systems the capacitor must be rated for 400 V or higher.
Calculate a minimum capacitor value using:

\[
C_{BULK} = \frac{2 \cdot P_{IN} \left( 1 + \frac{1}{2\pi} \sin^{-1}\left( \frac{V_{INDC(Min)}}{\sqrt{2} \cdot V_{LINE(Min)}} \right) \right)}{\left( \sqrt{2} \cdot V_{LINE(Min)} \right)^2 - V_{INDC(Min)}^2 \cdot f_{LINE(Min)}}
\]

where:

- \( P_{IN} \) is the input power,
- \( V_{INDC(Min)} \) is the minimum voltage on the bulk capacitor each ac half cycle,
- \( V_{LINE(Min)} \) is the minimum line input voltage (RMS), and
- \( f_{LINE(Min)} \) is the minimum line frequency.

Ripple voltage for the bulk capacitor is given by \( \sqrt{2} \cdot V_{LINE(Min)} \) - \( V_{INDC(Min)} \). The initial design can target a ripple voltage of 40 V for 120 V systems or 60 V for 230 V systems. Increasing the ripple voltage allows a smaller value capacitor to be used with a lower ESR at the expense of higher stress on the dimmer.

\( P_{IN} \) can be estimated using:

\[
P_{IN} = \frac{I_{OUT} \cdot V_{OUT(Max)}}{\eta}
\]

**Output Capacitor, C10**

The output capacitor filters the pulsed current from the flyback converter to provide a smooth current to the LEDs.

As a general rule, use 1 uF per 10 mA of LED current. Using a total output capacitance of greater than 1 uF for every 5 mA of LED current may trigger the output shorted protection feature during start up and must be avoided.

Electrolytic, ceramic, or a combination of both types of capacitor may be used. If an electrolytic capacitor is used, care must be taken to ensure the ripple current in this capacitor meets the manufacturer’s limits to ensure lifetime targets for the system are met.

If space constraints require, the capacitor may be split into several smaller value capacitors in parallel.

As for the bulk capacitor, temperature rating of this capacitor must be sufficient. Usually this requires it be rated for 105 °C or higher.

**Flyback Transformer, T1**

The CY8CLEDAC02 is used to control an isolated flyback converter. A sophisticated digital controller within the device uses primary side current sensing to accurately regulate LED current and provide output overvoltage protection. Voltage from an auxiliary winding on the transformer provides chip supply voltage, valley mode switching, and output voltage information without the need for an opto-isolator.

The design of the flyback transformer is key to achieving a final system that meets requirements. The complete design of a flyback transformer needs to take into account many items beyond the scope of this document. For those familiar with designing and winding their own transformers, this document enables the number of turns for each of the windings to be calculated. Those not familiar with transformer design can use the following procedure to provide the necessary information to a transformer design company. Cypress reference designs use transformers from Renco Electronics, Epcos, and Würth Electronics Midcom.

**Maximum Secondary Voltage, \( V_{SEC(Max)} \)**

To provide design margin and ensure manufacturability, some headroom must be provided for the transformer output voltage. A 5% or 10% margin is sufficient. Define the maximum voltage on the secondary winding as:

\[
V_{SEC(Max)} = (1 + m_{VSEC}) \cdot V_{OUT(Max)} + V_{DIODE}
\]

Where:

- \( m_{VSEC} \) is design margin = 0.05 (5%) or 0.1 (10%)
- \( V_{DIODE} \) is the forward voltage of the output diode, D7, when current = 0A.

**Operating Maximum Volt-Seconds Limit, \( V_{INTON(Max\_limit)} \)**

The CY8CLEDAC02 device is designed to operate such that maximum \( V_{INTON} \) occurs at minimum input voltage. With minimum input voltage, \( T_{ON} \) is at its maximum, but cannot exceed the internally defined limit of 5.6 μs. Therefore, \( V_{INTON(Max\_limit)} \) can be calculated using:

\[
V_{INTON(Max\_limit)} = V_{INDC(Min)} \times 5.6\mu
\]

**Minimum Operating Frequency, \( f_{SW(Max\_Op)} \)**

Targeting a minimum switching frequency of 40 kHz to 90 kHz gives the highest efficiency and best performance. Higher switching frequencies can result in a smaller transformer but may reduce system efficiency due to core losses and other system-level switching losses.

**Turns Ratio, \( N_{TR} \)**

Turns ratio, \( N_{TR} \), determines the voltage stress seen by the output diode, D7, and flyback FET, Q1. Based on the breakdown voltages of the selected diode and FET, minimum and maximum allowed turns ratio can be determined.

The output diode maximum voltage stress occurs when the flyback FET is on. At this point, the secondary winding voltage is negative while the output capacitor holds the output voltage. DC analysis gives:

\[
V_{R(OutputDiode)} = \frac{\sqrt{2} \cdot V_{LINE(Max)}}{N_{TR}} + V_{SEC(Max)}
\]

where \( V_{LINE(Max)} \) is the maximum line input voltage, and \( V_{R(OutputDiode)} \) is the peak reverse voltage across the output diode.

Including a design margin, \( m_{VRout} \), to allow for switching spikes and re-arranging allows the minimum turns ratio to be determined:

\[
N_{TR(Min)} = \frac{\sqrt{2} \cdot V_{INDC(Max)}}{V_{R_OD} \cdot (1 - m_{VRout}) - V_{SEC(Max)}}
\]
where \( V_{R,op} \) is the reverse voltage rating for the selected output diode.

For the flyback FET, the maximum voltage occurs when the FET turns off. At this point, the drain node rises above the bulk capacitor voltage until the output diode conducts. DC analysis gives:

\[
V_{\text{DRAIN}(\text{peak})} = \sqrt{2} \times V_{\text{INAC(\text{Max})}} + N_{TR} \times V_{\text{SEC(\text{Max})}}
\]

Including a design margin, \( m_{\text{vds}} \) to allow for switching spikes and re-arranging allows the maximum turns ratio to be determined:

\[
N_{TR(\text{Max})} = \frac{V_{DS}}{1 - m_{\text{vds}}} - \sqrt{2} \times V_{\text{INAC(\text{Max})}}
\]

where \( V_{DS} \) is the drain source voltage breakdown rating for the selected flyback FET.

\( N_{TR(\text{Max})} \) may also be limited by the desired switching frequency, \( f_{SW(\text{Max,op})} \). While regulating output current, the device operates in critical discontinuous conduction mode where \( T_{\text{ON}} \) is determined by the primary peak current and \( T_{\text{RESET}} \) is determined by transformer reset time. Since the CY8CLEDAC02 uses valley mode switching:

\[
T_{\text{PERIOD}} = T_{\text{ON}} + T_{\text{RESET}} + T_{\text{VALLEY1}}
\]

Where:

\( T_{\text{VALLEY1}} \) is the time to reach the first valley on the flyback transistor drain node after the transformer resets. \( T_{\text{VALLEY1}} \) varies based on many factors but for most systems, it is approximately 0.5 µs to 1 µs.

By assuming the volt-seconds for primary and secondary are equal:

\[
T_{\text{ON}} = \frac{V_{\text{IN}} T_{\text{ON(\text{Max})}}}{V_{\text{INDC(\text{Min})}}}
\]

\[
T_{\text{RESET}} = \frac{V_{\text{IN}} T_{\text{ON(\text{Max})}}}{N_{TR} \times V_{\text{SEC(\text{Max})}}}
\]

Assuming critical discontinuous operation with valley switching we get:

\[
T_{\text{PERIOD}} = T_{\text{ON}} + T_{\text{RESET}} + T_{\text{VALLEY1}}
\]

\[
= \frac{V_{\text{IN}} T_{\text{ON(\text{Max})}}}{V_{\text{INDC(\text{Min})}}} + \frac{V_{\text{IN}} T_{\text{ON(\text{Max})}}}{N_{TR} \times V_{\text{SEC(\text{Max})}}} + T_{\text{VALLEY1}}
\]

Re-arranging, using chip limit of \( V_{\text{IN}} T_{\text{ON(\text{Max,limit})}} \) and substituting operating frequency \( f_{SW(\text{Max,op})} \) for \( \frac{1}{T_{\text{PERIOD}}} \) allows \( N_{TR(\text{Max,\text{fsw}})} \), maximum turns ratio, to be determined:

\[
N_{TR(\text{Max,\text{fsw}})} = \frac{1}{f_{SW(\text{Max,op})}} \frac{V_{\text{IN}} T_{\text{ON(\text{Max,limit})}}}{V_{\text{INDC(\text{Min})}}} \frac{1}{T_{\text{VALLEY1}}} V_{\text{SEC(\text{Max})}}
\]

The lower value of \( N_{TR(\text{Max})} \) and \( N_{TR(\text{Max,\text{fsw}})} \) should be used as the maximum turns ratio limit.

If the values calculated from the limits above show \( N_{TR(\text{Min})} \) above \( N_{TR(\text{Max})} \) or \( N_{TR(\text{Max,\text{fsw}})} \), then higher rated components or a higher \( f_{SW(\text{Max,op})} \) should be selected.

**Note:** In lower power designs (below 12 W), the boost circuit boosts the bulk cap voltage up to 30 V above peak of line. The value of \( V_{\text{INDC(\text{Max})}} \) used in the above calculations should be increased to allow for this boosted voltage.

Those not familiar with designing transformers may want to stop at this point and hand the design along with this application note to a transformer manufacturer.

Selecting a final value for \( N_{TR} \) requires detailed knowledge of the bobbin and wire gauge used in the final transformer. However, a desired \( N_{TR} \) should be selected and some calculations repeated after the final transformer design is complete.

Any \( N_{TR} \) within the range given by the limits above produces a working system. The optimal value depends on the core selected. A lower \( N_{TR} \) gives a lower primary inductance, which requires a larger gap in the core, possibly reducing efficiency due to fringing effects. This lower inductance may also result in a short \( T_{\text{ON}} \), which can reduce dimming performance due to fidelity issues with the \( ISENSE \) signal. It is recommended to keep \( T_{\text{ON}} \) above 2.5 µs for maximum dimmer performance.

Low \( N_{TR} \) also results in the most number of secondary turns, which may be a problem if triple insulated secondary wire is required to meet primary to secondary isolation requirements.

Increasing \( N_{TR} \) too high may cause problems too. Core gap can become very small and difficult to control. High \( N_{TR} \) may push the design closer the FET drain source breakdown limit requiring a lower primary leakage inductance. A high value of primary inductance may also trigger protection modes and delay system start up.

### Operating \( V_{\text{IN}} T_{\text{ON(\text{Max})}} \)

Re-arranging the equation for \( N_{TR(\text{Max,\text{fsw}})} \) it is possible to calculate the actual operating \( V_{\text{IN}} T_{\text{ON}} \) using selected \( N_{TR} \):

\[
V_{\text{IN}} T_{\text{ON(\text{Max})}} = \frac{1}{f_{SW(\text{Max,op})}} \frac{1}{V_{\text{INDC(\text{Min})}}} + N_{TR} \times V_{\text{SEC(\text{Max})}}
\]

### Recommended Primary Inductance, \( L_{M(\text{Rec})} \)

For an inductor the power is defined as:

\[
P = \frac{1}{2} L \times I^2 \times f
\]

Combining this with the basic inductor volt-seconds equation, \( V \times t = L \times I \) gives:

\[
P = \frac{1}{2} \frac{(V \times t)^2}{L} \times f
\]

Simplifying, re-arranging, and substituting design parameters gives:
Converting to the voltage seen on the ISENSE pin gives:

\[ I_{OUT} = \frac{1}{2} * \frac{V_{ISENSE}}{R_{ISENSE}} * N_{TR} * \frac{T_{RESET}}{T_{PERIOD}} * \eta_{XFMR} \]

Re-arranging this gives the equation for \( R_{ISENSE} \)

\[ R_{ISENSE} = \frac{1}{2} * \frac{N_{TR}}{T_{PERIOD}} * \frac{T_{RESET}}{T_{PERIOD}} * \eta_{XFMR} \]

The CY8CLEDAC02 flyback controller is a peak current mode controller and adjusts \( V_{ISENSE} \) based on measured \( T_{RESET} \) and \( T_{PERIOD} \) to keep the term \( V_{ISENSE} * \frac{T_{RESET}}{T_{PERIOD}} \) constant at 0.7 V (\( K_{CC} \)). The above equation can be re-written as:

\[ R_{ISENSE} = \frac{K_{CC}}{2} * \frac{N_{TR}}{I_{OUT}} * \eta_{XFMR} \]

\( R_{ISENSE} \) is implemented using two parallel resistors, R15 and R16. This allows for very accurate non-standard values of \( R_{ISENSE} \) to be implemented using inexpensive 1% resistors.

The above equations give an estimate for R15 and R16. After the prototype is built, the value of R15 and R16 can be adjusted to match the performance of the actual transformer and system.

To ensure flicker-free operation at all dimming levels a small RC filter is necessary to filter the high-frequency switching noise present in the current sense signal. R14 and C5 provide this filter. Usually R14 is set to 100 Ω and C5 is set to 220 pF. Since the CY8CLEDAC02 uses peak mode current control, this RC filter must not significantly distort the ramping current signal.

A snubber may also be required across the output diode, D7, to minimize steps in the dimming. This snubber prevents ringing that can occur when the flyback FET, Q1, turns on and voltage across D7 suddenly changes.

Note that the FET turn-off delay affects the final peak primary current and, hence, the average output current. Changing components that affect this delay such as the transistor and gate resistor may require the values for R15 and R16 to be adjusted.

**Transformer Core Selection**

Knowing \( f_{SW} \), \( P_{XFMR} \), \( V_{IN(TON)(Max)} \), \( I_{PRI(Max)} \), and form factor it is possible to select a core. It is beyond the scope of this application note to detail the selection process. It is recommended that you work with your preferred transformer manufacturer to determine the most appropriate core.

**Primary Turns, \( N_{PRI} \)**

In the above calculations a range for \( N_{TR} \) was defined. While it is possible to select a required \( N_{TR} \), this may impose unnecessary restriction on the transformer design because both primary and secondary turns must be integers. It is better to select a desired value of \( N_{TR} \) and repeat calculations after the actual value of \( N_{TR} \) is known. In most cases the change in \( N_{TR} \) due to real values for \( N_{PRI} \) and \( N_{SEC} \) does not significantly affect the values determined using the desired \( N_{TR} \).
Two equations are required to determine \(N_{PRI}\), the minimum number of primary turns. First, the core flux density volt-seconds method should be used to determine the steady state minimum number of primary turns:

\[
N_{PRI(VIN_{TON})} = \frac{V_{IN}T_{ON(Max)}}{B_{MAX} * A_e}
\]

\(B_{MAX}\) and \(A_e\) are determined by the core selected.

Second, saturation due to \(I_{PRI(\text{Max})}\) should also be used to calculate minimum number of primary turns:

\[
N_{PRI(IPRI,\text{Max})} = \frac{L_{\text{Rec}}(Max) * I_{PRI(\text{Max})}}{B_{MAX} * A_e}
\]

Since \(I_{PRI(\text{Max})}\) is only reached under dynamic conditions the core can be pushed harder and a higher value of \(B_{MAX}\) can be used in the \(N_{PRI(IPRI,\text{Max})}\) equation to keep the number of primary turns lower.

The largest value of \(N_{PRI(VIN_{TON})}\) and \(N_{PRI(IPRI,\text{Max})}\) should be used to determine the minimum number of primary turns. The actual number of turns must be an integer.

**Secondary Turns, \(N_{SEC}\)**

Based on the desired \(N_{TR}\) a value for \(N_{SEC}\) can be calculated.

\[
N_{SEC} = \frac{N_{PRI}}{N_{TR}}
\]

Note that only whole or half turns are possible. For \(N_{SEC}\) to meet this requirement it may be necessary to adjust \(N_{PRI}\) and/or \(N_{TR}\).

**Auxiliary Turns, \(N_{AUX}\)**

The auxiliary winding provides \(V_{CC}\) for the CY8CLEDAC02 device. The turns ratio between secondary and auxiliary windings determines the voltage on the auxiliary winding. A diode (D6) and a current limiting resistor (R19) connected in series with auxiliary winding reduce the maximum voltage seen on \(V_{CC}\). With maximum output voltage on the secondary, \(V_{CC}\) for the CY8CLEDAC02 must not exceed 16 V.

Zener Z1 provides a voltage clamp at 15 V ensuring the chip \(V_{CC}\) does not reach the 16 V limit. The auxiliary winding must be designed such that \(V_{CC}\) never exceeds this zener voltage. Remember that \(V_{CC}\) charges while the current in the secondary winding is high which results in an increased voltage drop across the output diode. For most diodes, the voltage drop approximately doubles when passing current; therefore, the auxiliary winding turns can be calculated using:

\[
N_{AUX} = \frac{N_{SEC} * (V_{Z1} + V_{D9})}{V_{SEC(Max)} + V_{DIODE}}
\]

where \(V_{Z1}\) is the rated voltage for Z1 (15 V) and \(V_{D9}\) is the forward voltage for D9 (usually 0.7 V). \(N_{AUX}\) must be rounded down to the nearest integer or half turn.

If the voltage provided at the auxiliary winding after D9 does not reach the \(V_{CC}\) under-voltage lockout, \(V_{CCUVL}\) the CY8CLEDAC02 will reset. This limits the minimum LED voltage load that may be attached to the secondary.

\[
V_{OUT(min)} = \frac{N_{SEC} * (V_{CCUVL} + V_{D9})}{N_{AUX}} - V_{DIODE}
\]

**Final Check Of Transformer**

After the actual turns ratio of the transformer is known, some of the previously calculated values should be recalculated using the actual \(N_{TR}\).

First, the \(L_{\text{Rec}}(\text{Max})\) should be recalculated. This value can be used to determine the required core gap and define a manufacturing target for \(L_{M}\).

Either using the manufacturing target or by measuring a finished transformer a value for \(L_{M}\) can be determined.

Finally, \(N_{TR}\) and \(L_{M}\) can be used to recalculate \(I_{PRI(\text{Max})}\).

Next, the actual minimum operating frequency under worst case conditions can be estimated. Starting with the equation for \(L_{\text{Rec}}(\text{Max})\):

\[
L_{\text{Rec}}(\text{Max}) = \frac{V_{IN}T_{ON(Max)}^2 * f_{SW(\text{Max,op})}}{2 * P_{XFMR(\text{Max})}}
\]

Substituting \(L_{M}\) and rearranging gives:

\[
f_{SW(\text{Max,op})} = \frac{2 * L_{M} * P_{XFMR(\text{Max})}}{V_{IN}T_{ON(Max)}^2}
\]

From the equation for \(T_{\text{PERIOD}}\):

\[
T_{\text{PERIOD}} = \frac{V_{IN}T_{ON(Max)}}{V_{INDC(Min)}} + \frac{V_{IN}T_{ON(Max)}}{N_{TR} * V_{SEC(\text{Max})}} + T_{\text{VALLEY1}}
\]

Rearranging gives:

\[
V_{IN}T_{ON(Max)} = \frac{T_{\text{PERIOD}} - T_{\text{VALLEY1}}}{1} \frac{1}{V_{INDC(Min)} + \frac{N_{TR} * V_{SEC(\text{Max})}}{N_{TR} * V_{SEC(\text{Max})}}}
\]

Remembering \(T_{\text{PERIOD}} = \frac{1}{f_{SW}}\) and substituting into the equation for \(f_{SW(\text{Max,op})}\) above gives:

\[
\frac{1}{T_{\text{PERIOD}}} = 2 * P_{XFMR(\text{Max})} * L_{M} \left( \frac{V_{INDC(Min)} + N_{TR} * V_{SEC(\text{Max})}}{T_{\text{PERIOD}} - T_{\text{VALLEY1}}} \right) ^2
\]

Simplifying a little gives:

\[
\frac{(T_{\text{PERIOD}} - T_{\text{VALLEY1}})^2}{T_{\text{PERIOD}}} = 2 * P_{XFMR(\text{Max})} * L_{M} \left( \frac{1}{V_{INDC(Min)}} + \frac{1}{N_{TR} * V_{SEC(\text{Max})}} \right) ^2
\]

This is a quadratic equation and can be solved using standard techniques to give a value for \(T_{\text{PERIOD}}\) and thus \(f_{SW(\text{Max,op})}\). Using this estimated \(f_{SW(\text{Max,op})}\) in previous equations allows actual \(V_{IN}T_{ON(Max)}\) to be determined.
Finally, $B_{\text{MAX}}$ under static and dynamic conditions can also be calculated.

This completes design of the transformer.

**V\text{SENSE} Resistor Divider, R20, R21**

The auxiliary winding voltage provides feedback to the controller that is processed to determine load voltage and transformer reset. R20 and R21 scale the auxiliary winding voltage. C6 provides some filtering of high-frequency noise.

For constant current operation the voltage at V\text{Sense} must be less than V\text{SENSE}NOM. If the voltage at Vsense rises above V\text{SENSE}MAX output overvoltage protection will be triggered and the CY8CLEDAC02 shuts down.

The voltage at V\text{SENSE}, $V_\text{SENSE}$, is determined by:

$$V_{\text{SENSE}} = V_{\text{SEC}} \cdot \frac{N_{\text{AUX}}}{N_{\text{SEC}}} \cdot \frac{R_{21}}{(R_{21} + R_{20})}$$

Rearranging to find the ratio gives:

$$\frac{R_{21}}{(R_{21} + R_{20})} = \frac{V_{\text{SENSE}}}{V_{\text{SEC}}} \cdot \frac{N_{\text{SEC}}}{N_{\text{AUX}}}$$

Rearranging to calculate $R_{20}$ gives:

$$R_{20} = R_{21} \left( \frac{V_{\text{SEC}}}{V_{\text{SENSE}}} \cdot \frac{N_{\text{AUX}}}{N_{\text{SEC}}} - 1 \right)$$

$R_{21}$ can target a value around 2.4 KΩ allowing $R_{20}$ to be calculated by substituting appropriate values for $V_{\text{SENSE}}$ and $V_{\text{SEC}}$.

$$R_{20} = R_{21} \left( \frac{V_{\text{SEC(MAX)}}}{V_{\text{SENSE(NOM)}}} \cdot \frac{N_{\text{AUX}}}{N_{\text{SEC}}} - 1 \right)$$

**$V_{\text{IN}}$ Scaling, R3, R4, R28, R29, C7, Z2**

Vin scaling resistors, $R_3 + R_4 + R_{29}$ must be chosen such that the maximum line rms voltage is scaled to 1 Vrms across the internal 2.5 KΩ Vin resistor, $R_{V\text{IN}}$. When converting the calculated value to a standard value select the closest standard value that is above the calculated value.

For a 230 V line, $\frac{V_{\text{LINE}}}{V_{\text{IN}}} = 0.004$

For a 120 V line, $\frac{V_{\text{LINE}}}{V_{\text{IN}}} = 0.0076$

The basic resistor divider equation applies:

$$V_{\text{IN}} = V_{\text{LINE}} \cdot \frac{R_{V\text{IN}}}{R_3 + R_4 + R_{29} + R_{V\text{IN}}}$$

Rearranging to solve for $R_3$ + $R_4$ gives

$$R_3 + R_4 = \frac{V_{\text{LINE}}}{V_{\text{IN}}} \cdot R_{V\text{IN}} - R_{29} - R_{V\text{IN}}$$

$R_{29}$ must be set to 56 KΩ and $R_{V\text{IN}} = 2.5$ KΩ. Using the scale factors given above, $R_3 + R_4$ can be calculated using:

$$R_3 + R_4 = \frac{2.5}{0.004} - 56 - 2.5 = 567 \text{ KΩ for 230 V line}$$

$R_3 + R_4 = \frac{2.5}{0.004} - 56 - 2.5 = 270 \text{ KΩ for 120 V line}$

A 20 V zener, Z2, and a series 22 KΩ resistor, $R_{28}$, are included with the Vin scaling resistors as shown in the schematic. This provides immunity to line zero crossing distortion.

A filter capacitor, $C_7 = 1 \text{nF}$, is also included to filter any high-frequency noise from the boost and flyback converters.

Two series 1206 or larger resistors, $R_3 + R_4$, must be used to set the scaling of line voltage for the Vin pin. This is necessary to meet working voltage limit of surface mount resistors for systems targeting higher line voltages.

**Fast Start Resistors, R9 + R10**

$R_9$ and $R_{10}$ provide a path to fast charge the Vcc capacitors, $C_9 + C_8$, at power-up. Choosing values that are 1/8 the values of $R_3$ and $R_4$ enable start up in less than 500 ms.

Two series resistors are necessary to meet working voltage requirements for system targeting a line voltage above 140 V.

**Chopper Inductor and Resistors, L3, R5, R6**

The chopper inductor and resistors provide the necessary load to enable phase-cut wall dimmers to operate correctly. They also improve PF when no dimmer is present.

For leading edge triac-based dimmers, the resistors provide the necessary current to latch the triac on. The inductor, operating as a boost converter, provides the necessary hold current to keep the triac conducting until the bulk capacitor charges to peak of line. A side effect of this boost converter is that cycle by cycle peak currents are reduced as the voltage on the bulk capacitor does not droop as much each AC half cycle.

At the end of each half cycle, the resistors provide the necessary load to reset the dimmer’s internal circuitry and ensure correct firing in the next half cycle.

For trailing edge dimmers the inductor operates as a boost converter presenting a load on the dimmer throughout the cycle. This enables reliable detection of the conduction phase of the dimmer as the boost converter pulls the line low when the dimmer turns off during each half cycle.

When no dimmer is present the inductor also operates as a boost converter providing current draw before and after the bulk capacitor peak charging current. This reduces the peak current required to charge the bulk capacitor and provides current draw over a larger portion of each AC half cycle to improve PF.

The selection of values for the chopper components plays a significant role in overall dimmer compatibility. Based upon testing of many makes and models of dimmers, the recommend value of chopper components are:
R5, the chopper resistor = 220 Ω, 2 W
R6, chopper current limit resistor = 47 Ω, 1/2 W
L3, chopper inductor = 1 mH for 100 V systems, 1.2 mH for 120 V systems, 5 mH for 230 V, ISAT >200 mA

Other values may result in acceptable dimmer operation. For those interested in experimenting with other values, here is a brief explanation of the impact of changing these components values.

Overall, the chopper components implement a boost circuit. Although the output of the boost is unmonitored, the energy delivered by the boost circuit is limited so the boost acts as a pseudo voltage follower. Configured correctly, it can never boost the bulk capacitor voltage more than 30 V above peak of line. This is achieved by allowing the boost to enter CCM operation around peak of line. For higher power designs, >12 W, constant current CCM operation may also be entered.

R6 is the source resistor for Q2 and provides a limit to the maximum current in the chopper. This limits the power dissipation in R5 when the boost convert enters constant current CCM operation and during dimmer confirmation cycles at power-up. A current limit of approximately 200 mA is achieved using a 47 Ω resistor. This current value is chosen as it meets the latching current of many triacs commonly used in leading edge dimmers.

Increasing the value of R6 reduces the current limit, reducing power dissipation during constant current CCM operation and dimmer confirmation. However, if it is increased significantly the peak current during constant current CCM operation may be so limited that the power factor is reduced and an insufficient current is available to hold triacs in leading edge dimmers.

R5 is the drain resistor for Q2. This resistor, in combination with R6, provides a resistive load on the dimmer during the dimmer configuration at power-up. During boost operation, this resistor dissipates power based on $I^2R$ – lowering the resistor lowers the power dissipation. Since this resistor acts to dampen oscillations on the drain of Q2, making it too low can compromise EMI. This resistor also helps reduce the power dissipation in Q2 when Q2 limits the boost current.

L3 is the boost inductor. When Q2 is on, L3 current ramps and energy is stored in L3. When Q2 turns off, the voltage across L3 reverses forcing D3 to conduct and discharge the stored energy. Timing for Q2 is determined by the voltage at Vin such that the mean current draw is proportionate to the line voltage improving power factor.

Increasing L3 results in lower peak current and lower average current. This reduces the power factor. It also reduces the current available to hold the triac in leading edge dimmers. Multi-firing of the triac early in the AC half cycle is usually not a problem, but if multi-firing persists through to the peak of line, the bulk capacitor will not be charged for that AC half cycle. This may result DC current draw from the mains, lamp flicker and very high cycle to cycle peak currents, which will stress the dimmers and lamp components.

Note: As mentioned above, the boost circuit output is unmonitored. If non-recommended component values are used, it is important to check that the boost circuit is not allowing the bulk capacitor to charge more than 30 V above the peak line voltage.

Flyback FET Drain Clamp, D4, C4, R11

No transformer is perfect and some primary side leakage inductance will exist. This leakage inductance reacts with the primary side current to produce large voltage spikes on the drain of the flyback FET. Such spikes may not immediately damage the FET, but over time they can lead to early failure of the FET.

Measures must be taken to minimize these voltage spikes to ensure a reliable design.

Adding an RCD clamp limits the voltage spike on the drain at the FET turn off. The energy stored in the leakage inductance is then dissipated over the rest of the switching period. For maximum efficiency the leakage inductance must be minimized.

Final component values for a fully optimized clamp will be determined empirically. Initial values can be determined using energy balance. Energy stored in an inductor is:

$$e = LI^2$$

Energy stored in a capacitor is given by:

$$e = CV^2$$

Defining the voltage across the clamp capacitor just before the FET turns off as $V_{CLAMP(VAI)}$, and the voltage across the clamp capacitor after it has been charged by the leakage inductance as $V_{CLAMP(PK)}$ then the energy balance equation becomes:

$$L_{PRI(LK)} * I_{PRI(MAX)}^2 = C_{CLAMP} * (V_{CLAMP(PK)} - V_{CLAMP(VAI)})^2$$

where:

- $L_{PRI(LK)} = $ Primary leakage inductance;
- $I_{PRI(MAX)} = $ Peak primary current from above
- $C_{CLAMP} = $ Clamp capacitance value, C4.

Rearranging gives:

$$C_4 = \frac{L_{PRI(LK)} * I_{PRI(MAX)}^2}{(V_{CLAMP(PK)} - V_{CLAMP(VAI)})^2}$$

When the FET is off, the secondary voltage is reflected back through the transformer to the primary. The value of $V_{CLAMP(VAI)}$ must not be lower than this reflected voltage $(N_{TR} * V_{SEC(MAX)});$ otherwise significant power dissipation occurs in R11 reducing system efficiency.

The maximum drain voltage seen by the flyback FET can be estimated by:

$$V_{DS(PK)} = V_{BULK(PK)} + V_{CLAMP(PK)}$$

where:

- $V_{BULK(MAX)}$ is the maximum voltage on the bulk capacitor at maximum line voltage.

Rearranging this and substituting into the above equation allows the minimum value for C4 to be determined:
A value significantly above the minimum given above must be chosen. Larger values cost more but clamp the voltage spike better reducing the stress on the FET. Having chosen a value for C4, it is possible to back calculate a value for $V_{CLAMP(Pk)} - V_{CLAMP(Val)}$ to determine the value for the clamp resistor.

R11 must dissipate the power released by the leakage inductance into the clamp, $P_{CLAMP}$:

$$P_{CLAMP} = \frac{1}{2} L_{PRI(Lk)} \cdot I_{PRI(Max)}^2 \cdot f_{SW(Max)}$$

Combining and rearranging gives:

$$R11 = \frac{2 \cdot V_{CLAMP(RMS)}^2}{L_{PRI(Lk)} \cdot I_{PRI(Max)}^2 \cdot f_{SW(Max)}}$$

Determining the exact RMS value of the waveform on C4 is complex but approximating it to a sawtooth waveform is reasonable. Using this assumption, a value for $V_{CLAMP(RMS)}$ can be determined using:

$$V_{CLAMP(RMS)} = \frac{V_{CLAMP(Pk)} - V_{CLAMP(Val)}}{\sqrt{3}} + V_{CLAMP(Val)}$$

Substituting the value of $V_{CLAMP(Pk)} - V_{CLAMP(Val)}$ back calculated from C11 equation gives:

$$V_{CLAMP(RMS)} = \frac{I_{PRI(Max)} \cdot \sqrt{L_{PRI(Pk)}}}{\sqrt{3} \cdot C11} + V_{CLAMP(Val)}$$

As mentioned above, $V_{CLAMP(Val)} > N_{TR} \cdot V_{SEC(Max)}$. The above can be used to estimate initial values, but careful characterization of the first prototypes is necessary to determine the final values.

For D4 the main selection criterion is reverse voltage. This diode sees the same voltage extreme as the flyback FET, Q1, and must have the same or higher voltage rating. Maximum current for this diode is the same as calculated in the Maximum Primary Current, $I_{PRI(Max)}$ section on page 4.

**Flyback FET, Q1**

As detailed in the Flyback FET Drain Clamp, D4, C4, R11 section on page 7, maximum $V_{DS}$ is one of the main criteria for selecting the flyback FET, Q1. The drain voltage seen by this FET is higher than peak line voltage due to the reflection of the output voltage through the transformer and leakage inductance effects.

Peak current capability of Q1 must meet the value given in the Maximum Primary Current, $I_{PRI(Max)}$ section on page 4.

To improve efficiency, a FET with a higher current rating can be chosen. However, higher current rated FETs usually have larger capacitances, which results in higher switching losses. A few FETs may be tried to find a FET that provides maximum efficiency by balancing conduction losses and switching losses.

**Output Diode, D7**

The overall system efficiency and EMI performance can be greatly affected by the characteristics of this diode. Selecting a schottky diode improves efficiency and EMI performance.

Current rating for this diode needs to meet the maximum secondary current given by:

$$I_{SEC(Max)} = I_{PRI(Max)} \cdot N_{TR}$$

Efficiency can be improved by selecting a diode with higher current rating.

Reverse voltage rating is important for the output diode. When the flyback FET is on the DC reverse voltage seen by D7 is:

$$V_{R(OutputDiode)} = \frac{V_{BULK(Max)}}{N_{TR}} + V_{SEC(Max)}$$

Transients increase the actual voltage seen by D7. For initial design, select a diode with a voltage rating at least 30% higher than the value given above.

**EMI Filter, L1, L2, C1, C11, R1, R2**

Sufficient filtering must be included to meet EMI requirements. Adding EMI filtering can have a significant impact on overall system performance, particularly when the system is connected to a dimmer.

The capacitive components within the EMI filter have the maximum effect on performance. To ensure maximum dimmer compatibility keep the total capacitance connected across the input terminals below 22 nF. Using an anti-ladder filter with two 10 nF capacitors and two 4.7 mH inductors usually gives sufficient EMI filtering.

Damping resistors, R1 and R2, must be placed across the EMI filter inductors, L1 and L2, to dampen the self ringing of these inductors. Setting R1 and R2 to 4.7K usually provides sufficient damping.
Using the Calculator

An excel file with the above equations is attached along with this application note.

Cells are color-coded in the calculator with a decode of the color coding given at the top of the calculator. The flow is very similar to that given in this application note. Most users should only enter or edit values on the GUI worksheet. Advanced users can enter values on the calculator worksheet, if desired, although this is not recommended.

First, click on the “Start Over” button at the top of the spreadsheet to clear any values in the transformer design section. Next make sure the “CY8CLEDAC02” device is selected.

Then enter high level system level parameters such as line voltage, frequency, LED voltage and current, and desired operating frequency. Next, decide on the value for ripple voltage on the bulk capacitor. For 120 V designs, 40 V is recommended starting point; for 230 V designs 60 V is the recommended starting point. The value may be adjusted such that the recommended value for C3 is close to available standard value.

Next, select voltage rating of the output diode, D7, and flyback FET, Q1 while viewing NTR(Min) and NTR(Max) cells. Make sure NTR(Min) < NTR(Max) and that the selected devices are readily available from your supplier. fSW(MaxOp) may also need to be increased.

Once NTR(Min) < NTR(Max) the calculator and this application note can be sent to your transformer vendor to complete the transformer design. The other option is to select your desired core and continue to design the transformer in detail by entering the correct Ae.

If you design your own transformer, make sure the NSEC cell is cleared during the initial selection of turns to ensure a correct value of NPRI is displayed. This can be achieved by clicking the “Start Over” button at the top of the worksheet. After a value is entered for NPRI and NSEC, the actual NTR is calculated and used to determine recommended minimum NPRI.

After all sections of the transformer section are entered values for all remaining system components are displayed.

To confirm, the system functions with the lowest LED load ensure cell VLOAD(Floor) is not red.

Summary

Using the above calculations, it is possible to select or design the components necessary to create a working CY8CLEDAC02 system. After a prototype is built, characterization is necessary and some component values will need to be updated.

Components in the schematic for which no calculations are given above do not change.
Appendix 1 – Schematic
Document History

Document Title: CY8CLEDAC02 Design Guidelines – AN60466
Document Number: 001-60466

<table>
<thead>
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<th>Revision</th>
<th>ECN</th>
<th>Orig. of Change</th>
<th>Submission Date</th>
<th>Description of Change</th>
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<td>2898853</td>
<td>VED</td>
<td>03/24/2010</td>
<td>New Spec.</td>
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<td>3122702</td>
<td>BAL</td>
<td>12/29/2010</td>
<td>Updated design flow and calculator.</td>
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<tr>
<td>*B</td>
<td>3262223</td>
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<td>Added recommended min value for Ton, adjusted instructions to match latest version of calculator. Updated calculator to correct minor errors and add option for AC03.</td>
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