Reducing EMI in digital systems through spread spectrum clock generators

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Over the past couple of decades, more and more applications are going digital. Implementation of digital systems is very simple as it is entirely about logic; however, complexity increases exponentially with signal speed, specifically clock synchronization, setup and hold time, jitter, and so on. These problems affect the functionality of not only the individual subsystem but also cause electromagnetic interference (EMI) when high frequency devices are operating in close proximity. Figure 1 shows a typical example of EMI caused by a DVD player on TV reception.

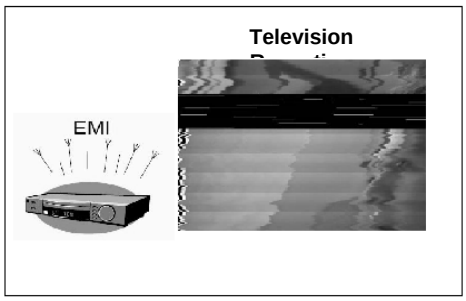

Figure 1: EMI Effect

EMI is an undesirable system response due to either electromagnetic conduction or radiation emitted from an external source. This undesirable response or disturbance may interrupt and degrade the effective performance of any electronic system and might cause a complete system failure. Controlling electromagnetic interference (EMI) in any electronic system, therefore, has become an important design issue for electronic system designers.

Most of the problems faced while designing a digital system are directly or indirectly related to the clock of the system. Being the highest frequency signal, high slew rate and periodic nature (usually 50% duty cycle), clock signals become the largest contributor and primary source of EMI. Furthermore, increasing speed requirements result in radiation with higher electromagnetic energy. To keep control of this radiation, there are several regulatory agencies across the globe which manage various EMI standards to ensure that any electronic equipment does not cause problems to the functioning of other devices. These agencies set the limit on the maximum allowed radiation emission, which may vary from one country to another. Note that the maximum allowed radiation does not refer to the averaged emission but rather to peak emission. Any single frequency violating this limit will cause a device to fail compliance testing.

Multiple ways have been devised to address EMI and reduce radiated emissions. These include shielding, filtering, isolation, ferrite beads, slew-rate control, and good PCB layout using added power layer and ground planes. These methods can be used individually or in conjunction with others. While shielding seems to be a relatively simple approach to reducing EMI, it is a mechanical implementation which is expensive and not at all suitable for portable and handheld equipment. Filtering and low slew-rate may be an effective approach at low frequencies but not at the signal transitions rates being implemented today. Precise PCB layout techniques, for their part, tend to be time consuming and unique to a system, meaning that one kind of layout technique used in a system may not transfer exactly to another system.

Spread spectrum clocking is another method which can be used effectively to bring down EMI radiations. This article specifically discusses how Spread Spectrum Clock Generators can be used to cut down EMI radiations.

SPREAD SPECTRUM CLOCK GENERATORS

With Spread Spectrum Clocking, the concentrated energy of the narrowband clock signal is spread out over a wider bandwidth, reducing the radiated peak emission. Spread spectrum clocking can be visualized as frequency modulation of the input reference clock with controlled frequency deviation (Δf) and modulation rate where the output modulated clock sweeps its frequency repeatedly with time between two fixed frequency points as shown in figure 2.

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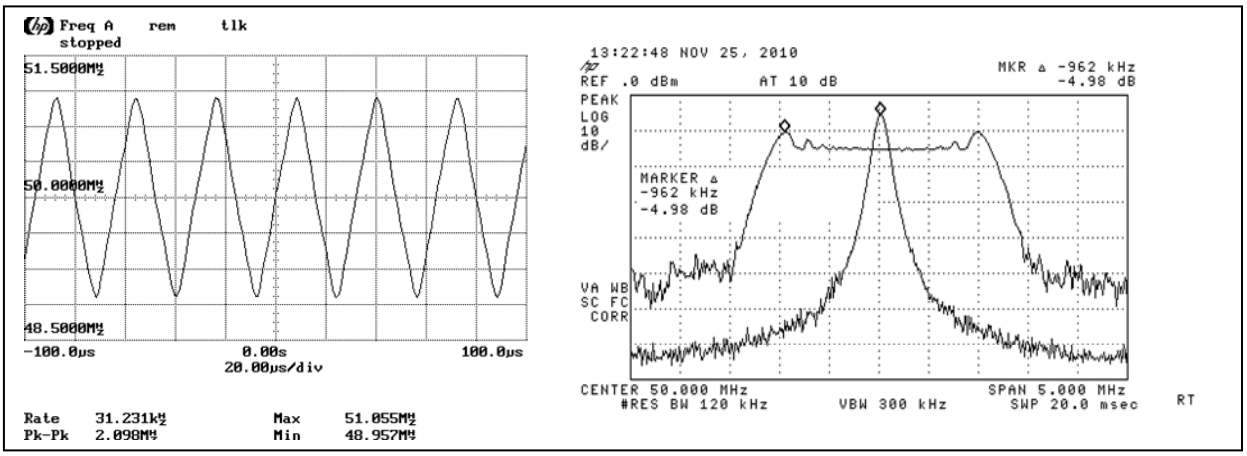


a) Modulated clock signal **b) Output spectrum**

Figure 2: Frequency Modulation of Clock signal and EMI Reduction

Since the total energy contained in the signal remains constant and is distributed over a range of frequencies, the peak emission at any particular frequency is reduced. As the frequency band is made wider, the peak energy is reduced more. A peak EMI reduction of approximately 2dB to 18dB can be achieved using this technique. Such clock generators which generate Spread Spectrum (SS) clock are called *Spread Spectrum Clock Generators (SSCG).*

The biggest advantage of using spread spectrum techniques is that other timing, data, address, and control signals which are commonly synchronized with and derived from the source clock are also modulated, contributing a prominent EMI reduction throughout the system. Low cost and portability between different kinds of systems are some of the major advantages of spread spectrum clocking.

Conventional digital clocks have a very high Q factor which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, resulting in a higher energy peak. When viewed in the frequency domain for spectral density, one can clearly observe a taller narrow peak at the centre frequency and other relatively smaller but again narrow peaks on either side located at the harmonic frequencies.

SSCGs use the approach of reducing the peak energy in the clock by increasing the clock bandwidth and lowering the Q factor. SSCGs take a narrow band digital clock signal to the input and generate an output clock which sweeps between a controlled start and stop frequency at a precise modulation rate. In practical applications, the clock frequency is modulated with a modulation rate of 30 KHz to 120 KHz. This modulation rate is selected such that it stays high above the audio band to avoid any interference with audio frequencies and not cause the system to suffer from any kind of tracking (e.g. setup, hold) problems.

The reduction in EMI is directly proportional to the spread amount of clock. The spread amount is usually quantified in terms of a percentage and is defined as the ratio of difference between the two boundary frequencies (Δf) to the clock target frequency (f_o). Figure 3 shows EMI radiation with different spread amounts.

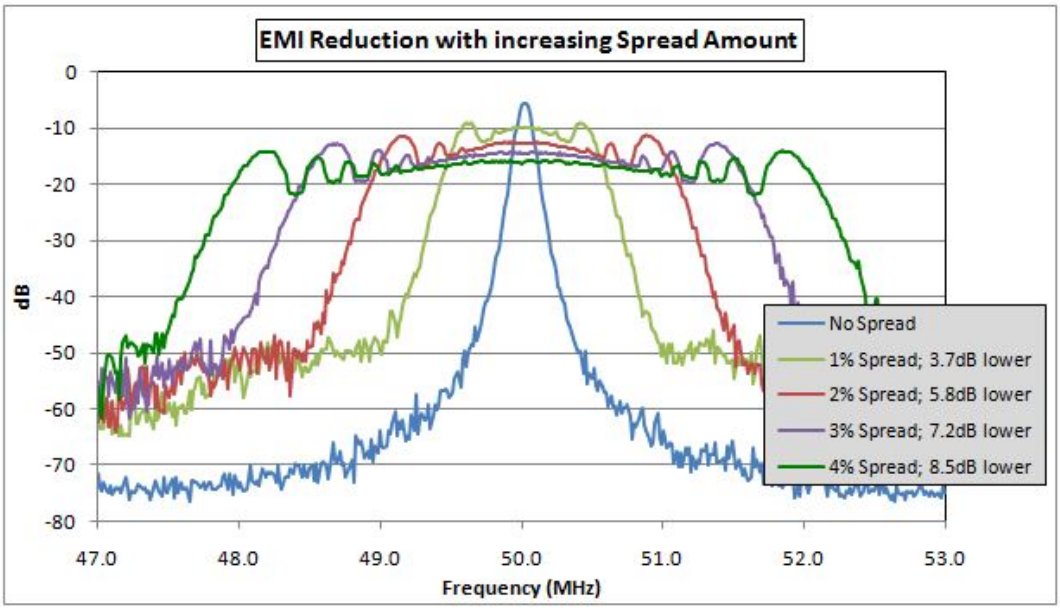


Figure 3: EMI reduction with Increasing Spread amount

In most systems, it is the harmonics of the fundamental frequency which create problems. Fortunately, SSCG reduces EMI not only in the fundamental clock frequency but also attenuates the radiation from harmonic frequencies as well. In fact, the attenuation of peak energy is more prominent at higher order harmonics compared with attenuation at the fundamental frequency. This happens because for a fixed spread amount, the frequency band becomes wider at higher frequency values (i.e. at the harmonics which are just an integer multiplication of the center frequency) hence causing more reduction in radiated energy as depicted by Figure 4.

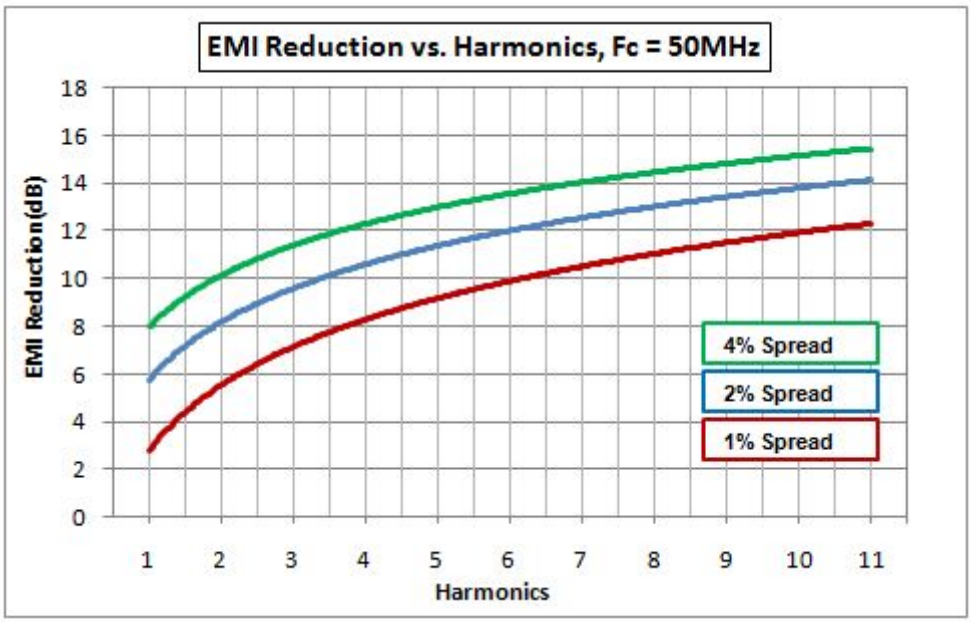
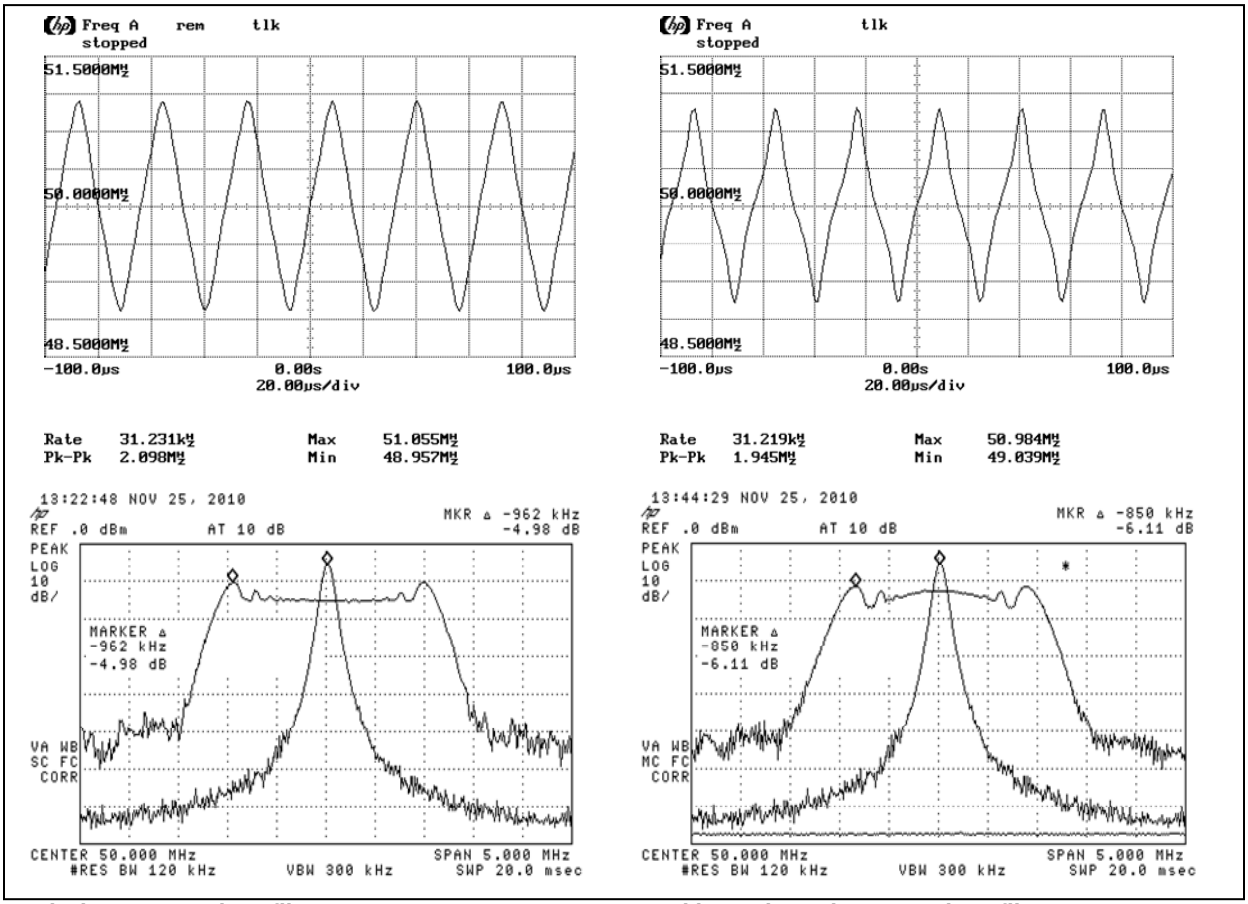


Figure 4: EMI reduction vs. Harmonics

Selection of the spread profile also plays a vital in determining the amount of reduction in peak energy content with SS technique. The spread profile is nothing but the envelope of the frequency variation of modulated signal (spread clock) with

respect to time. A triangular profile is easy to implement from a design point of view but the spectrum produced using this profile exhibits side lobes approximately 1-2dB higher than the center part as shown in Figure 5a. As discussed earlier, a device will fail the EMI standard even if one frequency component falls out of the maximum allowed radition limit. Thus, a triangular spread profile which contains the peak emission in side lobes of the spectrum may violate the spec under certain operating conditions.



a) Linear Spread profile & Output Spectrum

b) Hershey Kiss Spread Profile & Output Spectrum

Figure 5: Comparison between Triangular and Hershey Kiss Spread profiles

An almost flat spectrum can be obtained by with more EMI reduction using a Hershey kiss (Lexmark) spread profile (see Figure 5b). The Hershey kiss spread profile has a radically distinctive shape where the clock frequency sweeps at a higher rate near the start and end frequency points and is slowed down at the center. Because of the higher rate of frequency change near the two boundary points, the two side lobes are attenuated and the reduced energy is distributed over the center flat portion of the spectrum. This results in a dramatic change by approximately flattening the complete energy spectrum. As shown in figure, the Hershey kiss spread profile has provided a further 1.13dB reduction. This reduction can be higher based on the actual frequency values.

TYPES OF SPREAD

Based on the position of start and stop frequencies with respect to reference frequency, SSCGs can be classified in the following three categories:

1. *Down Spread:* Modulates the reference clock downwards and restricts the maximum frequency of the modulated signal to the frequency of reference clock. Useful in applications which are frequency sensitive and are already operating at the maximum rate they can operate.

   Down spread (%) = $(\Delta f / f_o) * 100$, where $\Delta f = f_{ref} - f_{min}$

   A down spread provides the spread spectrum clock while maintaining the maximum allowed frequency in the system.

2. *Center Spread:* Modulates the output clock symmetrically about the reference frequency (i.e., the output frequency will increase and decrease the same amount above and below the center frequency). A 1% center spread will provide a total variation of 2% with 1% variation above and another 1% below the reference frequency.

   Center spread (%) = $\frac{1}{2} (\Delta f / f_o) * 100$, where $\Delta f = f_{max} - f_{min}$

   Center spread is useful in systems where the frequency restriction doesn't apply.

3. *Up Spread:* Up-spread is exactly opposite down-spread. The reference clock is modulated upwards by restricting the lower limit to reference clock.

   Up spread (%) = $(\Delta f / f_o) * 100$, where $\Delta f = f_{max} - f_{ref}$

PRECAUTIONS WHILE USING SPREAD SPECTRUM CLOCK:

1. JITTER:

One of the significant disadvantages of using a spread spectrum clock is that it cannot be used in systems where clock accuracy is of major concern; e.g. for Ethernet or CAN bus applications. Engineers must take special care in selecting spread clocks and the spread amount for their application requirements as it may introduce substantial jitter number to the clock signal. This jitter may adversely affect system performance, causing critical setup and hold time violations, higher bit error rates, and PLL unlock issues. Jitter can be of different types and can have different effects on the performance of a system.

i. *Period Jitter (PJ):* PJ refers to the maximum change in a clock's output transition from its ideal position. PJ is generally measured as the peak-to-peak period variation evaluated over time, typically ten thousand cycles, which is simply the difference between the earliest and the latest edge. Period jitter can impact the performance of a synchronous system by reducing the timing budget. The variation of clock period from its ideal position may also lead to data setup and hold time violations. A 100 MHz clock signal modulated with 1% up spread will have a total frequency variation (Δf) of 1Mhz, with a start frequency being 100Mhz and stop frequency 101Mhz. This corresponds to variation in period from 9.9ns to 10ns. As a result, the ideal spread clock will have peak-to-peak period jitter of 0.1ns (100ps). As the spread amount is increased or the clock frequency increments keeping the spread fixed, the total frequency variation increases proportionally, hence the PJ may violate certain timing parameters. One must note here that the PJ mentioned here is solely the one introduced due to the spread clock. The device itself may add its own intrinsic jitter, making the total jitter higher than estimated above. The intrinsic jitter of device may be measured by turning off the spread.

ii. *Long-Term Jitter (LTJ):* LTJ is similar to period jitter but represents the maximum change in a clock's output transition from its ideal position over many cycles. Although it is applicable to a few specific applications, it becomes crucial with spread spectrum signals where the timing edges could be significantly displaced in time from their ideal locations. The best example of a problem with LTJ can be seen on a graphics card driving a display: excessive LTJ may cause the pixel data to be shifted from its desired position over a span of time.

iii. *Cycle-to-Cycle Jitter (CTCJ):* CTCJ is another jitter type defined as the change in clock's output transition from its corresponding position in the previous cycle. CTCJ is mostly undesirable in communication systems or in ADC circuits where the input signal is sampled at a particular instance and digitized according to the sampled value. CTCJ

in a sampling clock may cause the input to be sampled away from the desired instance leading to a bit error in the output data stream. The spread spectrum clock actually introduces an insignificant amount of CTCJ to the clock. With a very slow modulation rate, between 30khz to 120khz which is at least one thousand times slower in comparison to the reference clock frequency, it takes more than a thousand clock cycles to complete one modulation cycle, leading to negligible period differences between adjacent cycles. However, the device itself might add its own intrinsic CTCJ to the output clock. Spread spectrum techniques contributes less than 0.05% of CTCJ to the system. Thus, an SSCG may be well-suited for systems requiring low CTCJ, low bit error rates, and low EMI.

2. SPREAD SPECTRUM WITH PLL:

Another area where extra precautions must be taken is in those designs where a PLL device is a downstream and driven by the spread clock. A PLL exhibits the characteristics of a low pass filter which allows the low speed variations in the input frequency to be passed while attenuating high frequency changes above its bandwidth. Since the spread spectrum purposefully modulates the clock, the PLL may have trouble maintaining the lock to the input spread spectrum clock. The downstream PLL must be able to track the frequency change to pass the modulated clock. This depends on the PLL's bandwidth. If the PLL's bandwidth is too low, the PLL will not reliably track the input signal, resulting in tracking skew which in turn adds more jitter to the system.

PROGRAMMABLE SSCGs:

Programmability provides flexibility and easy inventory management. With a programming option available on a clock generator chip such as configurable drive strength, system designers can easily change the drive strength (rise / fall time) of the clock edge based on application requirements. This may be helpful in further reducing EMI. There are SSCGs in market with more conciliatory programming options where system designers can change parameters such as spread amount, spread profile type, spread on/off, type of spread and output clock frequency. Another major advantage of programmable SSCG is that multiple unique programmable frequency outputs can be integrated into a single chip, thus eliminating the large number of crystal and reducing the overall cost. Depending upon the application, designers can use a single SSCG to provide clocks with different properties to each subsystem, resulting in faster time to market and lower cost.

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