Motor Control - Brushless DC Motor Control

AN2227

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Associated Project: Yes
Associated Part Family: CY8C27xxx
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Software Version: PSoC Designer™ 4.2
Associated Application Notes: AN2170

Application Note Abstract

The Application Note demonstrates a PSoC® implementation of brushless direct current (BLDC) motor control using sensor-less, back-EMF technology.

Introduction

BLDC motors are widely used in industrial applications, home appliances, and vehicle systems. Such motors consist of a multi-pole permanent magnet placed on the rotor and several windings [1].

Various methods can be employed to control the BLDC motor. The simplest way is to use rotor position sensors. The sensors can be optical, magnetic (Hall effect or magneto-resistance, effect-based) or inductive. However, sensors increase cost and add reliability problems in motors operating in harsh environments where demands for sensor robustness are high. The increasing power of embedded computing, coupled with lower prices for power semiconductors and microcontrollers, has allowed for more sophisticated methods of motor control. One popular technique is to use a back-electromagnetic force (back-EMF) signal, which is induced by revolving the rotor permanent magnet around the drive coils.

This Application Note describes how a BLDC motor driver can be built using back-EMF sensing.

The motor driver has the following features:

- Reliable motor start with and without load;
- Stable operation when the load on the drive shaft changes;
- Rotation speed stabilization with power supply and load fluctuations;
- Overload protection;
- Runtime rotation speed control using preset speed tables;
- Error diagnostics and recovery after failures.

A distinctive feature of this driver is its use of three PSoC™ mixed-signal array low-pass filters (LPFs), built around PSoC's switched capacitor (SC) blocks. These filters are second-order Bessel filters and used for phase delay in the drive phase switching mechanism, generating the optimal torque on the motor shaft.

The proposed project uses a 75W BLDC motor with a nominal 220V power supply. However, the project can be adapted to motors with 12-, 24-, 48- or 120-volt power supplies; only the phase voltage resistive divider and the motor coil level translators (frequently named coil drivers) must be adapted to specific motors. Table 1 lists the main characteristics of a motor driver.

Table 1. Driver Specifications

Parameter	Value
Number Phases	3
Input Voltage	220V AC ±20%
Output Power	100W
Max Output Current	3.5A
Output Signal Frequency: **Minimum** **Maximum**	 50 Hz 120 Hz
Motor	BLDC, Sensor-less
Motor Pole Pairs	4

Driver Flowchart

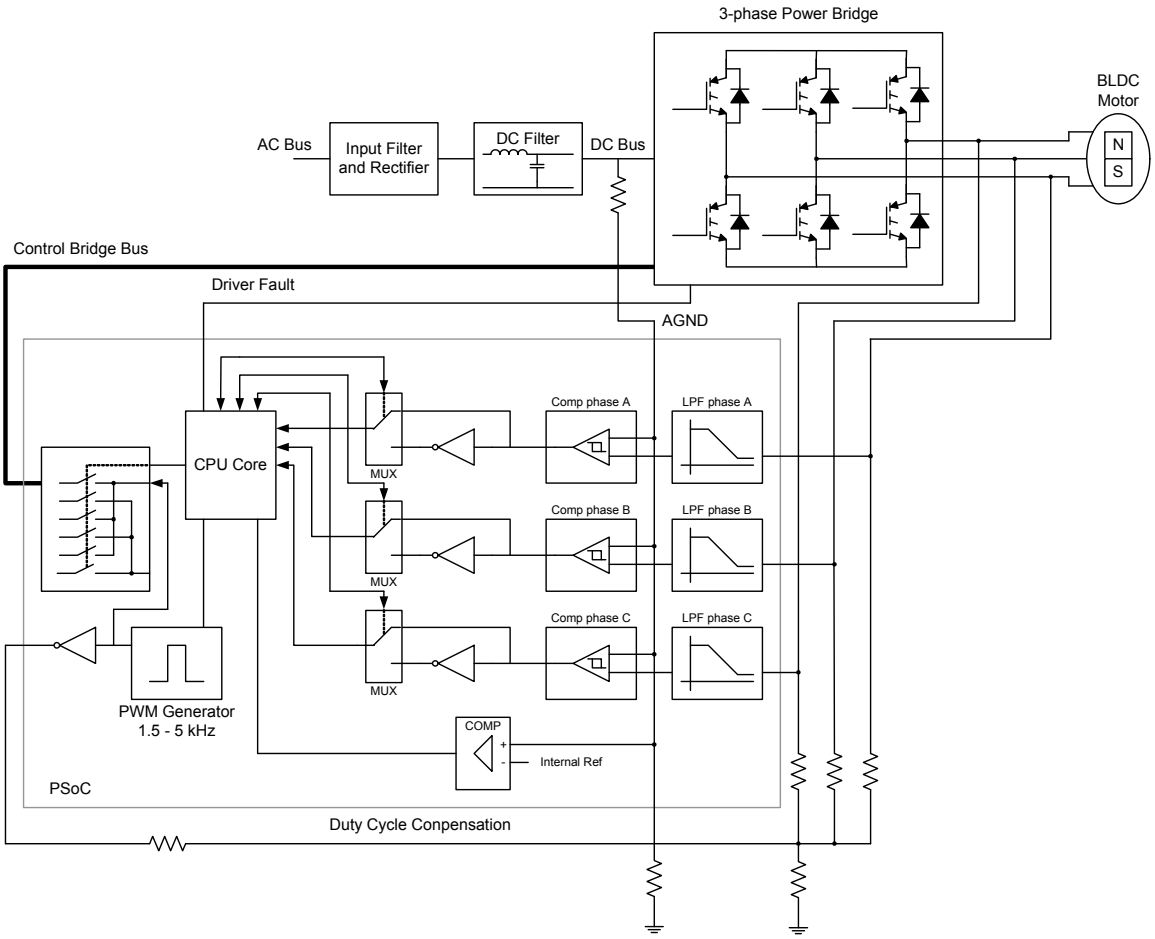
The driver flowchart is shown in Figure 1. The power circuit includes:

- AC input line noise filter,
- AC line LC filter,
- AC mains rectifier,
- A step-down regulator to produce regulated 15V and 5V electronic supplies (not shown on the flowchart),
- A three-phase power bridge with a level translator to control the bridge using low-power digital signals.

For simplification, the driver status display LEDs and speed setting switches are omitted.

Only a detailed view of the driver is provided in Figure 1. Power modules are fairly simple and not examined here. The driver consists of a bridge chip driver for the IGBT transistors and a current sense resistor for measuring current, which is proportional to the total bridge-arms current. The IGBT level translator converts the logic level signals from the PSoC (control bridge bus), into levels suitable for driving the IGBT bridges' low and high sides. The International Rectifier IR2130 chip is used as the IGBT driver. This chip has elements to protect the bridge transistors from overcurrent conditions, a low-power voltage output stage, and internal dead time control. Such features let the PSoC concentrate its resources on motor control and react only when a complex *DriverFault* event is raised by the IR2130. Lower cost drivers can be used by integrating these features into the PSoC device.

Figure 1. BLDC Motor Driver Flowchart



The device handles the following signals from the power driver circuit:

- Three voltage signals that are proportional to the output phase voltage of the IGBT driver.
- The voltage signal, which is relative to the DC bus voltage. This signal is the PSoC analog ground (AGND). The resistive divider attenuates this signal to double the phase signals.
- Driver fault signal, which indicates that at least one fault event has occurred.

The phase voltage signals enter the LPFs. Their cutoff frequency is three times higher than the phase switching frequency generated by the motor driver.

The PSoC analog blocks process the phase voltages.

As mentioned above, PSoC's AGND is floating and proportional to half the DC bus voltage, which is the rectified and filtered AC main voltage.

LPFs serve two functions. The first is to generate the necessary phase delay for the motor phase voltages. Thirty degrees is optimum for motor operation in this application. The second function is to filter the phase voltage from the PWM frequency to generate a signal wave, which is close to sinusoidal. When the filtered signal crosses AGND, the internal comparator triggers and a falling or rising edge signal is determined. At runtime, the awaiting edge type and queried phase channel are determined in firmware. The comparator toggle initiates the interrupt, which is handled in the firmware.

The PWM generator forms the pulse-with modulated signal for high side bridge. The low side is controlled by constant, clear logic levels.

The bridge high side PWM signal-routing is routed through an internal, firmware-controlled de-multiplexer. Note that the divided phase voltages are non-symmetric relative to AGND. This results in a strong influence when a small PWM duty cycle is set. To resolve this, a single compensation voltage is added simultaneously to the three phase signals. This voltage is inversely proportional to the PWM duty cycle and is generated by inverting and filtering the PWM output signal.

DC bus voltage monitoring is implemented using the programmable voltage window comparator. If the voltage value on the DC bus (which powers the bridge high side) is above or below preset values, an interrupt is generated. This stops the motor, prohibiting operation in unsafe regions. If necessary, the analog-to-digital converter (ADC) can be used to monitor the DC bus voltage.

Device Schematic

Device schematics are shown in Appendix A.

The device has three elements. The power element includes:

- Supply-Line Filter
- Rectifier
- DC Bus Filter
- IGBT Transistor Bridge
- Voltage Converter for Low-Voltage Parts Supply

The second element includes the IR2130 driver and dividers for the phase voltages. The third element contains the PSoC chip and speed selector. The speed selector is made with opto-couplers (which perform the galvanic isolation and are connected in parallel with DIPswitches for manual speed control) for external speed control. The three LED indicators display alarm events. These three parts are presented as three different circuit boards to provide better flexibility for specific motor applications.

Device Operation Details

As mentioned above, the motor control system uses the sensor-less back-EMF technique. The motor winding functions operate as position sensors during rotor rotation. To accomplish this, the winding, working in sensor-position mode, is disconnected from the line supply. An Induced voltage is generated on the winding by the revolving magnet on the motor rotor. The sign and direction of the voltage change indicates the rotor pole location relative to fixed stator windings.

The main tasks of PSoC are to detect the position of the rotor using the generated voltage and to perform the phase switching in such a way that the new driving phase assists rotor revolution in the desired direction. This is the main condition of motor rotation stability.

At first glance, a simple comparator on each phase is enough for proper operation. But back-EMF voltage has a more complex waveform, as shown in Figure 6 in Appendix D. In Figure 6, the PWM induced noise from neighboring windings can clearly be seen because the back-EMF winding is not loaded.

There are a couple of ways to separate the back-EMF signal from unwanted noise. The first way is to use low-pass filtering to suppress the PWM-induced noise. The second method is to perform the phase voltage analysis when the PWM signal is inactive and the transient process of the winding is complete. This method is suitable for low PWM duty cycle values or for low-power motors, where inductive/capacitance cross coupling between coils is weak. The first method for noise suppression works well when it is implemented using PSoC LPFs. After filtering, the signal can easily be compared to a reference signal.

All filters have phase delay. This delay depends on the signal frequency. Thus, the moment of windings commutation is changed at the same time as rotor revolution frequency. This can cause a loss of back-EMF signal synchronization or large torque ripples. Two solutions for this problem are:

1. Use the phase correction filter, analog or digital, to provide near-constant phase delay in the operational frequency range.
2. Apply the tunable conventional switched capacitor-based filter.

The first approach requires using complicated analog circuits or a more expensive DSP core for multi-channel signal processing. Such firmware must continuously read and process triple ADC conversions in real-time. There are other tasks for the drive controller, such as speed control. This makes the first approach difficult to implement with low-cost microcontrollers. The second approach requires external reconfigurable filters when conventional microcontrollers are used. This increases the driver price and complicates the circuit. However, PSoC has many firmware-controlled filters inside. Therefore, the best solution is to use the tunable LPF approach. This gives the optimal combination of price, quality, and complexity.

The phase-delay filters can be placed in three PSoC columns and the built-in comparators can be used for output signal-crossing detection. Bessel filters are preferred since they provide linear phase delay versus frequency up-to-a cutoff point. The filter phase delay at the cutoff frequency is 90 degrees. The SC filter cutoff frequency is directly proportional to the filter clock rate, which allows stable phase delay in the full input frequency range by properly adjusting the filter clock frequency. This delay corresponds to a constant angle between the rotor poles and the stator windings in commutation moment. The phase delay angle is kept to 30 degrees in this application. The clock rate for the filters can be generated using the 16-bit counter with a programmable period, which can be allocated in the PSoC digital resources.

Each SC filter has an output comparator that compares the filter output signal to AGND. The comparator output drives the comparator bus, which can be polled in software or trigger the interrupts. The built-in look-up table (LUT) allows triggering the interrupts on the rising or falling edge of the comparator bus, as pre-configured in the firmware. This feature is used to detect the back-EMF signals' zero-crossing events and to generate signals for motor winding commutation. Each filter triggers interrupts which are handled in the firmware using a dedicated state machine to determine the next phase switching order and adjust the next interrupt polarity in runtime by modifying the content of the LUT control register.

Note For every motor phase change, the next expected back-EMF signal polarity change direction is opposite the previous. Therefore, the comparator bus signal is inversed using the LUT in the triggered interrupt service routine (ISR) just after it starts. This provides hysteresis and additional noise immunity with regard to triggering multiple interrupts.

Figures 2 and 3 illustrate key principles of driver and motor operation. A, B, and C are the voltages on motor phases. UP_A, DOWN_A, UP_B, DOWN_B, UP_C, and DOWN_C are the bridge branch control voltages. UP is the upper (high side) branch. DOWN is the lower (low side) branch. A high level denotes the "on" state and a low level denotes the "off" state). INT is the interrupt signal on the phases. A30, B30, and C30 are delayed 30 degrees from the filtered voltages phase.

One peculiarity of this architecture is that the control PWM voltage is supplied only at the upper bridge branch (high side). This produces an asymmetrical signal relative to half of the supply DC bus voltage.

At low PWM duty cycles, the filtered phase voltage is much smaller than half the supply voltage. This, together with ripple on the DC bus (which is in the filter's pass-band), can cause false triggers on the comparators at motor start. To prevent this, the compensation network uses an inversed PWM signal and biases the three filters together. This raises the filter's DC component to half of DC supply voltage throughout the whole PWM duty cycle range.

For this purpose, the inversed main PWM signal is routed to an external pin and filtered using an RC filter with a voltage divider (R4, C5, and R5 on the driver schematic). As a result, the C1 DC voltage is inversely proportional to the main PWM DC component. The divided voltage from C1 is summed with the back-EMF signal relative to PSoC digital ground and compensates the DC component relative to the divided "DC bus in" signal. Figure 12 illustrates the compensation voltages for minimum and maximum rotation speeds and minimum and maximum PWM duty cycle values. Channel_1 displays the inversed PWM signal and Channel_2 displays the compensation voltage.

Figure 2. Driver Phase Signals

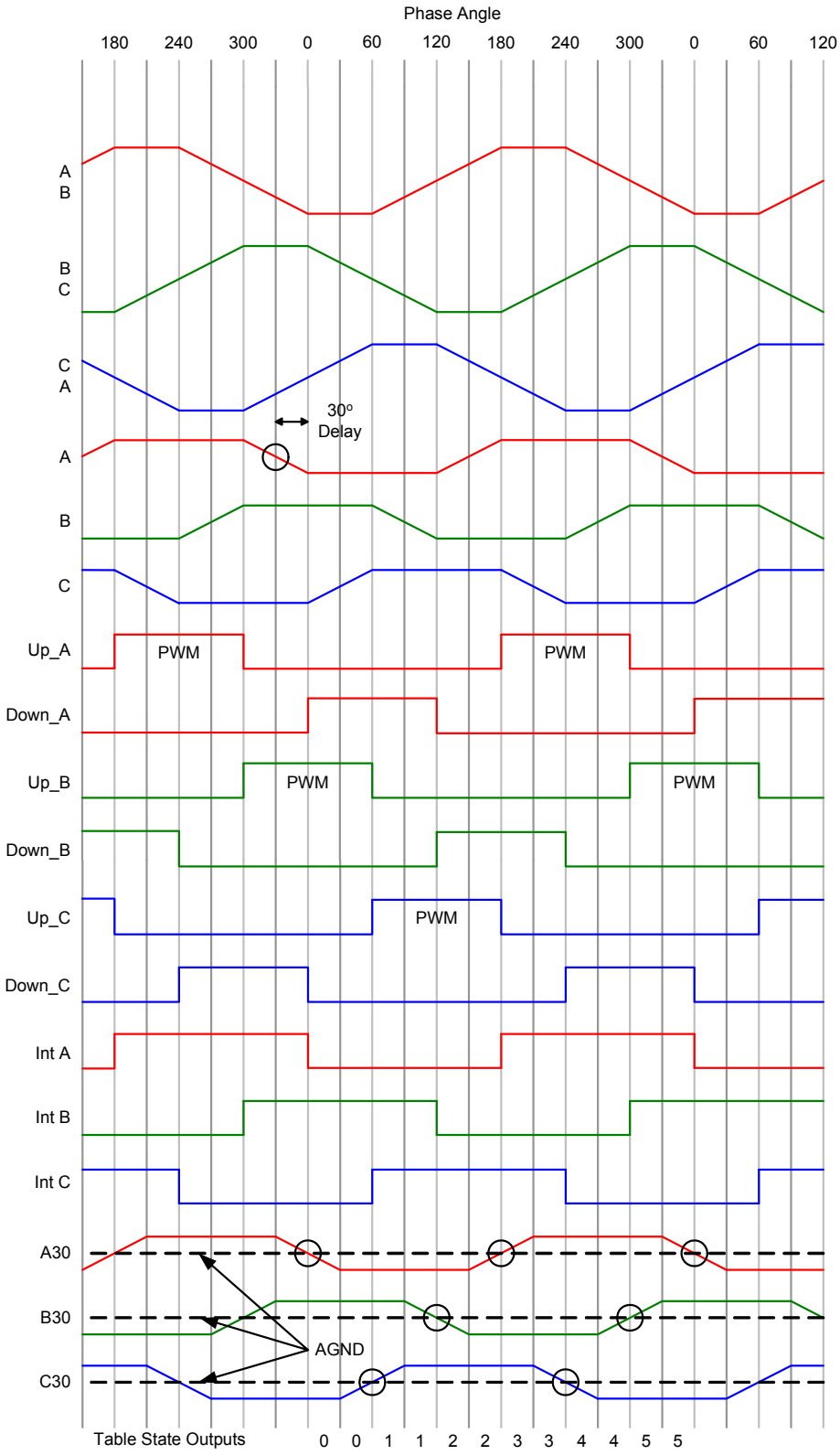
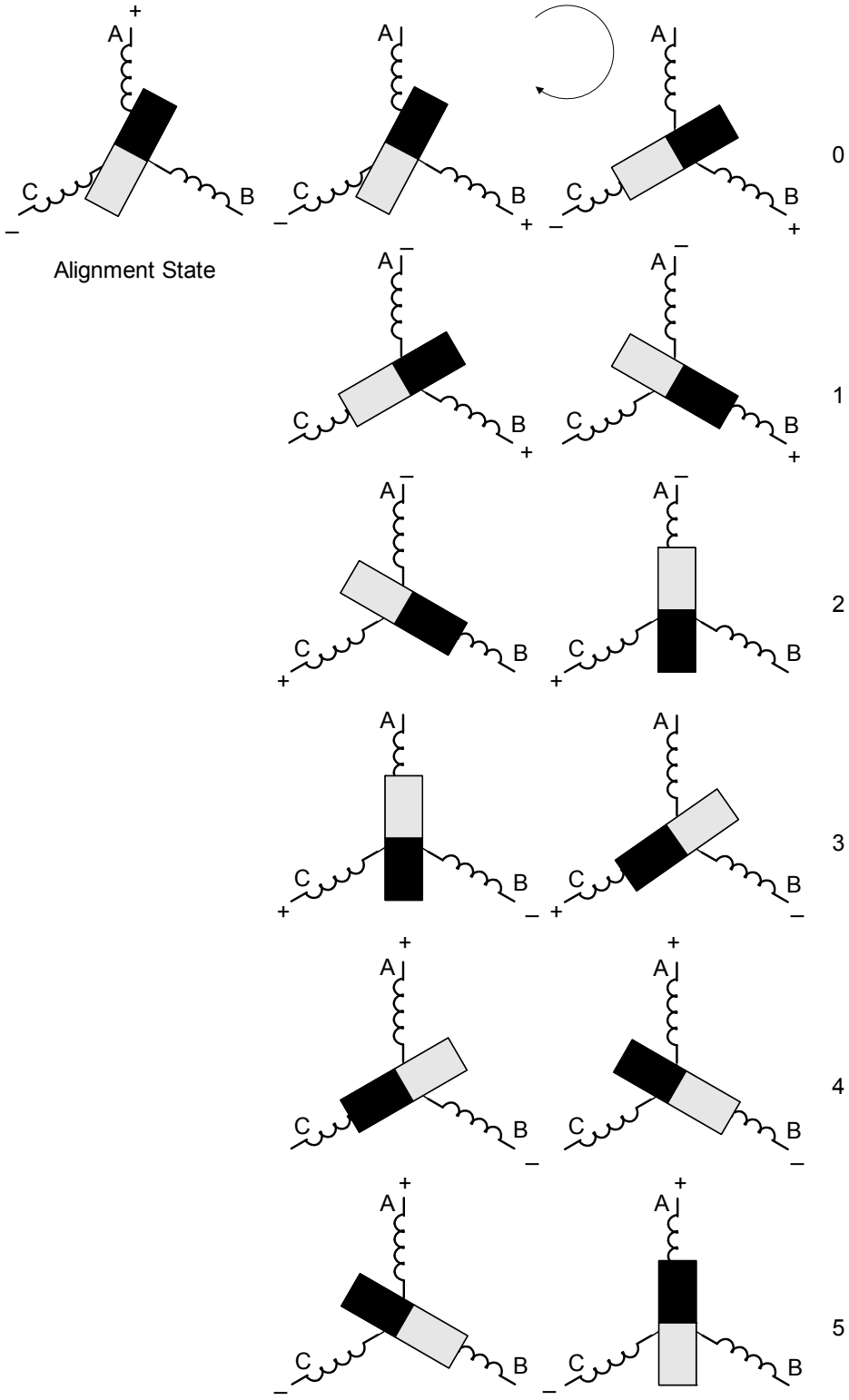


Figure 3. Rotor Positions for Various Phase Drive Signals*



* See Figure 2 for Voltage Diagrams

Driver operation contains the following stages:

1. Stop Stage

The events register marks which event triggered the stop stage. If the counter does not exceed the preset threshold, the PSoC reads the speed-setting switches. In this state, all bridge drivers are switched off and the PSoC polls the speed-setting switches. This stage is exited by setting a non-zero speed value. See Table 3 for possible speed values.

2. Full Stop Stage

The driver enters full stop stage after a preset number of failed motor start attempts. LED D2 indicates this stage. Only power-on-reset can reinitialize the driver from this stage.

3. Driver Preparation Stage

The IR2130 driver has a bootstrap capacitor feature. The bootstrap capacitor must be charged to 10V before it can be used. Otherwise, high side outputs are turned off regardless of control signals. It is necessary to hold the bridge low-side power transistors on during this stage.

To precharge the bootstrap capacitor, the low side transistors are switched on and the IR2130 output *DriverFault* is interrogated. If this signal is low, the low-side power transistors are turned off and the cycle is repeated. Transistor on/off switching is necessary to clear the error flag of the internal IR2130 driver.

The driver preparation stage is illustrated in Figure 10. Channel_1 shows the voltage of the motor coil windings' current sense resistor during initial PWM duty cycle determination. Channel_2 shows the "Fault driver" signal, which triggers when the current reaches 3.5A. The falling edge of this signal turns off bridge drivers inside the IR2130 and stores this state in the driver internal trigger. To make the IGBT driver operational, this trigger should be cleared. This trigger is cleared after a preset timeout by applying a falling edge on any low-side bridge control input. In the project associated with this Application Note, the trigger is reset by applying pulses to the phase C lower switch and polling the "Fault driver" in the software. If the "Fault driver" signal cannot be cleared (trigger cannot be reset) within 2 ms, motor start attempts are aborted and a motor start error flag is set.

4. Binding Stage

There are two actions in the binding stage. First, the rotor is set at a predetermined start position by applying the drive voltage to two windings. Second, the maximum possible startup duty cycle is determined. This duty cycle is proportional to the motor start-up current. Rotor position, set during the binding stage, is shown in Figure 3 on the left. The necessary windings are commutated in accordance with the jump table. The PWM generator frequency is set to 1.5 kHz during this stage. The duty cycle is then incremented every 0.8 ms. After each PWM duty cycle increment, the *DriverFault* output is queried. If *DriverFault* equals zero, the motor winding current exceeds the maximum possible value. In the example project, this maximum value is set to 3.5A. The PWM duty cycle increment is finished as soon as a zero value at the *Driverfault* output is received.

The amplitude of the AC ripple voltage also depends on DC filter parameters. If this measured duty cycle is directly selected as the maximum PWM pulse width, the overcurrent protection can prematurely turn off the motor. Therefore, the maximum measurable duty cycle ratio must be slightly decreased to prevent a false overcurrent protection trigger. The measured duty cycle is decreased by 25% and used to start the PWM duty cycle value in the example project.

5. Free Running Stage

In this stage, the rotor begins rotation and is synchronized with a back-EMF signal. The stage the PWM operational frequency is set to is 5 kHz (it is possible to increase to 8 kHz). The timeout for every winding combination is determined using Table 4 in Appendix B, where units are PWM periods (200 us). This time is controlled by using reprogrammable 16-bit timer interrupts. The PSoC's *CycleCounter* is used for this purpose.

The time intervals between phase switching events during motor start-up are much longer than during normal motor operation. As a result, the motor coils accumulate more energy during the driving stage. Considerable time is required to dissipate this energy though the IGBT's transistors' reverse current protection diodes when the coil driving stops. The back-EMF signal can be received only when all stored energy is dissipated and the diodes are closed. This limits the time interval during which the back-EMF signal can be sensed. The dedicated 16-bit counter is used to set the delay proportional to the current phase switching period. This determines the interval during which a valid back-EMF signal should be sensed. This counter is used for other purposes later, thanks to PSoC's dynamic re-configuration capabilities.

The LPF cut-off frequency has a fixed value at this driver stage and is set by using the dedicated 16-bit counter, *Filt_Counter16*, in the PSoC configuration.

The back-EMF signal is sensed after each phase switch event (starting from the second switch event). If the expected event is well received, the driver exits from free running stage and switches to the synchronous rotation state.

Figure 13 illustrates the motor start-up procedure and the switch to back-EMF control mode. For motor start-up the rotor is accelerated in the free-running stage by decreasing the step-by-step coil switching time intervals. These intervals are longer than normal phase switching intervals. During these intervals, the rotor can reach equilibrium position where the shaft torque drops. To get maximum starting torque, the coil switching can be implemented by analyzing the back-EMF signal. The back-EMF signal is analyzed during the free running stage. This is after the second windings commutation and the first valid back-EMF signal transition across AGND level finishes the free-running stage and switches to the back-EMF sensored stage. The back-EMF signal is analyzed by the comparator bus control register software polling in the loop, unlike the interrupt-driven operation of the sensored state. Using the back-EMF signal analysis during motor start-up allows a reduction in the motor current overload by eliminating redundant free-running stage operation time, which is characterized by larger winding currents.

6. Sensored Rotation Stage

Phase switching is initiated by the back-EMF signal, which is delayed at the phase plane by the LPF. This is the primary motor operation stage. The period between winding commutations is measured by a cycle counter with accuracy equal to 1/32 of the PWM period. This value is used to adjust the rotor rotation frequency with the PI regulator.

The counter terminal count interrupts are used to generate the timeout to wait for the proper back-EMF signal.

If the timeout has expired and no back-EMF received, the control state machine leaves the sensored rotation state and switches to the stop state and increases maximum driver start attempts counter. When this counter reaches the threshold value, the driver switches to the full stop stage and powers on an error LED.

The PI regulator calculates the PWM duty cycle to maintain constant rotation speed and is activated every sixth commutation cycle phase. This corresponds to one electric motor period. The speed-setting switches are queried in this loop and, if a new value is read, the new LPF's clock frequency and new PI regulator reference values are set.

The following characteristics should be known in order to design an optimal rotation speed control PI regulator:

- Loaded and unloaded motor transfer function;
- Regulation control parameters such as suitable control overshoot and maximum speed-setting time.

Since this project is intended to demonstrate PSoC in control of a sensor-less BLDC motor, the PI regulator is implemented using a simple approach. As mentioned above, the speed control is induced once every motor electrical period. The rotation period is determined by using the measuring counter. The regulator input signal is obtained as the difference between the reference (T^{ref}) and measured (T^{mes}) periods. The new PWM value is calculated by using the formulae:

$$\Delta t_i = T^{ref} - T_i^{mea}$$

Equation 1

$$P_i^{PWM} = \frac{(K_{\text{int}} - 1) D_{i-1}^{PWM} + K_{\text{int}} \Delta t_i}{K_{\text{int}}} + K_{prg} \Delta t_i$$

$$D_i^{PWM} = \max\left[\min\left(\frac{17}{16} D_{i-1}^{PWM}, P_i^{PWM} \right), \frac{15}{16} D_{i-1}^{PWM} \right]$$

Equation 2

The proportion term:

$$K_{prp} = 1/32$$

was selected empirically for the motor used with this example project. The integration term was selected to be:

$$K_{\text{int}} = 1/32$$

This value is the same as the proportional term. The end user can adjust the regulator coefficients according to load specifications.

The maximum PWM change speed value is limited in effort to prevent large PWM duty cycle changes over time. The regulator coefficients were chosen to be powers of 2 in the example project. However, the PSoC power is enough (due to a built-in MAC) to run the regulator with other coefficients.

The falling edge of the IR2130 *DriverFault* triggers an interrupt, which turns off all the bridge transistors, exits the current state, enters the stop state, and turns on the LED D1 (see schematics). As described above, the motor makes several attempts to restart from the stop state after a several-second delay.

The nominal time to reach speed is checked in the sensored state as well. If motor rotation speed does not reach 7/8 of the nominal value during a predefined timeout, the driver leaves the sensored state and switches to the stop state. The time is measured in motor rotation periods. LED D3 displays that the nominal rotation speed exceeds the timeout.

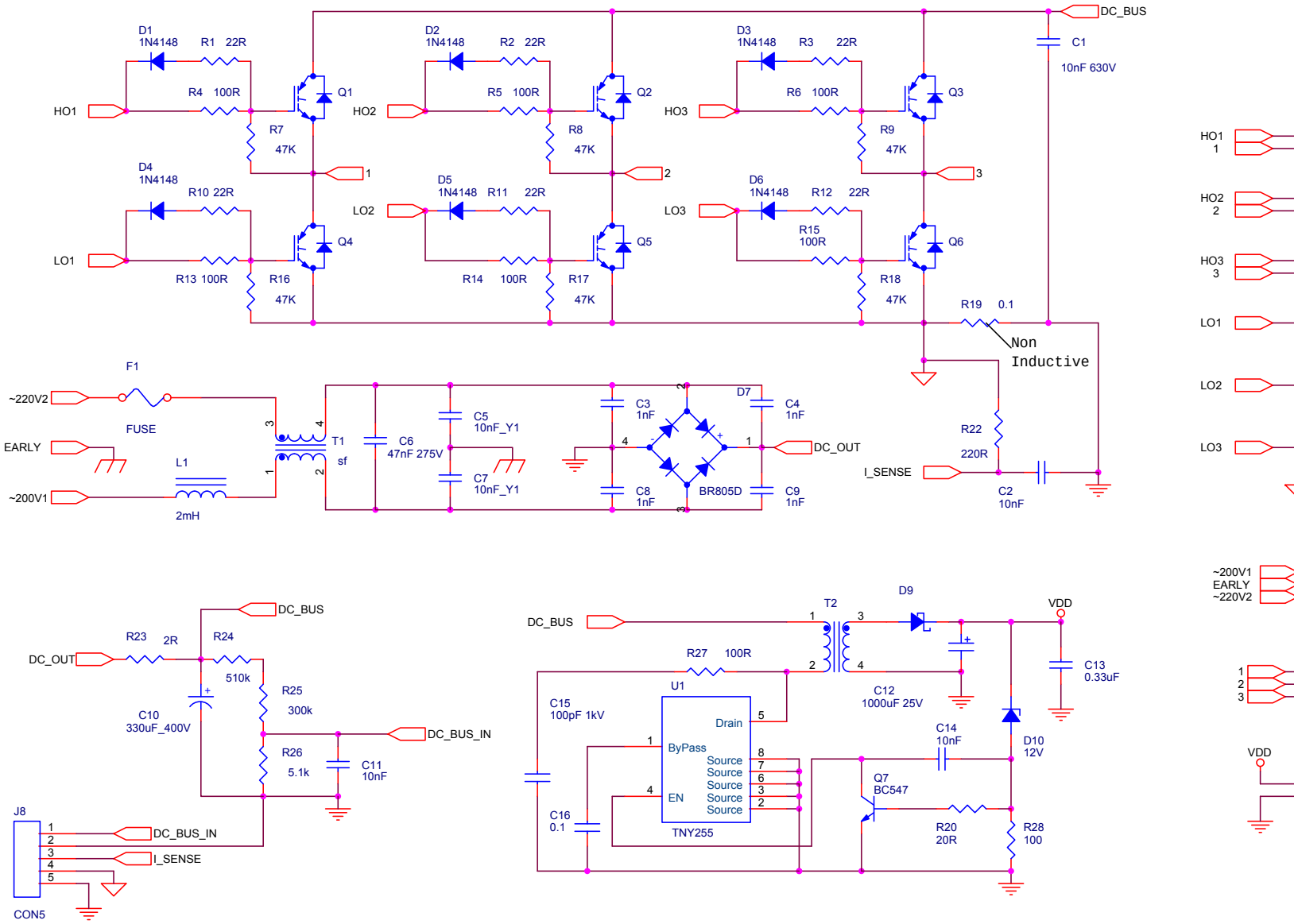
Conclusion

This Application Note demonstrates a PSoC sensor-less BLDC motor driver. With minimal hardware and software modifications, this driver can be used to control BLDC.

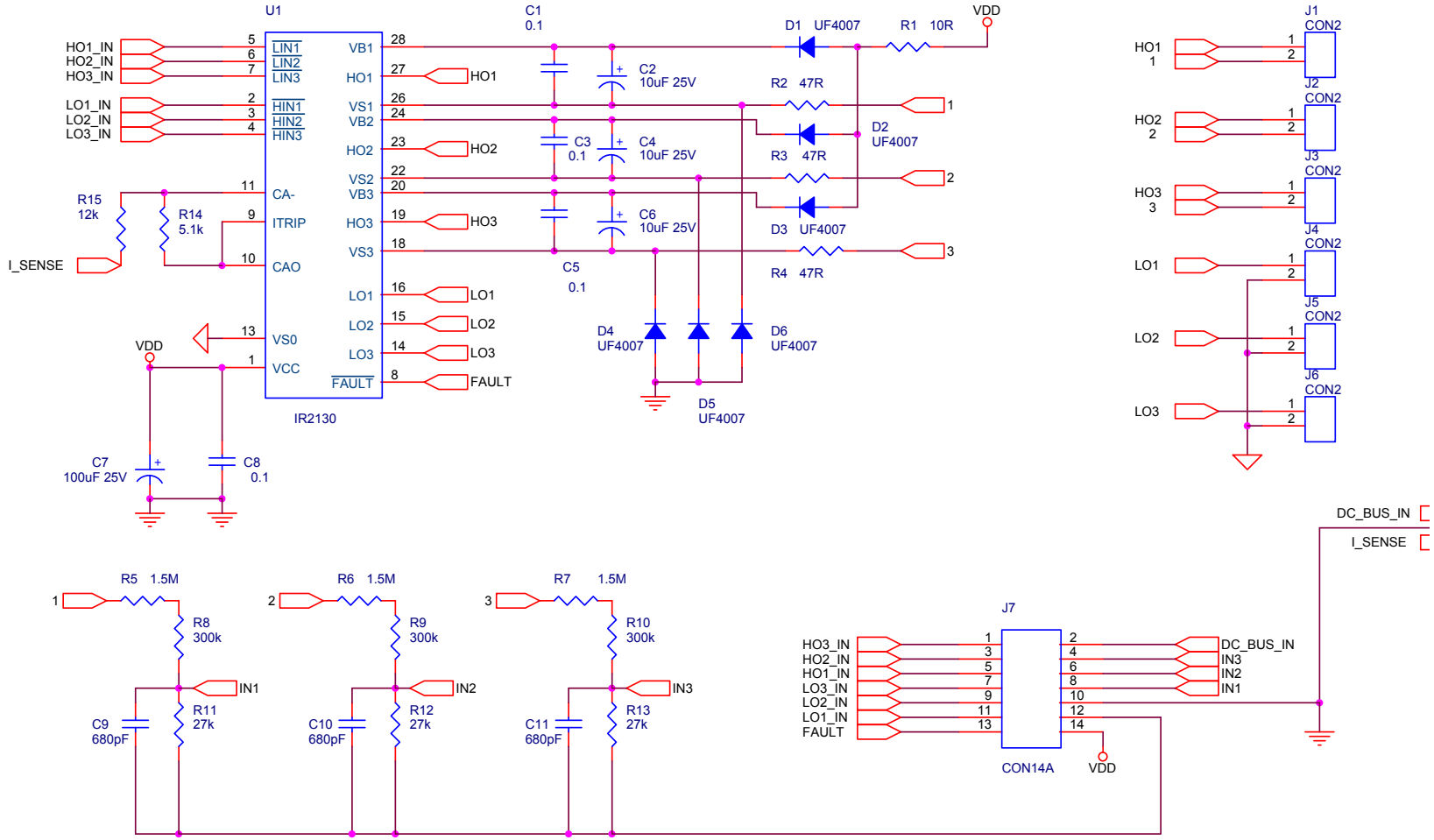
References

1. “Handbook of small electric motors”, William H. Yeadon, Alan W. Yeadon, McGraw-Hill, 2001.

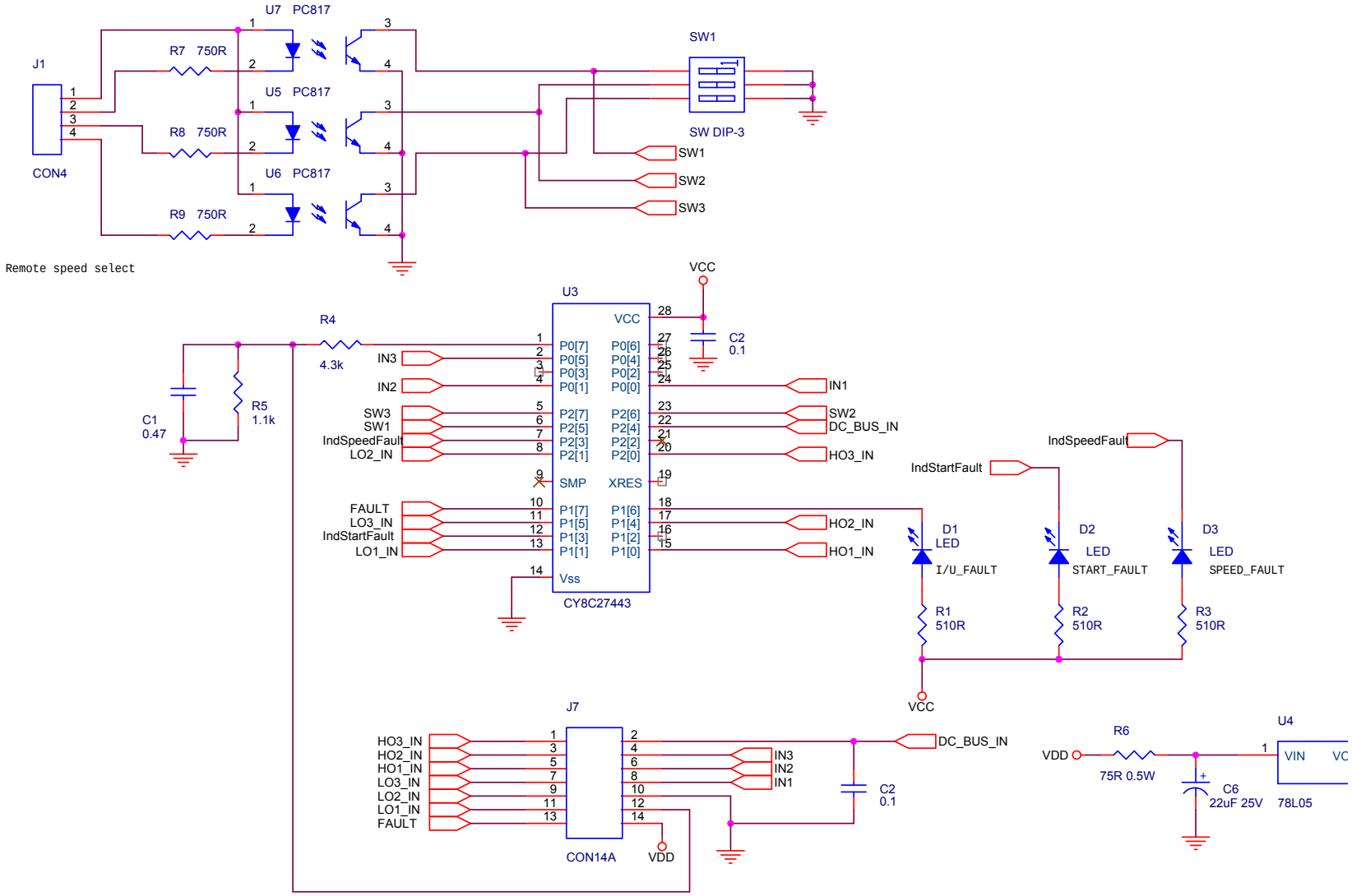
Appendix A. Driver Schematics



The Driver Power Schematic



IGBT Driver Schematic



CPU Module Schematic

Appendix B. Referenced Tables

Table 2. IGBT Bridge Control Table

# Phase	Up A	Up B	Up C	Down A	Down B	Down C
0.	0	1	0	1	0	0
1.	0	0	1	1	0	0
2.	0	0	1	0	1	0
3.	1	0	0	0	1	0
4.	1	0	0	0	0	1
5.	0	1	0	0	0	1

Table 3. Speed-Setting Switches and Nominal Speeds

Setting	Speed RPM	Electrical Frequency Hz	Filter Frequency Hz	Period in Counter Units*
b000	Stop	0	0	0
b001	2200	73.3	220	2182
b010	2400	80.0	240	2000
b011	2600	86.6	260	1846
b100	2800	93.3	280	1714
b101	3000	100.0	300	1600
b110	3200	106.6	320	1500
b111	3400	113.3	340	1412

* Counter unit = PWM_period*32*6
The following items were selected in this driver:
Freq_mechanical = RPM / 60, where RPM – revolutions per minute
Freq_electrical = Freq_mechanical*p
Freq_interrupt = Freq_electrical*6 (rising and falling edges)
RisingEdge_interrupt_Freq = Freq_electrical*3
p = motor pairs poles number

Table 4. Phase Commutation Duration During Motor Free-Running Starting

Cycle	0	1	2	3	4	5 and More
Duration in PWM Period Units (200uS)	125	113	100	88	75	63

Appendix C. Firmware Flowcharts

Figure 4. Driver Initialization and Determination of Maximum PWM Value

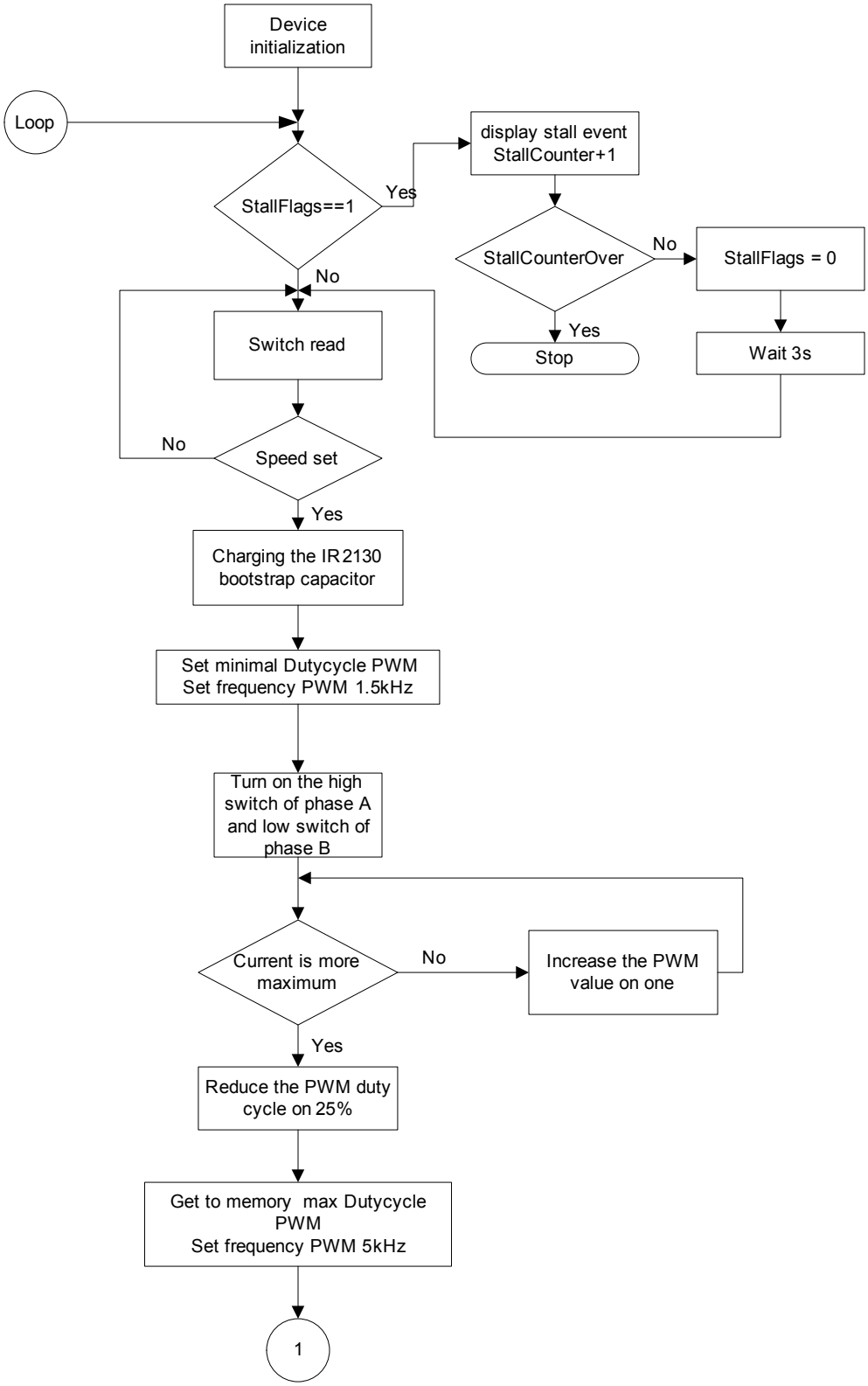
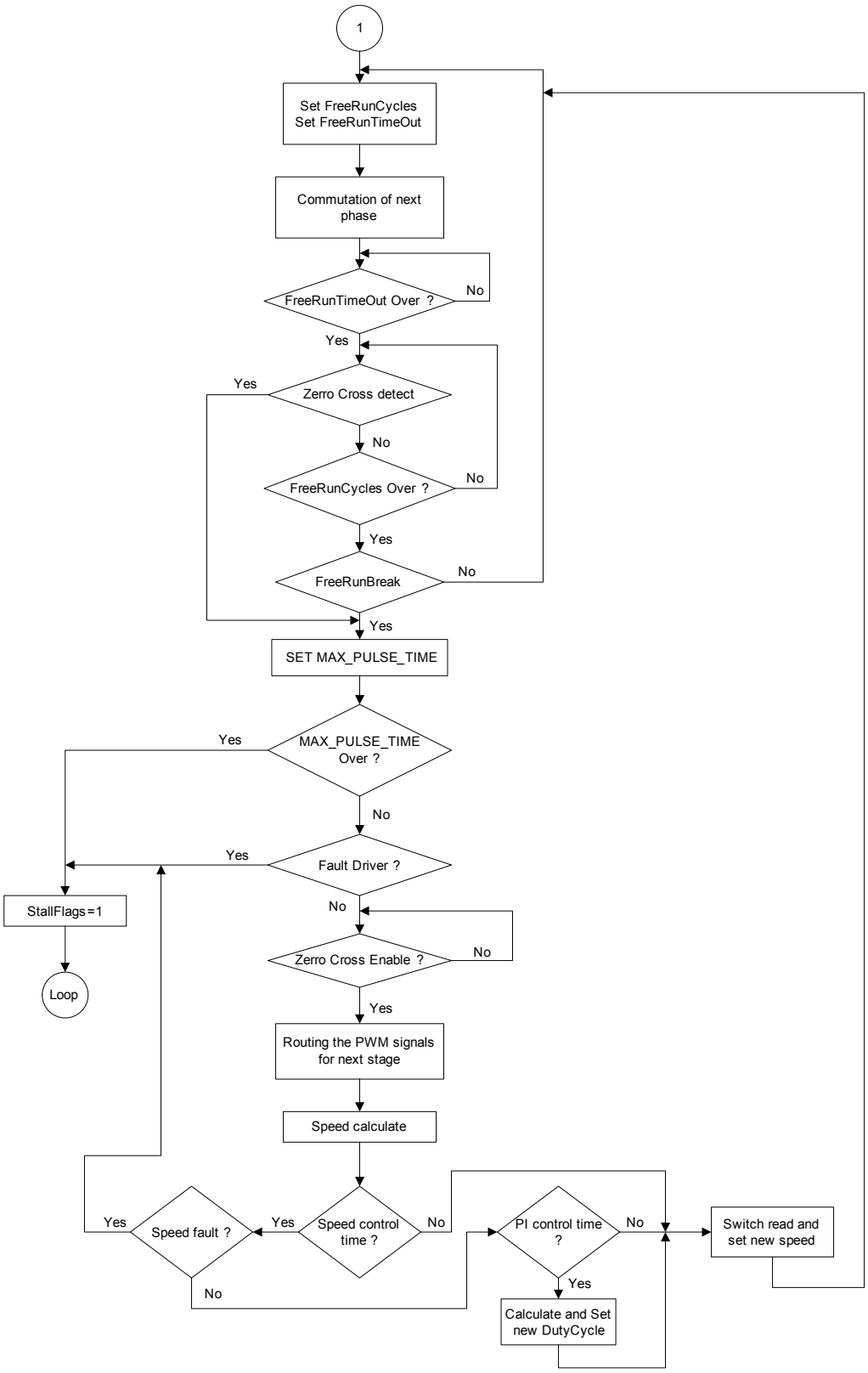
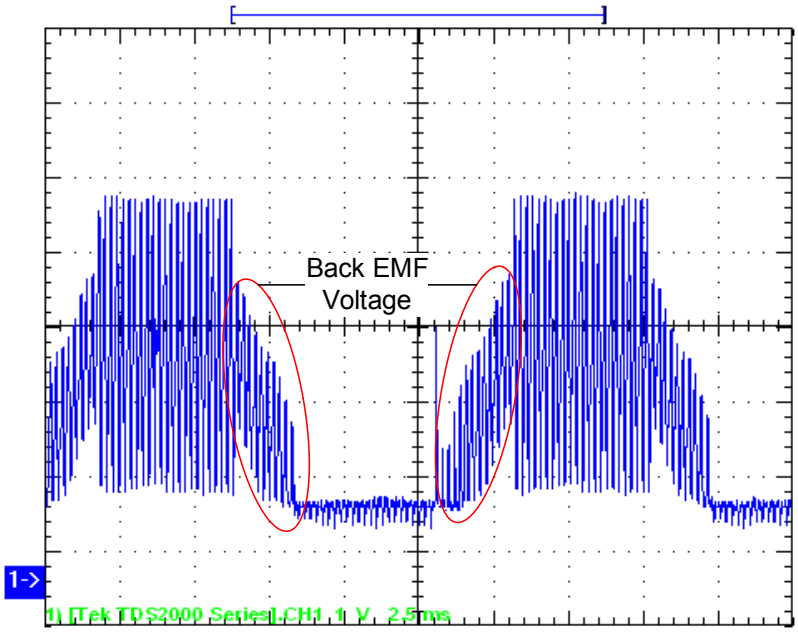


Figure 5. Motor Operational

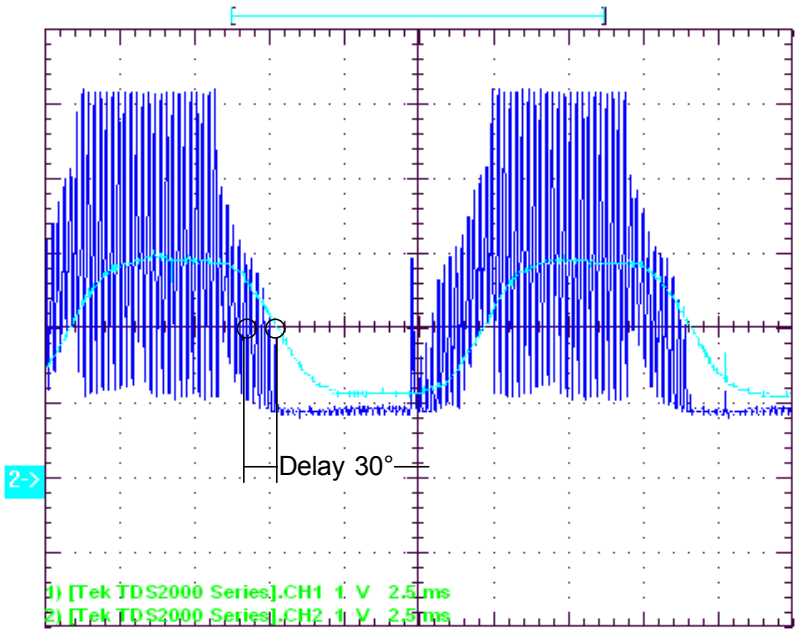


Appendix D. Scope Images

Figure 6. Back-EMF Signal (a) and Filtered Signal (b)



(a)



(b)

Figure 7. Motor Phase Signals

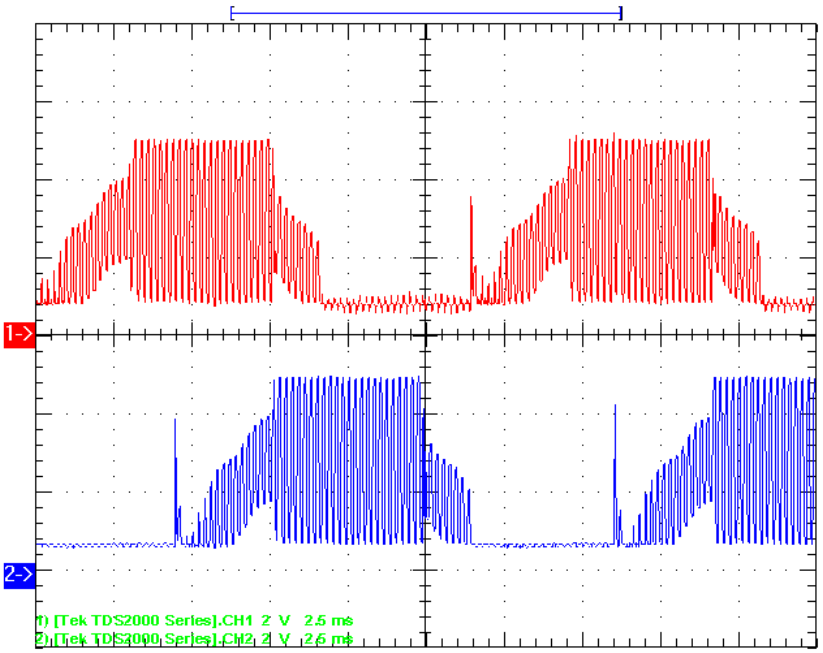


Figure 8. Filter Output Signals

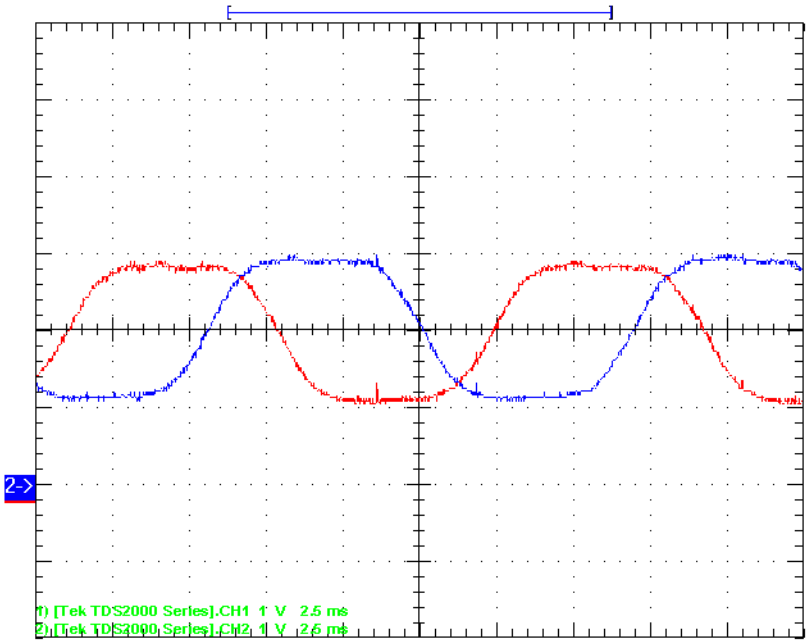


Figure 9. Motor Start Procedure for Varied Loads

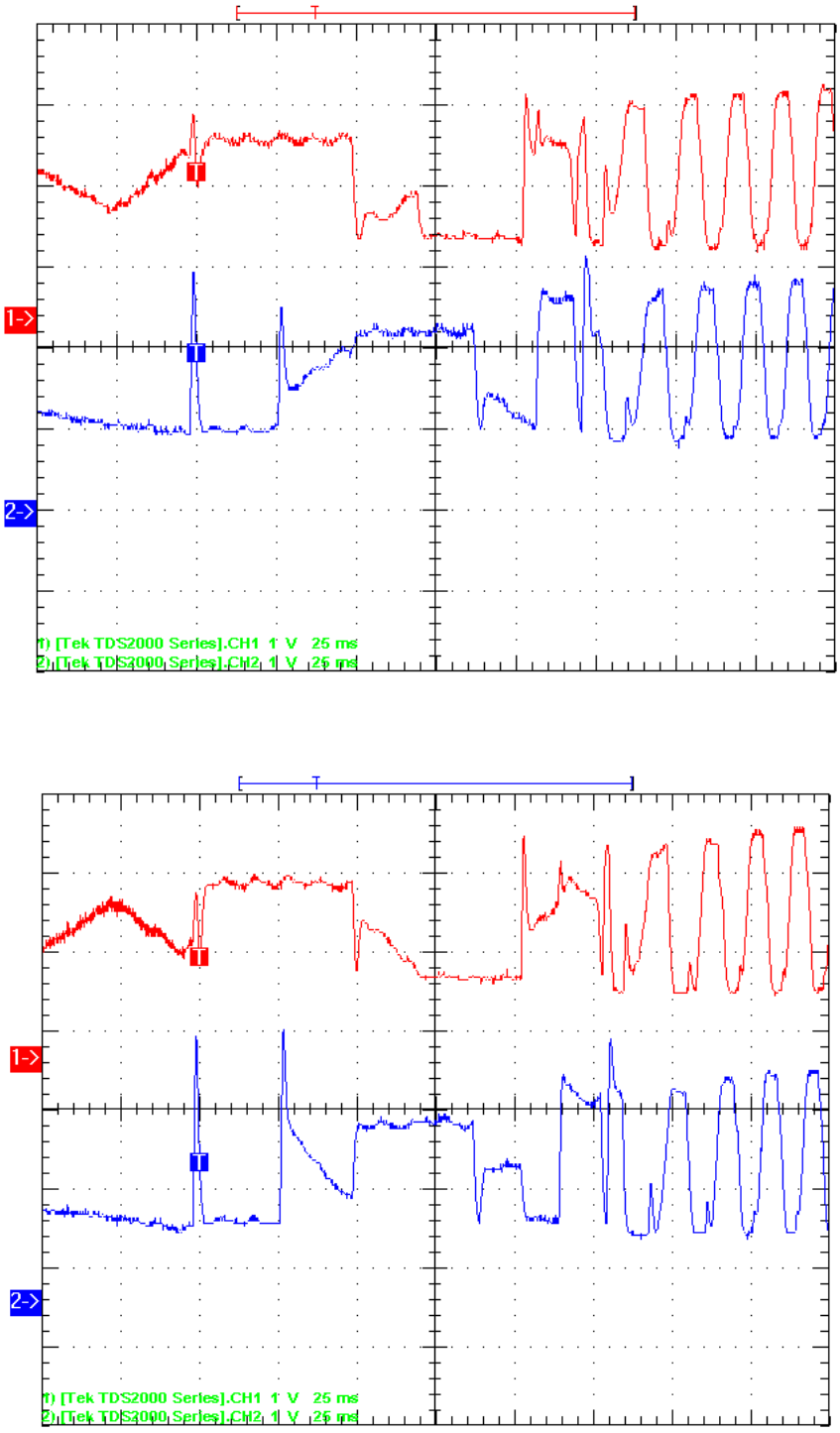


Figure 10. Scope Image for Initial Duty Cycle Determination (Driver Preparation)

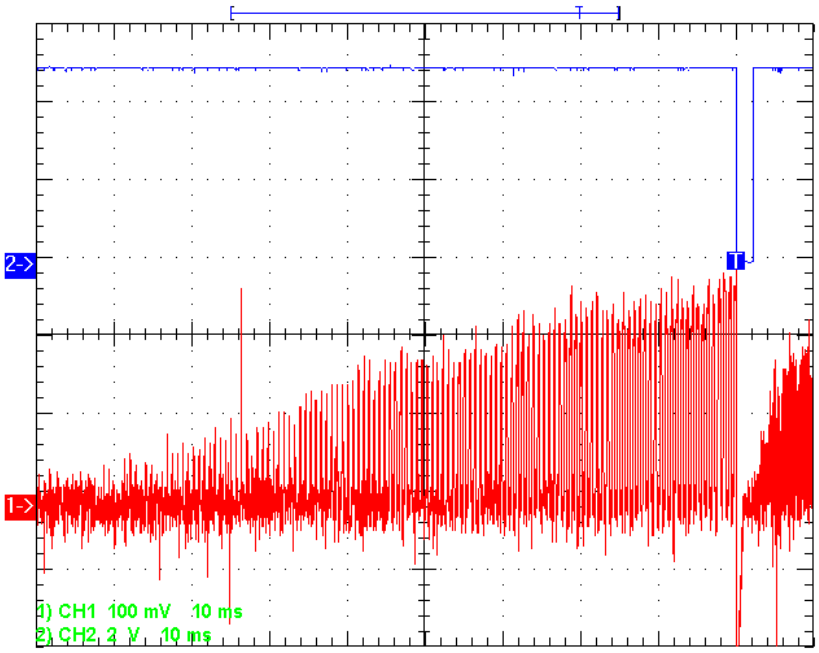
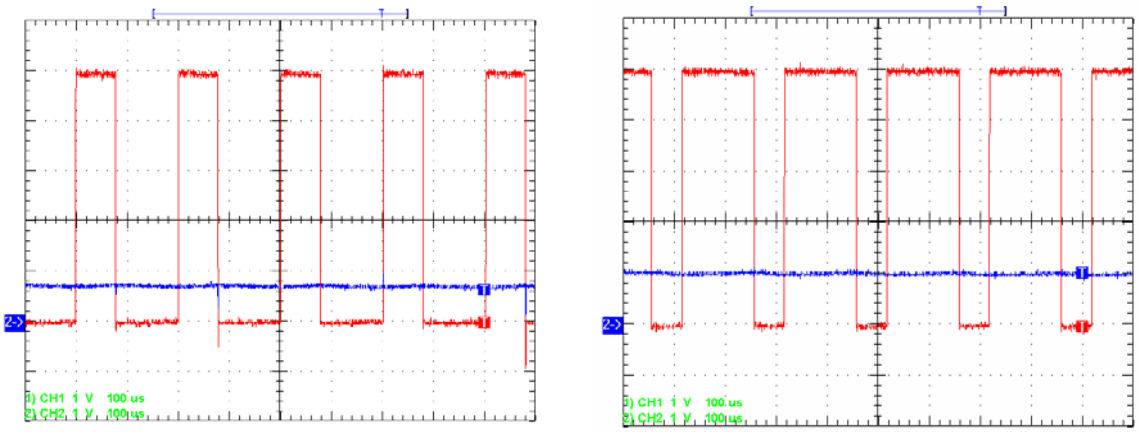
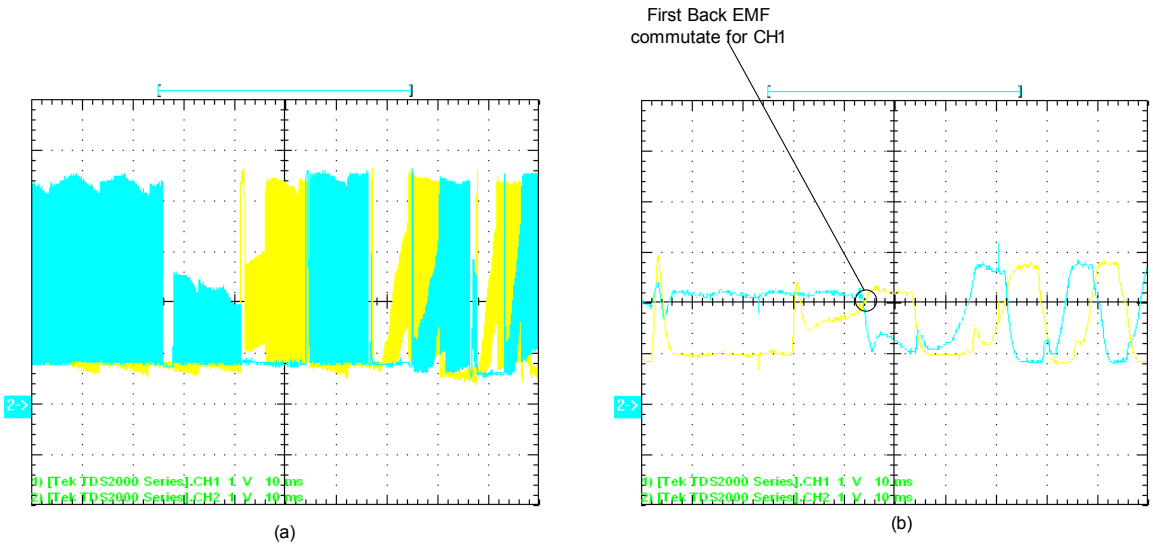


Figure 11. Scope Images for the Compensation Voltage for Two Different PWM Values



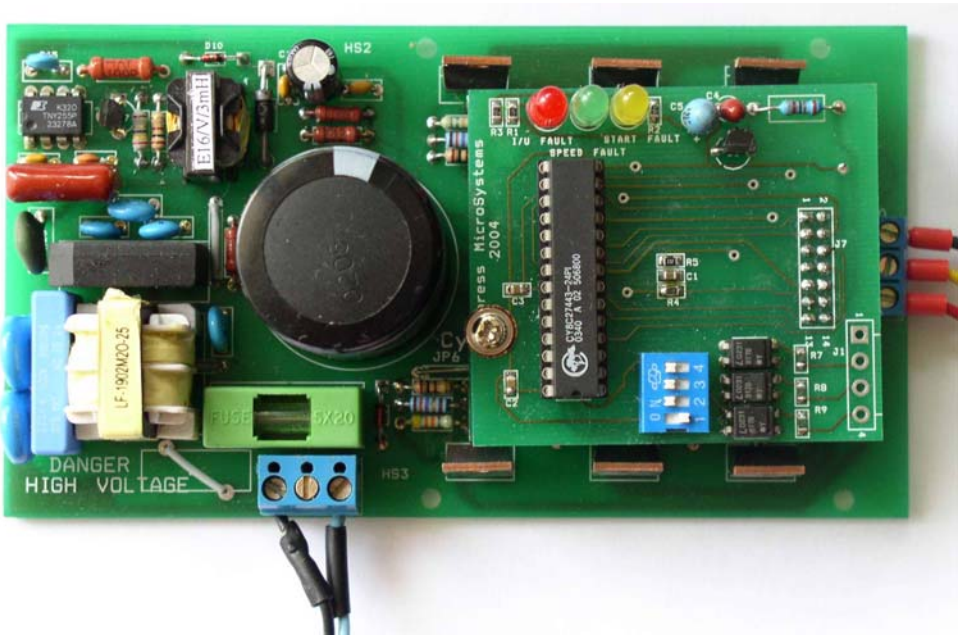
(a) (b)

Figure 12. Unfiltered Back-EMF Signal (a) and Signal After LPF
(b) When Driver Switches from Free-Running Stage to Sensored Stage



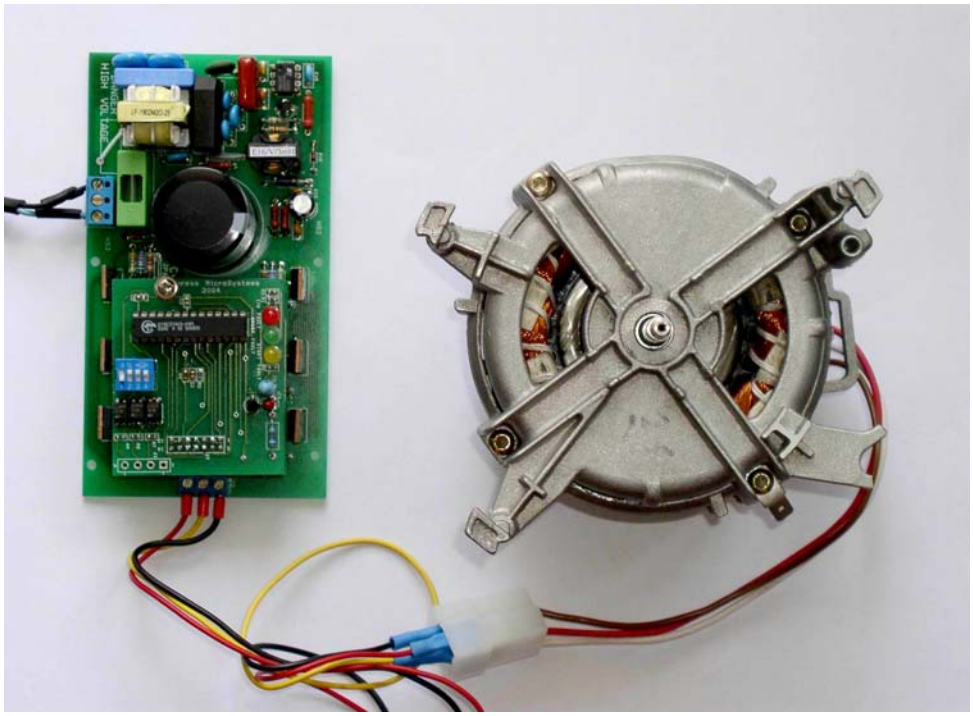
Appendix E. Driver Photograph

Figure 13. Assembled Driver Photograph



Note Driver components are mounted on three separate PCBs to simplify future upgrades and modifications.

Figure 14. Driver Photograph with 75W Motor



About the Author

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