CYWB0224ABS/CYWB0224ABM

Integrating West Bridge® Astoria with ThreadX Reference Design Guide

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Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 880.858.1810
Phone (Intnl): 408.943.2600
http://www.cypress.com

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1. Introduction

This guide provides information on integrating West Bridge® Astoria with ThreadX / FileX. The development was done using Texas Instruments OMAP5912, although the majority of the information contained in this document is not specific to this processor. Software components referenced here were developed and tested on the OSK5912 kit interfaced to an Astoria Development Kit.

Astoria is a mass storage controller from the Cypress West Bridge product family. Astoria can support up to two SD/SDIO/MMC+ devices and enables system support for multiple types of storage and SDIO peripherals such as WiFi, Bluetooth, UWB, GPS, DVB-H. Astoria can also support up to16 SLC or MLC NAND devices with up to 4 bit ECC. Built to connect to virtually any embedded processor, Astoria utilizes a flexible processor interface that includes PNAND, ADMUX, SPI and SRAM.

The advantages of Astoria are fully realized with the Cypress provided West Bridge Astoria SDK that eases the processes of integrating the Astoria device into the overall software subsystem of the processor Astoria is interfaced with. The Astoria SDK contains

1. Example HAL layer implementations
2. API source code and documentation
3. Driver source code (Linux low level device driver, block device driver to access media, and gadget USB driver as well as Windows CE drivers)
4. Firmware for configuring Astoria as a USB and Media controller in various configurations
5. Complete documentation of all components

Please contact Cypress Semiconductor for obtaining a copy of the SDK.

ThreadX is a real time operating system (RTOS) designed and licensed by Express Logic that is at the core of many embedded systems. More information can be found at the Express Logic website.

Texas Instruments OMAP5912 is an application processor with an ARM9 core. More information on this processor can be found at Texas Instruments Website. The OSK5912 Development board was developed around this processor by Spectrum Digital. More information on this board can be found at Spectrum Digital website. Cypress has used the OSK5912 integration for many internal and external development efforts.

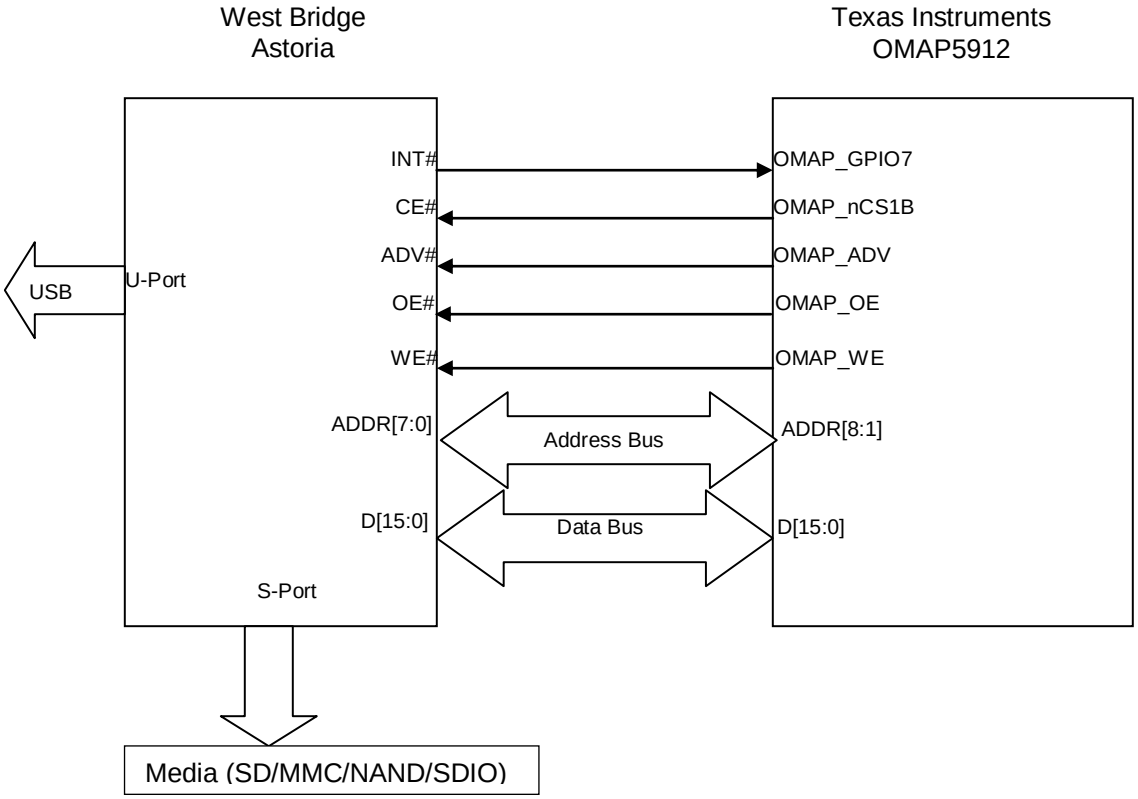
This document is intended to be a guide for the integration of Astoria with any system running ThreadX. The software components referenced and distributed here were developed and tested on the OSK5912, but they can be used as a starting point for any similar combination of hardware and software. The version of ThreadX/FileX used in this testing was 5.1. This integration was done with a focus on FileX, and USB functionality was implemented using direct calls to the Astoria SDK's USB APIs rather than through integration into a the existing ThreadX USB stack.

This guide includes

1. Astoria to OMAP5912 hardware interconnection details
2. Hardware Abstraction Layer Details and Source code (and ISR example)
3. Driver Source Code and Initialization routines.

1.1 Hardware Interconnection Details

This section explains the physical interconnection between Astoria and OMAP5912.



1.1.1 Astoria Hardware Configuration Details

Astoria supports a standard Cellular RAM (CRAM) interface on the processor port (P-Port). This interface allows Astoria to be connected to the standard SRAM interface of most processors. In the case of the OMAP5912, this interface is referred to as EMIFS. The processor can initialize Astoria, exchange data with a USB-host connected to Astoria's U-port and access the storage devices on Astoria's S-port through this same physical interface. Astoria is configured to CRAM mode by keeping the logic level of the P-Port Interface Configuration Control lines, TEST [2:0], in the low state during Astoria's boot up time. Please note that these lines should remain low during operation.

1.1.2 OMAP5912 Hardware Configuration Details

The OMAP5912 has a hardware Memory Controller unit called EMIFS (External Memory Interface Slow) to interface to memory devices or other peripherals with memory like interfaces. The General EMIFS provides glueless interfaces to different memory devices such as NOR Flash, NAND Flash, SRAM and Compact Flash. The EMIFS provides up to six chip selects. For each chip select, the controller can be configured for one of the supported interface types. The data and control lines are shared for all chip selects. The EMIFS provides for flexible timing settings on a per chip-select basis. Assertion and de-assertion timings of control lines can be individually controlled to match timing requirements of the memory device or peripheral the processor is connected to.

1.2 Hardware Abstraction Layer (HAL) Implementation Details

The HAL provides all of the services needed by the Astoria API from the underlying system. This includes operating system services like memory allocation and debug printing as well as hardware services like interrupt management, DMA and register read and write operations.

A detailed description of HAL implementation and APIs are available in the West Bridge Astoria SDK documentation. Specific details of the implementation for OMAP5912 are given here.

The Chip Select 1B from the OMAP EMIFS is used for the CE# control signal to Astoria from the OMAP5912. GPIO7 on the 5912 is used for the Astoria interrupt line. Additional GPIOs for the WAKEUP and RESET control signals of Astoria should be used in any production implementation of Astoria. For Cypress internal development boards, these signals were connected to switches which is why they are not explicitly listed here. All other control signals used in this implementation are memory specific signals from the EMIFS block.

All hardware configuration, including that of the memory interface and the GPIOs is included in the CyAsHalStart() and CyAsHalConfigureInterrupts() functions. Timing settings of the control lines (Chip Enable(CE), Read Enable(RE), Write Enable(WE), Address Valid (ADV)) used in this implementation are shown in the writes to the “EMIFS_” prefixed registers in CyAsHalStart(). These settings can likely be adjusted for faster access in a production system as the settings shown were used in the case where buffers (with associated delays) were placed between the two chips.

In addition to the standard HAL functions used in all West Bridge HAL layers, an assembly file is included which is an excerpt from tx_initialize_low_level.asm, a standard ThreadX OS file. ThreadX is optimized for real time performance and therefore does not contain standardized methods for drivers to register ISRs with it. This is in contrast to the bulkier operating systems that dominate the mobile market (Linux, Windows CE). As such, it is necessary to modify the low-level interrupt routines directly in order to integrate Astoria. The details of how this was accomplished are shown in the excerpt of the assembly file.

The source code of the implementation is available in the HAL folder in the archive associated with this document.

1.3 Drivers

The cy_fx_westbridge_driver.c file is a West Bridge specific low-level storage driver designed to interface with FileX. It is based heavily on the RAM disk implementation developed by Express Logic and provided as an example with FileX. It implements all basic functionality required such as initialization, read and write, although some functions such as abort were not included in the initial implementation.

The fs_init.c file shows how to initialize the driver and format the attached storage. After this initialization has been complete, higher level FileX calls such as fx_file_write() and fx_file_read() can be used.

Contact Cypress Semiconductor for questions concerning driver source code and support. A technical support case can be created at www.cypress.com/techsupport or talk to Technical Support team at the Toll Free number, +1(800) 541-4736 Ext. 8 (in the USA), or +1 (408) 943-2600 Ext. 8 (International).

Document Revision History

Revision	Issue Date	Origin of Change	Description of Change
**	02/24/2011	ODC	New reference design guide.