Designing in nvSRAM into PLC applications

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A Programmable Logic Controller (PLC) is a specialized computing system widely used to control real-time industrial processes and assemblies. The block diagram of a generic PLC is shown in Figure 1.

Programmable Logic Controller (PLC)

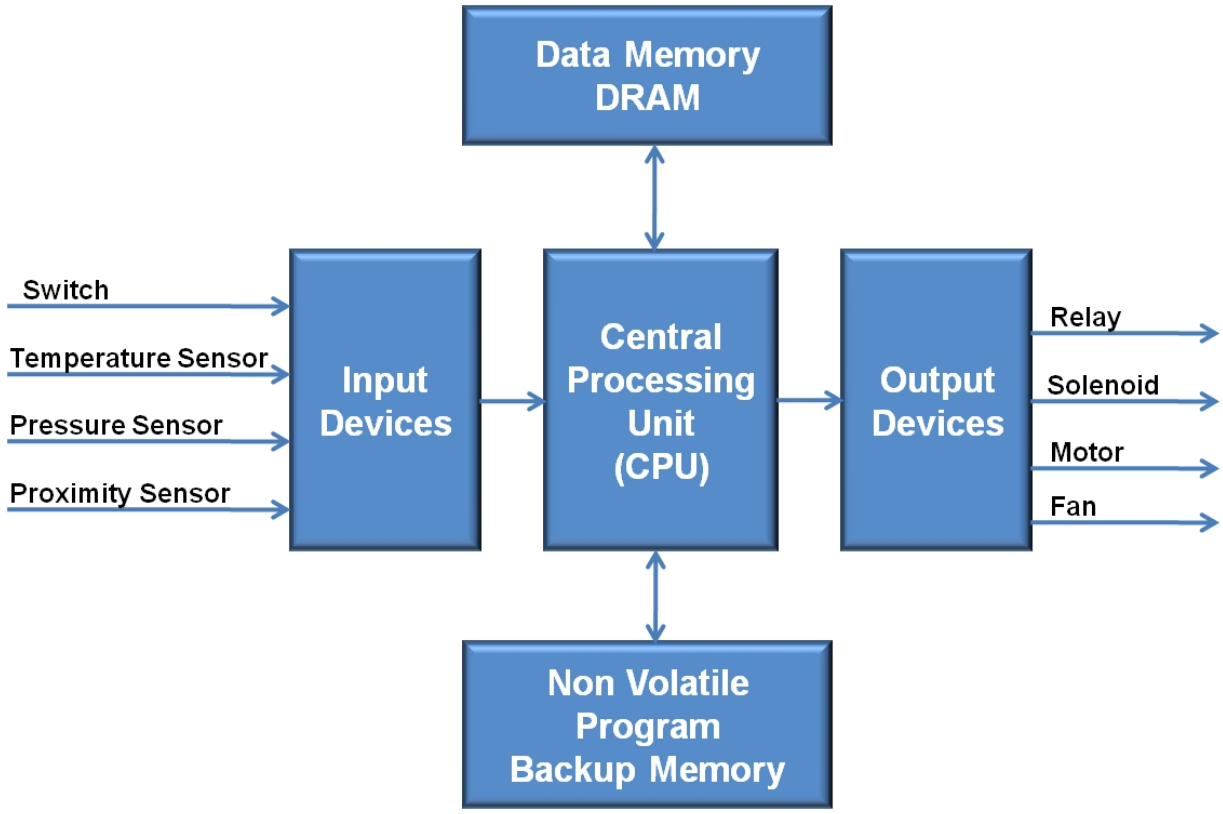

Figure1. Block Diagram of PLC

The PLC scans the states of inputs and controls the states of outputs through a CPU. The user program that has the control logic for CPU is stored in program memory. Examples of inputs are switches, push buttons, and sensors like those used to sense proximity, temperature, pressure, etc. Examples of outputs are relays, valves, solenoid, actuator, motor, fans, alarm, etc. There may also be a communication interface to other terminals in the system.

Most of the industrial automation PLC systems that control the machine operation are real-time systems since the output results must be produced with response to the input conditions within a finite interval time. If the output is delayed, unexpected operation will result which will directly affect productivity and negatively impact revenues.

Such real-time industrial automation PLC systems also require battery-backed or nonvolatile SRAM (nvSRAM) memory to store the programs which control the machine operation. Modern high-performance and high-capacity PLCs also require quick data backup during power failure and a large backup storage capacity on the order of 2MBytes. In case of power failure, the current data being processed must be stored in the nvSRAM without external intervention within the shortest possible time.

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This article addresses how nonvolatile store capabilities and fast access time of nvSRAMs play a significant role in modern high-performance PLC systems.

Eco-friendliness of nvSRAM for PLC systems program storage

When considering semiconductor memory for PLC systems, system designers have many options including, but not limited to, Battery Backed SRAM (BBSRAM), nvSRAM, and other nonvolatile RAM technologies. Existing PLC systems using BBSRAM are easy to use with moderate data retention capabilities. The biggest drawback of BBSRAM is its need for a battery, and hence the system requires maintenance to monitor and replace the battery at regular intervals. In addition, BBSRAMs are expensive, bulky in size, relatively slow in terms of access, and complicate RoHS compliance because of environmental hazard. One can also consider widely used NOR flash for the PLC system's backup memory, but due to its inherent command-oriented architecture, it is not suitable for PLC applications

Using nonvolatile SRAM provides both a low-cost and ecologically friendly approach that is also free from maintenance issues. In today's environmental conscious world, nvSRAM eliminates the requirement for battery replacement and disposal, thus contributing to a more eco-friendly solution with less pollution from discarded batteries and their by-products. The lack of a battery in nvSRAM-based systems also helps designers to reduce PLC system size and cost.

nVSRAM Architecture

An nvSRAM has a stacked (cell to cell) SRAM and Non-Volatile (NV) cell structure. It also has built-in microcontroller and power control circuitry dedicated to monitor the power glitch (or) power failure (see Figure 2). During the power fail (or) glitch, the chip has the intelligence to detect this condition and the contents of SRAM are automatically transferred in parallel into NV cells using a STORE command. The user can also initiate the STORE command from the application. The entire operation takes 8ms (or) less. On power-up, the contents are transferred back to SRAM from NV cells to SRAM using a RECALL command. This provides the system with the data it had before power was lost, and the system can resume the operation without the loss of data. The most versatile nvSRAM devices mostly support STORE / RECALL commands by software initiations and STORE commands by hardware initiation.

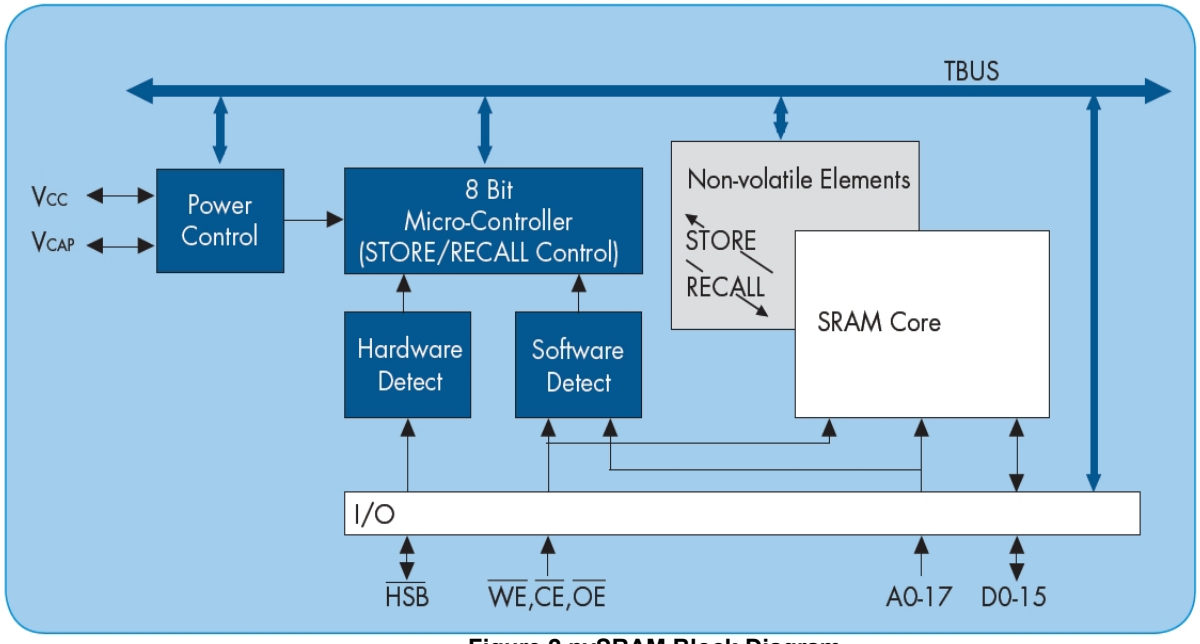

Figure 2.nvSRAM Block Diagram

An nVSRAM behaves likes a SRAM interface with random access. The read/write access time is up to 20ns using a standard SRAM interface and timing. It is guaranteed up to 1 Million STORE cycles for NV elements and for SRAM, the write cycles are infinite. Data can stay unchanged up to 20 years. Table 1 summarizes the design and functional advantages of nvSRAM over BBSRAM technology for a typical PLC system.

Table 1. Comparison of BBSRAM and nvSRAM

BBSRAM	nvSRAM
Requires a battery and therefore imposes environmental hazard and disposal problems	Battery-free for an eco-friendly green design
Requires time-consuming, in-field battery maintenance leading to down-time and added labor costs	No battery maintenance or replacement
Battery vulnerable to environmental conditions such as moisture, shock, and vibration	Not vulnerable to moisture, shock and vibration
Requires more board space and also increases system design complexity	No space for a battery is required, resulting in more functional system design flexibility
For data restore during power-up, SRAM will switch battery power to system VCC supply	Nonvolatile data is made available automatically in the SRAM
Data retention: 7 years	Data retention: 20 years
Access time 70 to 100 ns	Access time 20 to 45 ns

Operating Mode

Auto STORE performs STORE operations in the background during power-down, using zero system time. A small external capacitor guarantees sufficient energy to complete the STORE command when the system power supply drops below the minimum specified operating range. When power returns, data is automatically RECALL'ed from the non-volatile elements into the SRAM once the supply reaches minimum operating levels.

Software STORE and software RECALL may be initiated by a series of reads from six unique addresses clocked with chip enable. Those functions can be used to store new code and data or to perform software reset after the SRAM has been written.

Hardware STORE is initiated by asserting the HSB pin low.

The importance of nonvolatile memory access time in PLC systems

During uncertain sudden power failures, any PLC systems must preserve the current processing real-time data available in system RAM to nonvolatile memory. This operation typically requires a small battery in the PLC system to provide the back-up power to the PLC system. Modern PLC systems use super capacitors rather than batteries for short-term power backup due to maintenance and RoHS issues of batteries.

A super capacitor does not require any maintenance compared to batteries, but the backup time period of the super capacitors is much less. Typically about 100 ms, back-up time can be achieved by super capacitors within a reasonable size. The challenge then becomes to backup data within 100 ms or less during the power failure. This challenge is further increased since PLC systems can require 2 MB capacity of data to be backed up to the nonvolatile RAM from the system RAM. At least 70ms of time is required to transfer the 2MB data from the system RAM to the nvSRAM controller. Within the remaining 30ms, the complete 2MB data from the controller must be written to the nonvolatile memory. This requires a very fast access time of 25ns or less from the nonvolatile memory.

Typical 32-bit nvSRAM interface connection

Figure 3 shows the 2MB nvSRAM connection in 32-bit mode with system memory controller for a typical PLC application.

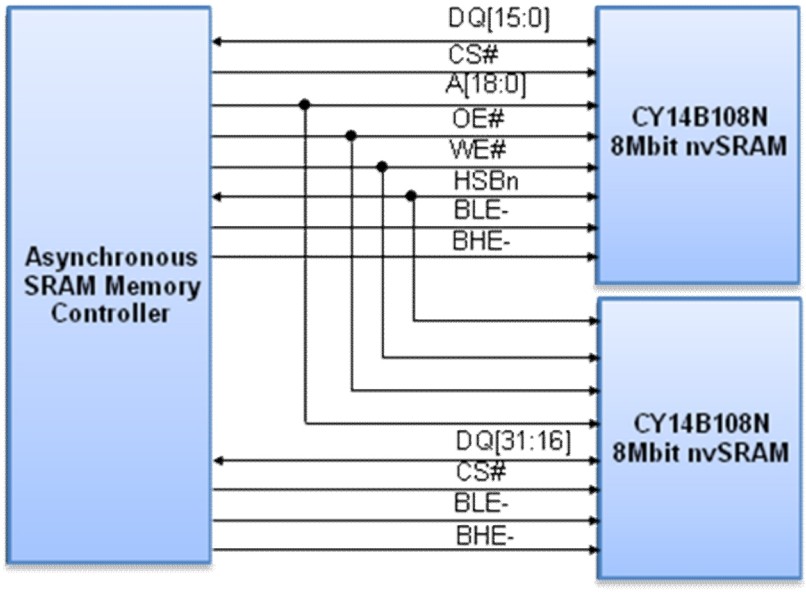

Figure 3.nvSRAM interface connection Diagram

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