



## System Performance Advantages of Higher Density SRAMs

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### Executive Summary

With ever increasing system bandwidth requirements on the order of multigigabits/sec, SRAMs need to be optimized for higher density and performance as well as reliability, especially for look up table and packet buffering in networking applications. This article will address the different factors affecting system performance using Synchronous SRAMs.

With ever-increasing system bandwidth requirements of the order of multigigabits/sec, SRAMs need to be optimized for higher density and performance.

Today, Synchronous SRAMs are used in networking applications, such as L2/L3 caches and buffers, and SRAM performance is a significant factor that contributes to overall system performance. The need for high-density, high-performance SRAMs with high reliability is crucial for networking applications, especially for look-up table and statistics buffers.

Some of the advantages of higher density SRAMs include:

- Reduced board area which can be achieved by replacing two or more lower density parts with a higher density part having the same package footprint
- Increased density to handle more data traffic leading to better system performance
- Fewer interface signals and lower pin count leading to improved signal integrity, timing management, and skew control
- Lower cost
- Lower power
- Lower latency

This article will address the different factors affecting system performance using Synchronous SRAMs. Some of the critical factors that enhance system performance using Synchronous SRAMs are:

- Higher density
- Higher operating frequencies and wider data bus
- Lower latency
- Lower power
- Improved signal integrity

### Higher density

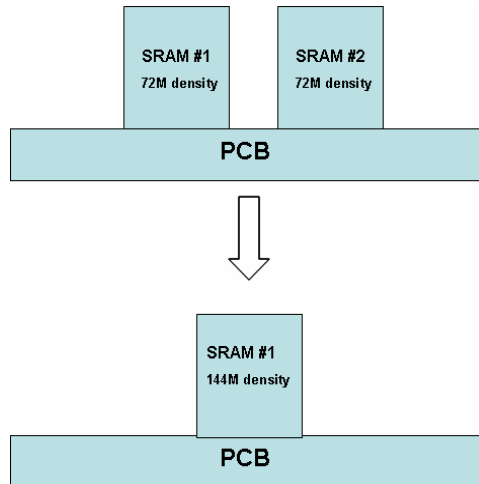
The higher the SRAM memory performance, the better will the system performance.

Higher SRAM memory performance can be enhanced by increasing the operating frequencies and increasing the capacity of storing data.

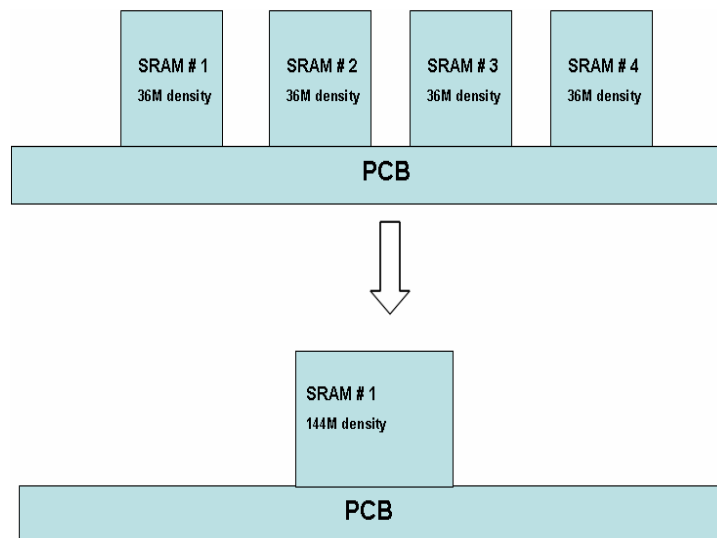
The latter can be achieved by increasing the density of the SRAMs. This enables more data to be buffered as well as increasing the number of transactions that can be performed in a fixed time interval. The greater the transaction speed, the higher the density required for the SRAMs. Therefore, increased density of the SRAMs enables it to handle more data traffic leading to better system performance.

Another advantage of using higher density SRAMs is reduced board space. System designers strive to reduce the board area occupied by the different components for reducing overall board cost. Because SRAM vendors may not be offering the

density required in their applications, system designers often have to use multiple SRAMs to meet the memory density requirements of the system. If higher density SRAMs are available, then 2 or more SRAMs can be replaced by a single SRAM. For example, a single 144M density SRAM can replace two 72M density SRAMs or four 36M density SRAMs mounted on the board thereby reducing board space occupied by the SRAMs (see Figures 1 and 2).



**Figure 1: Two 72M density SRAMs replaced by a single 144M density SRAM**



**Figure 2: Four 36M density SRAMs replaced by a single 144M density SRAM**



## Higher Operating Frequencies and Wider Data Bus

The higher the frequency of the SRAMs and greater the bus width, the better the bandwidth. The more bandwidth, the more number of bits that can be processed per time interval, leading to better performance.

Below is the formula for calculating bandwidth in SRAMs:

### For Single data rate SRAMs:

- Bandwidth = Bus width x SRAM Frequency
  - Example: for a Single data rate Synchronous SRAM operating at 250MHz with a bus width of 36:
  - Bandwidth =  $36 * 250 * 10^6 = 9\text{Gb/sec}$ .

### For Double data rate SRAMs:

- Bandwidth = Bus width x 2(DDR) x SRAM Frequency
  - Example: for a Double data rate Synchronous SRAM operating at 400MHz with a bus width of 36:
  - Bandwidth =  $36 * 2 * 400 * 10^6 = 28.8\text{Gb/sec}$ .

## Lower Latency

Lower latency results from the fact that the higher density part is capable of operating at higher frequencies. Reduced latency enables data to be driven out of the bus faster, leading to increased bus efficiency. Reduced latency also enables more transactions to be performed on the memory within a certain time interval.

## Lower power

One of the main challenges faced by system designers is to lower overall system power. The greater the density of the SRAMs, the fewer SRAMs required to satisfy system density requirements. Reducing the number of SRAMs used also lowers overall power consumption.

Consider the case of the following 2 density SRAMs.

### 144Mb density SRAM with Vdd =1.8V

I<sub>dd</sub> =1070mA

Core power = V<sub>dd</sub> \* I<sub>dd</sub> =1.926W

where V<sub>dd</sub> is the voltage of the core power supply and I<sub>dd</sub> is the operating current

### 72Mb density SRAM with Vdd =1.8V

I<sub>dd</sub> =1000mA

Core power = V<sub>dd</sub> \* I<sub>dd</sub> =1.800W

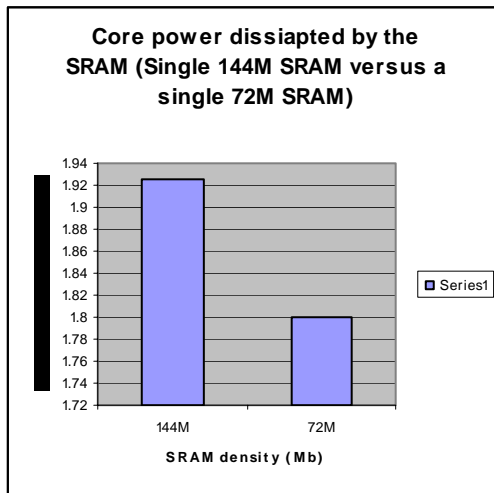
where V<sub>dd</sub> is the voltage of the core power supply and I<sub>dd</sub> is the operating current

Bear in mind that two 72M SRAMs could be replaced with a single 144M SRAM.

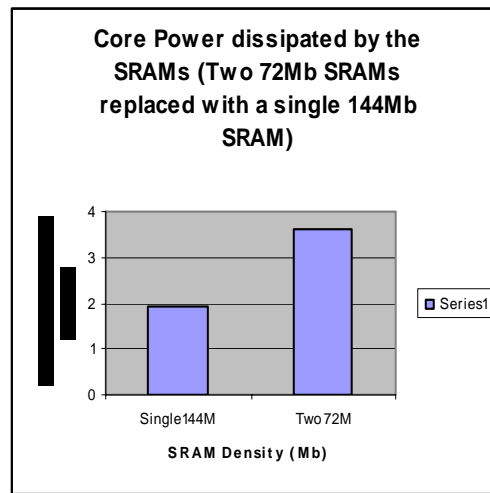
Core power dissipated by two 72M SRAMs =  $1.8 * 2=3.6\text{W}$

Core Power dissipated by a single 144M SRAM = 1.926W

Please refer to Figures 3 & 4 below:



**Figure 3:**



**Figure 4:**

Therefore, though the power consumed by a single 72M SRAM is lower than a single 144M SRAM, the power consumed by a single 144M SRAM is lower than the power consumed by two 72M SRAMs combined by about ~47%.

### ***Improved Signal Integrity***

The higher the density of the SRAMs, the fewer number of interface signals required, thus leading to improved signal integrity at high operating frequencies. This also eliminates the need to clamshell SRAMs to reduce board space, thus making the board routing less complicated and signal integrity better. Fewer traces also reduces crosstalk, thereby improving signal integrity, especially at high frequencies.



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