Implementing DVB-ASI Serial Interfaces Using HOTLink®

Introduction

Digital Video Broadcast - Asynchronous Serial Interface (DVB-ASI) has been widely adopted as one of the standard interfaces for transporting one or more MPEG-2 (Motion Picture Experts Group) transport streams between professional video equipment. DVB-ASI specifies the asynchronous transfer of MPEG-2 transport streams across 8B/10B encoded serial interface at a fixed signaling rate of 270 MBaud (Reference 1). Two different media types are supported: 75Ω coaxial cable and multi-mode optical fiber. The scope of this application note is limited to interfacing to coaxial media, the most popular media type of DVB-ASI.

This application note describes how to implement DVB-ASI serial interfaces using Cypress's HOTLink® chips. The main focuses are the device configuration and the line interface, although some information on the device operation is covered as needed. The ASI requirements are briefly summarized, followed by a discussion on how to implement the ASI interface using both the HOTLink CY7B923/CY7B933 Transmitter/Receiver and the HOTLink II™ transceiver family, such as the Quad HOTLink Transceiver CYP15G0401DXB. This application note also contains some information regarding other components required to meet the DVB-ASI specifications.

Full specifications for the DVB-ASI interface are documented in CENELEC EN 50083-9, Annex B *"Interfaces for CATV/SMATV Headends and Similar Professional Equipment"*. Additional information on the Digital Video Broadcasting standard is available from the DVB Project Office or from the DVB website at, *http://www.dvb.org*.

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DVB-ASI Protocol Description

A logic block diagram of a coaxial cable implementation of a DVB-ASI link is shown in *Figure 1* (Reference 1).

Layer-0 Physical Requirements

The physical layer of DVB-ASI is based in part on the FC-0 and FC-1 physical layers of the ANSI Fibre Channel (FC) Standard X3.230-1994, but at a slightly different signaling rate (Reference 2). ASI requires the encoded line rate to be maintained at 270 MBaud ±100 ppm.

The clock generator within the HOTLink Transmitter takes a byte-rate reference clock (27 MHz) and multiplies it to create the bit-rate clock for driving the serial shifter. At the receiver, an embedded phase-locked loop (PLL) recovers the serial transmission clock by tracking the frequency of the incoming bit stream and aligning the phase of its internal bit-rate clock to the serial data transitions.

In coax implementations, the cable and connector should both have a 75Ω impedance. The connector should also allow operation at frequencies up to 850 MHz. Full electrical details are listed in *Table 1* (Reference 1).

Layer-1 Data Encoding/Decoding

ASI uses a DC-balanced 8B/10B encoding technique that maps 8-bit data bytes to 10-bit character codes. 8B/10B code is a run-length limited code. This means that there are limits on the maximum and minimum length of a continuous sequence of 1s or 0s in the data stream. The minimum span of 1s or 0s is one bit, while the maximum span is five. This code was originally developed for use on fiber-optic links, but has numerous signaling benefits for transmission over copper media as well. Some of the 10-bit characters that are unused after encoding all data characters remain available as special characters. One such special character, K28.5, is employed as the synchronization character for the transmission link.

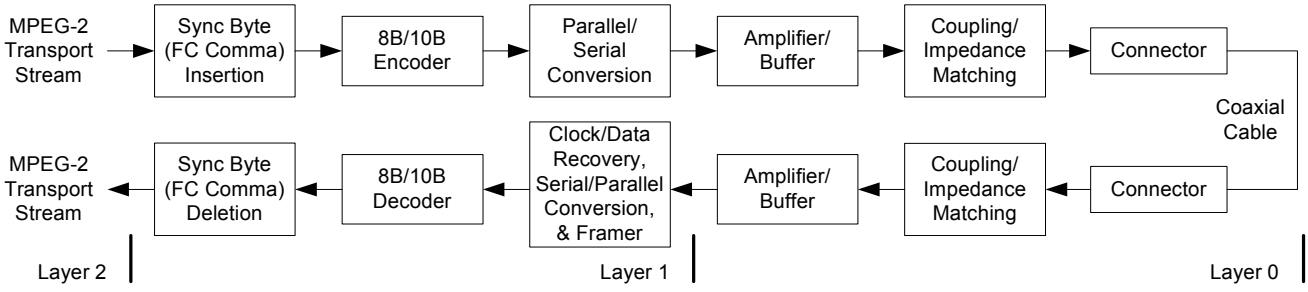

Figure 1. Block Diagram of DVB-ASI Coaxial Cable Based Link

Table 1. ASI Electrical Characteristics

Transmitter Output Characteristics	
Output Voltage	800 mV ±10% (p-p)
Deterministic Jitter	10% (p-p)
Random Jitter	8% (p-p)
Rise, Fall Time (20%-80%)	1.2 ns (max)
Receiver Input Characteristics	
Minimum Input Sensitivity	200 mV
Maximum Input Voltage	880 mV (p-p)
S_{11} (range:0.1 to 1.0 x bit rate)	–17 dB
Min. Discrete Connector return loss (5 MHz - 270 MHz)	–15 dB

Generally, HOTLink requires only one K28.5 character to synchronize the receiver. In DVB-ASI applications, however, the receiver needs to be configured such that the synchronization is performed when two K28.5 characters are received. These two K28.5 characters need to be on the same character boundaries within a five character window. The second K28.5 of the pair will be framed and delivered on the parallel bus. All characters following this K28.5 will also have a valid character alignment. This requirement can be implemented by configuring HOTLink in multi-byte framing mode.

Layer-2 Transport Protocol

ASI Layer-2 transport protocol is similar to the MPEG-2 transport stream packet definition in ISO/IEC 13818-1, with an additional requirement that a minimum of two K28.5 characters should precede every Layer-2 transport packet (Reference 1). This requirement is often overlooked when designing the interface. Having two K28.5s precede every packet ensures that the receiver will resync prior to the start of the next packet whenever loss of sync occurs. A simple state-machine can be designed to insert these two K28.5 characters before each packet.

HOTLink and DVB-ASI

HOTLink chips are designed for point-to-point communications that transfer data over high-speed serial links. Both HOTLink I and HOTLink II family devices comply with DVB-ASI specifications. The following HOTLink chips can be used to implement DVB-ASI serial interfaces:

- CY7B923/CY7B933 HOTLink Transmitter/Receiver
- CYP15G0401DXB Quad Channel HOTLink II Transceiver
- CYP15G0201DXB Dual Channel HOTLink II Transceiver
- CYP15G0101DXB Single Channel HOTLink II Transceiver
- CYP15G0403DXB Quad Channel Independent Clocking HOTLink II Transceiver
- CYP15G04Kxxx Programmable Serial Interface (PSI)

Implementing DVB-ASI Interfaces using the CY7B923/CY7B933 HOTLink Transmitter/Receiver

The CY7B923 and CY7B933 provide interfaces that are simple to design. When configured for DVB-ASI applications, the HOTLink Transmitter accepts the 8-bit parallel data, SC/$\overline{D}$, and SVS signals. It performs the required 8B/10B encoding before serializing the data. The MODE[1]pin should be connected to GND to enable 8B/10B encoding. A 27-MHz reference clock is used for CKW to create a fixed serial signaling rate of 270 MBaud.

CY7B923 outputs serialized data through three differential PECL drivers. Each output pair can be used to direct the serial stream to different destinations or be used as redundant channels. These PECL outputs require proper biasing and termination in order to work properly. A schematic of the transmit interface is shown in *Figure 2*.

The $\overline{ENA}$ and $\overline{ENN}$ inputs control the timing of data acceptance at the parallel interface. If $\overline{ENA}$ is LOW on the rising edge of CKW, the data is loaded, encoded, and sent. If $\overline{ENN}$ is LOW on the rising edge of the CKW, the data appearing on D_{0-7} at the next rising edge of CKW is loaded, encoded, and sent. If both $\overline{ENA}$ and $\overline{ENN}$ are inactive (HIGH), the transmitter inserts K28.5 characters to maintain link synchronization. SC/$\overline{D}$ controls the transmitter to encode the pattern that appears on D_{0-7} as a special character or as a normal 8B/10B data. When SVS is asserted (HIGH), a C0.7 violation signal is sent. HOTLink provides Built-In Self-Test (BIST) functionality which is enabled by driving $\overline{BISTEN}$ LOW. In coax applications, FOTO is generally not used and can be tied LOW.

The serial media interface requires a single-ended signal, at 800 mV ±10% (p-p), launched into a 75Ω transmission line or a matching resistive load. These signals must be source matched with a return loss (S_{11}) of better than 17 dB. The documented amplitude range of the CY7B923 driver is more than the ±10% variation permitted by the standard. Separate line drivers are available that are optimized for this type of signal transmission, such as the MC10EL89, or the CLC006/CLC007. These cable drivers provide the 800 mV ±10% (p-p) output required for standards compliance. While only a single external driver is shown in *Figure 2*, the CY7B923 can support multiple line drivers per PECL output pair. The triple redundant output pairs of the CY7B923 permit a wide array of local and external connections.

DVB-ASI specifies that the line interface should be coupled to the coax via a transformer. The transformer, however, is not electrically needed on either end of the cable. This requirement was originally copied from the ANSI Fibre Channel standard that also specified use of transformer coupling. While the Fibre Channel standard was eventually corrected to allow both capacitor or transformer coupling, the DVB document never tracked the change. As a matter of fact, it is difficult to meet the return loss specification with the transformer in place. To ensure standards compliance, all transmitter designs should be tested for return loss.

On the receiver side, a transformer is used to convert the single-ended signal to a balanced signal. The CY7B933 HOTLink receiver performs the inverse operation of the transmitter. It accepts the serial data stream and performs

Note:
1. 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC}. When not connected or allowed to float, a 3-Level select input will self-bias to the MID level.

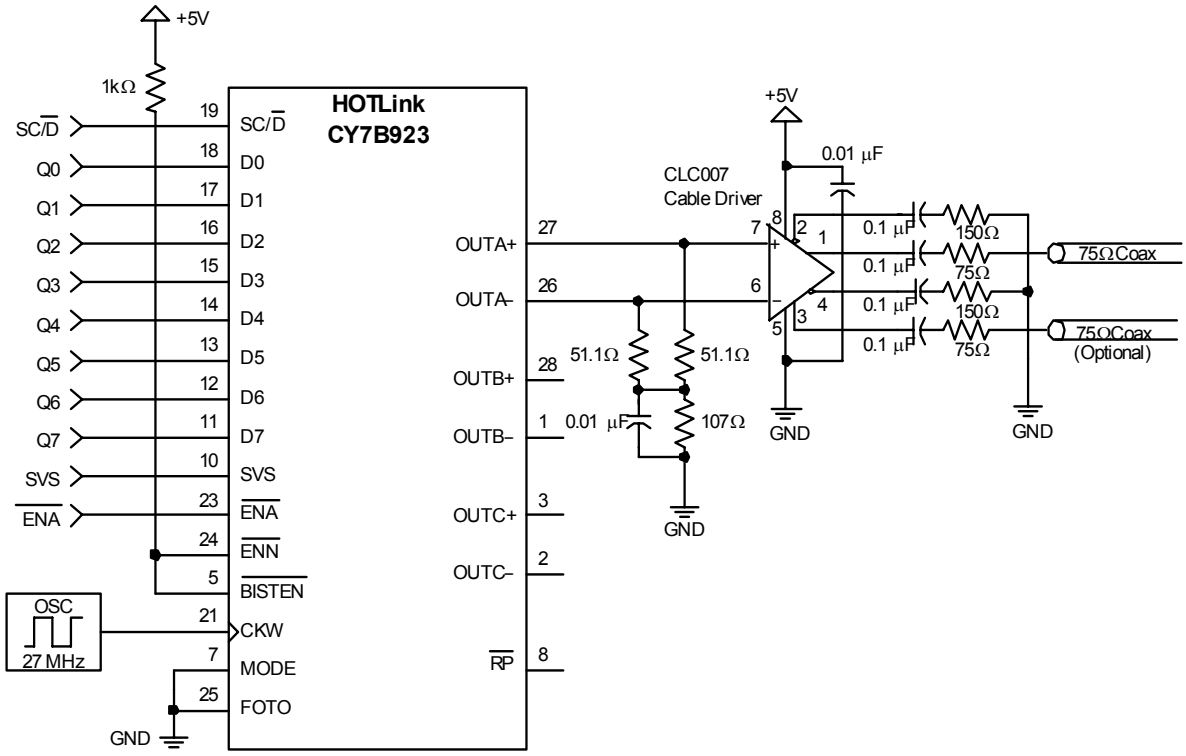

Figure 2. Schematic of a DVB-ASI Transmitter Using CY7B923

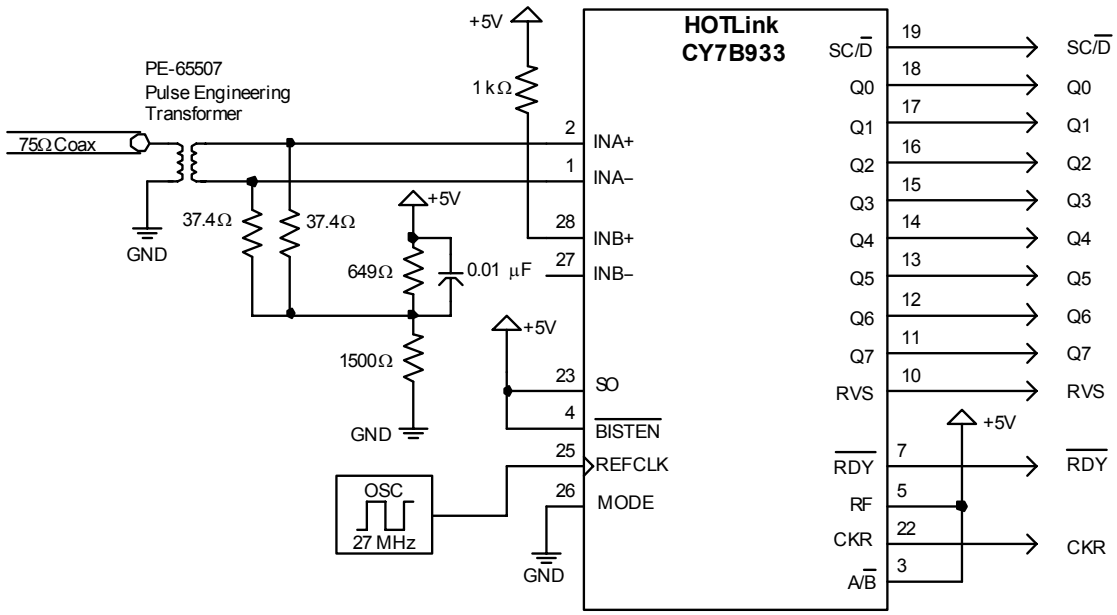

Figure 3. Schematic of a DVB-ASI Receiver Using CY7C933

serial-to-parallel conversion. If enabled, the Framer logic checks the incoming bit stream for the unique pattern (K28.5) that defines the character boundaries. It then passes the data through a 10B/8B decoder, and presents 8-bit parallel characters, along with the SC/$\overline{D}$ and RVS, at the outputs. SC/$\overline{D}$ indicates whether a data or a special character has been received. If the receiver cannot find the character in the valid 10B/8B decoding table, RVS is asserted (HIGH) to indicate that a violation was detected. $\overline{RDY}$ indicates that new data has been received and is available on the output bus. A schematic of the receive interface is shown in *Figure 3*.

The MODE pin on the receiver needs to be connected to GND to enable the 10B/8B decoder. The reference clock (REFCLK) frequency for the receiver needs to be within ±0.1% compared to CKW. Reframe enable (RF) pin is normally tied HIGH to enable multi-byte framing (which is required for compliance to the DVB-ASI specification). Once RF has been HIGH continuously for more than (approximately) 2048 REFCLK cycles, the multi-byte framer is enabled. A/$\overline{B}$ is used to select between INA or INB.

The HOTLink CY7B933 receiver has an input sensitivity of 50 mV which surpasses the minimum sensitivity of 200 mV specified by the ASI standard. Even though HOTLink can operate over greater distance, the maximum cable length is limited by the electrical characteristics as specified by the ASI standard.

If we calculate for a worst case scenario of 720-mV output signal (800 mV–10%) and the 200-mV receiver input sensitivity, the maximum allowed attenuation for the link is approximately 11.1 dB. To see how this number limits the cable length, we can take RG-59/U coax cable type 8281 *(http://www.belden.com*) as an example. The attenuation for this cable is roughly 4.3 dB/100 feet at 135 MHz (270 MBaud). At this rate, the operation length can achieve approximately 250 feet. Passive or active equalization can increase reliable transmission to much longer distances.

In this link, the frequency attenuation characteristics of the copper media are the primary length limiting factors. In reality, the calculation cannot be solely based on the above criteria, considering this calculation does not include the intersymbol interference, connector loss, pcb traces, and other effects that have not been accounted for. All of these effects degrade the signal and serve to prevent a clean signal from reaching the receiver well before the attenuation limit set by the previous calculation. With lower loss cable or a simple compensation filter built from passive components, the operation length can be significantly increased.

Another alternative is to add an adaptive equalizer on the receiver input to compensate for the signal attenuation, as shown in *Figure 4*. An adaptive equalizer, such as CLC014, can compensate for cable loses greater than 40 dB @ 200 MHz. This corresponds to more than 300 meters of Belden 8281 cable. More information is available in the "*HOTLink Copper Interconnect - Maximum Length vs. Frequency*" application note (Reference 4).

Many of the requirements discussed above are not necessarily needed to make the link works. However in order to be compliant, all of these requirements need to be met.

Implementing DVB-ASI Interfaces using HOTLink II Transceiver

When full-duplex operation is needed, HOTLink II provides both transmitter and receiver functions on the same chip. CYP15G0401DXB (Quad Channel) and CYP15G0201DXB (Dual Channel) provide options to have multiple DVB-ASI channels while CYP15G0101DXB can be used as a single channel solution. CYP15G0403DX adds independent clocking capability into the HOTLink II product's portfolio, which allow each channel to operate at an unrelated frequency. CYP15G0401DXB is used as an example for the discussion; however similar line interfaces and pin configurations can be used for the remainder of HOTLink II device family.

Figure 5 shows the schematic of a CYP15G0401DXB-based ASI interface. The part is configured to work similar to the Cypress HOTLink CY7B923 and CY7B933. Most of the control pins in this device can be hardwired or left unconnected for DVB-ASI configuration. *Table 2* lists the pin configuration used in this example and provides an explanation of each pin's function. A full data sheet with pin descriptions for the CYP15G0401DXB may be downloaded from the Cypress website at *http://www.cypress.com.*

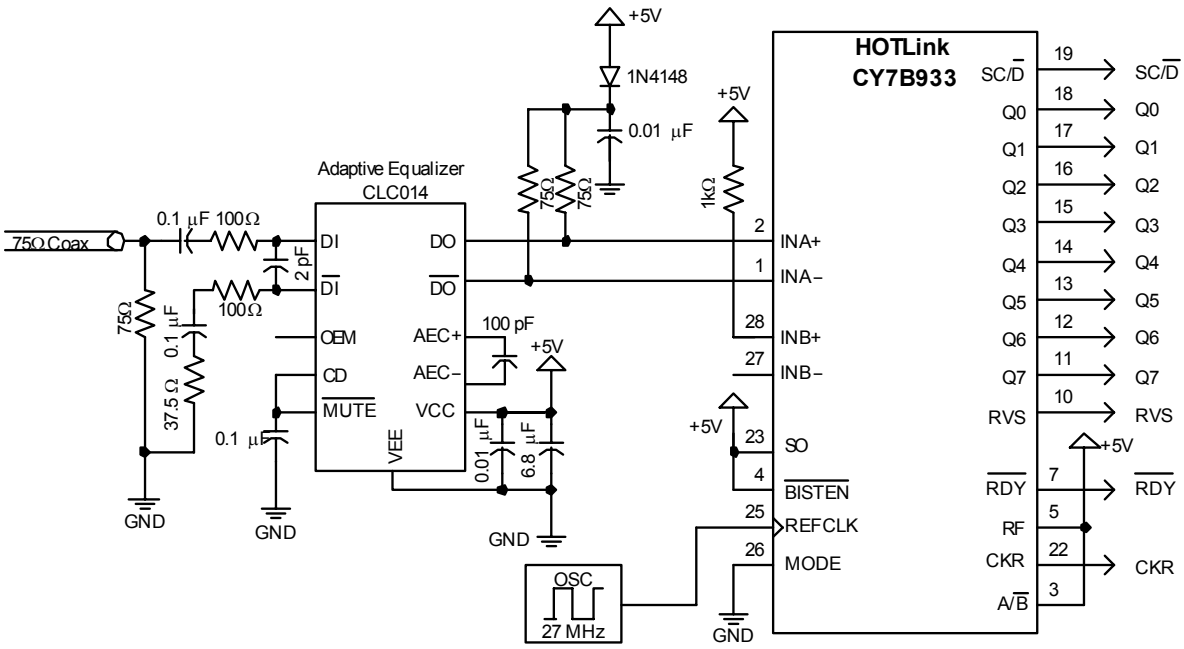

Figure 4. Schematic of a DVB-ASI Receiver Using CY7C933 and Adaptive Equalizer

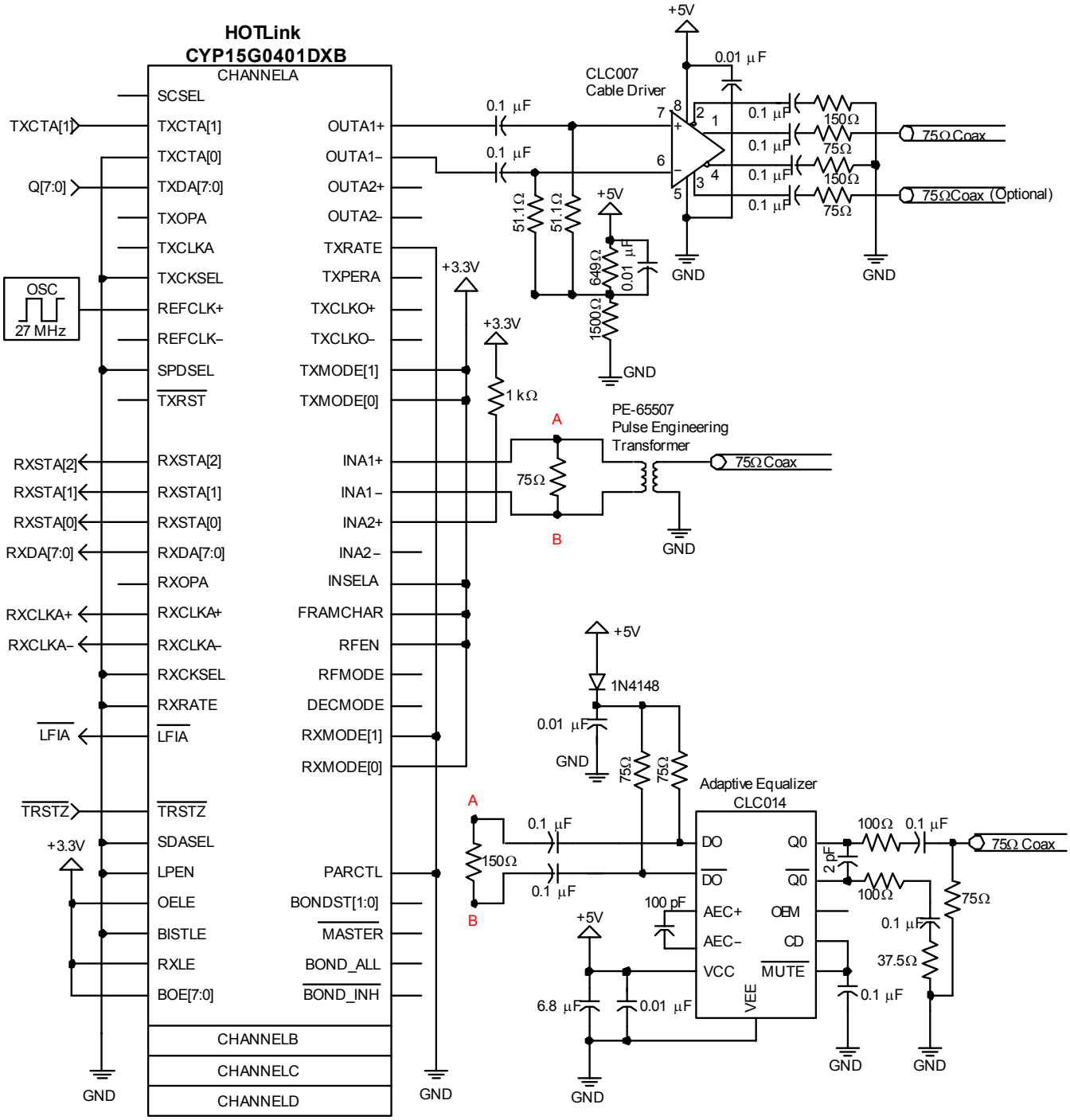

Figure 5. Schematic of DVB-ASI Transceiver SDI Using CYP15G0401DXB[2,3,4,5,6]

Notes:

2. BONDST[1:0], $\overline{\text{MASTER}}$, BOND_ALL, and $\overline{\text{BOND\_INH}}$ pins are not available in CYP15G0201DXB, CYP15G0101DXB, or CYP15G0403DX
3. BOE[7:0] in CYP15G0401DXB and CYP15G0403DX, BOE[3:0] in CYP15G0201DXB, and BOE[1:0] in CYP15G0101DXB
4. CYP15G0101DXB only has a single RXMODE pin to select between Receiver Character Status A or Status B
5. Channel C and D are not available in CYP15G0201DXB; Channel B, C, and D are not available in CYP15G0101DXBT
6. TXMODE, RXMODE, RXLE, DECMODE, RFMODE, RXCKSEL, and TXCKSEL functions has been replaced with latch enable pins (RLE, BYPASSLE, CLKSELLE, and RFMODELE) in CYP15G0403DX. BOE inputs are passed to these latch enable pins to enable/disable certain features. Refer to Table 4 of CYP15G0403DX data sheet for more information on the control latches signal mapping.

Table 2. CYP15G0401DXB Configuration for DVB-ASI Application

Signal Name	Type	Configuration	Function
TXPERx	LVTTL OUT	N/C	Optional output
TXCTx[1]	LVTTL IN	LOW	Use TXCTx[0] only as a transmit control signal
TXCTx[0]	LVTTL IN	TXCTx[0]	Select between sending encoded data or K28.5 character
TXDx[7:0]	LVTTL IN	TXDx[7:0]	TX Parallel Data Input
TXOPx	LVTTL IN	N/C	Not used when PARCTL = LOW
$\overline{\text{TXRST}}$	LVTTL IN	N/C	Not used when TXCKSEL = LOW
SCSEL	LVTTL IN	N/C	Not used in TXMODE 8
TXCKSEL	3-Level Select IN	LOW	Use REFCLK to write data into the transmit input register
TXCLKO±	LVTTL OUT	N/C	Optional output
TXRATE	LVTTL IN	LOW	Use Full Rate clock for TX path
TXCLKx	LVTTL IN	N/C	Not used when TXCKSEL = LOW
TXMODE[1:0]	3-Level Select IN	HIGH, HIGH	Select TXMODE 8, Encoding Enabled (Interruptible)
RXDx[7:0]	LVTTL OUT	RXDx[7:0]	RX Parallel Data Output
RXSTx[2:0]	LVTTL OUT	RXSTx[2:0]	RX Status Output
RXOPx	LVTTL OUT	N/C	Not used when parity function is disabled
RXRATE	LVTTL IN	LOW	Use Full Rate clock for RX path
FRAMCHAR	3-Level Select IN	HIGH	Use full K28.5 character as a framing character
RFEN	LVTTL IN	HIGH	Enable framing
RXMODE[1:0]	3-Level Select IN	LOW, HIGH	RX MODE 2, Non-Channel Bonding Status B Mode
RXCLKx±	LVTTL OUT	RXCLKx±	RX Clock Output
RXCKSEL	3-Level Select IN	LOW	Use REFCLK to transfer data to the receive output register
DECMODE	3-Level Select IN	MID	Use Cypress Decoder table
RFMODE	3-Level Select IN	MID	Use Multi-Byte Framing
PARCTL	3-Level Select IN	LOW	Disable Parity function
SPDSEL	3-Level Select IN	LOW	200-400 MBaud range is selected
REFCLK+[7]	LVTTL IN	REFCLK+	Reference Clock 27 MHz
$\overline{\text{TRSTZ}}$	LVPECL IN	$\overline{\text{TRSTZ}}$	Device Reset pin
OUTx1± OUTx2±	CML DIFF OUT	OUTx1± OUTx2±	Differential Serial Output
INx1± INx2±	LVPECL DIFF IN	INx1± INx2±	Differential Serial Input
INSELx	LVTTL IN	INSELx	Input Select between INx1 or INx2
SDASEL	3-Level Select IN	LOW	Use 140-mV p-p differential to detect valid signal level
LPEN	LVTTL IN	LOW	Disable Loop Enable for normal operation
OELE	LVTTL IN	HIGH	TX Channels Latch Enable
BISTLE	LVTTL IN	LOW	BIST Latch Enable
RXLE	LVTTL IN	HIGH	RX Channels Latch Enable

Note:

7. REFCLK± can accept differential LVPECL clock source or single-ended LVTTL clock source. When driven by a single-ended LVTTL clock source, connect the clock source to either the true or complement REFCLK input, and leave the alternate REFCLK input open (floating).

Table 2. CYP15G0401DXB Configuration for DVB-ASI Application (continued)

Signal Name	Type	Configuration	Function
BOE[7:0]	LVTTL IN	HIGH	BOE, OELE, RXLE, BISTLE work together to turn ON/OFF the channels and BIST mode
$\overline{\text{LFIx}}$	LVTTL OUT	$\overline{\text{LFIx}}$	Link Fault Indicator (Optional Output)
BONDST[1:0]	BIDIR	N/C	Not used in non-channel bonding mode
$\overline{\text{MASTER}}$	LVTTL IN	N/C	Not used in non-channel bonding mode
BOND_ALL	BIDIR	N/C	Not used in non-channel bonding mode
$\overline{\text{BOND\_INH}}$	LVTTL IN	N/C	Not used in non-channel bonding mode

The part is configured in non-channel bonding encoded mode and transmit mode 8. This allows one transmit control pin to select between encoding data or special characters similar to the SC/$\overline{\text{D}}$ pin on CY7B923. If TXCTA[1] is set to LOW, TXCTA[0] selects between encoding data character or sending the K28.5 character. The data can be captured synchronous to the REFCLK or synchronous to the input register clock (TXCLK).

The transmit interface is very similar to the CY7B923 design. One difference is that the CYP15G0401DXB uses a 3.3V power supply instead of the 5.0V required by the CY7B923 design. In order to interface with a cable driver such as CLC007, which uses a 5.0V power supply, the interface needs to be AC-coupled. A DC-restoration and termination network is also required at the input of the cable driver.

The CYP15G0401DXB serial input has internal DC-restoration, thus the only external components needed are the transformer and the termination resistor that is placed across the differential line. An adaptive equalizer can also similarly be used to replace the transformer in order to increase the transmission distance as shown in *Figure 5*. Similar line interfaces can be used for the remainder of the channels with little modifications to the control pins.

On the receiver side, multi-byte framing must be enabled. HOTLink II uses three bits to report the status of the channel while CY7B933 uses SC/$\overline{\text{D}}$ and RVS. While some information may be lost, RXSTA[0] can be mapped as SC/$\overline{\text{D}}$, and RXSTA[2] can be used to report error or violation events (RVS in CY7B933). RX paths can be clocked by the recovered clock from the data stream or synchronous to REFCLK.

If the serial inputs are not used, one half of the differential pair should be connected to V_{CC} through a 1-kΩ resistor to assure that no data transitions are accidentally created. Unused input and output circuitry can also be turned OFF individually to save power through the latch enable pins (OELE, RXLE, and BOEs).

SMPTE and DVB-ASI

The electrical specifications for SMPTE 259M are almost identical to DVB-ASI. For example, both interfaces operate on 75Ω cables terminated with BNC type connectors. They also specify a peak-to-peak launch amplitude of 800 mV ±10% and share a common serial transmission rate of 270 MBaud (SMPTE 259M - C). Since HOTLink is a frequency agile part, it can support other operating data rates specified by the SMPTE 259M standard. HOTLink II also supports SMPTE 292M standard for HDTV.

DVB-ASI data streams are 8B/10B encoded to ensure sufficient transition density in the serial stream, while SMPTE uses scrambled 10-bit characters to also force transitions into the data stream. These differences exist only at the protocol level and do not prevent the possibility of using the same line interface.

The other difference is that DVB-ASI does not specify an operational length requirement, while SMPTE 259M requires operation with up to 300m of RG6 cable. Thus, the configuration with an adaptive equalizer is needed for SMPTE 259M applications. Additional notes regarding SMPTE implementation can be found in the “Implement SMPTE 259M Using the CY7C9235/9335” application note (Reference 3).

Conclusion

HOTLink is capable of generating and receiving DVB-ASI serial data streams and allows you to simplify your design without compromising the flexibility and reliability of the interface. HOTLink’s broad portfolio provides you a selection of devices to suit your application needs.

References

1. *Interfaces for CATV/SMATV Headends and Similar Professional Equipment*, DVB Document A010, October 1995.
2. *Fibre Channel Physical Standard*, ANSI X3.230-1994, American National Standards Institute, 1994
3. *Implement SMPTE 259M Using The CY7C9235/CY7C9335 application note*, Cypress Semiconductor, 1999
4. *HOTLink Copper Interconnect - Maximum Length vs. Frequency application note*, Cypress Semiconductor, 1999

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