Cypress Semiconductor
Product Qualification Report

QTP# 024601 VERSION 1.1
May, 2003

CY22313ZC	**Two-PLL Clock Generator with Direct Rambus™ (Lite) Support**
	E35C-06B Technology, Fab CSM / R42LDHA, Fab 4

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
98357		R42 with Hot Aluminum / 4 Meg, 128K x 36 Pipelined SRAM CY7C1350		Sep 98
IMISM561		Qualification Summary for IMISM561 device , E35C technology, CSM-Singapore		1999
024601		New Two-PLL Clock Generator with Direct Rambus (Lite) Support CY22313ZC		Nov 02

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify CY22313ZC in R42LDHA Fab 4 and E35C-06B technology		
Marketing Part #:	CY22313ZC	
Device Description:	3.45V, Commercial, available in 24-lead TSSOP package	
Cypress Division:	Cypress Semiconductor Corporation – Timing Technology Division (TTD) WA	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A
What ID markings on Die:	E35C-06B 7C80820A	

TECHNOLOGY/FAB PROCESS DESCRIPTION - E35C-06B			
Number of Metal Layers:	3	Metal Composition:	Metal 1,2: 100Å IMPTi/300Å TiN/.5KAlCu/350Å Tin ARC Metal 3: 300Å IMPTi /300Å TiN/.8K AlCu/350Å TiN ARC
Passivation Type and Materials:	350Å TiN/2K PSG/7K Si_3N_4		
Free Phosphorus contents in top glass layer(%):	0%		
Number of Transistors in Device:	8,000		
Number of Gates in Device	2225		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Triple Metal /0.35 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 65Å		
Name/Location of Die Fab (prime) Facility:	Chartered Semiconductor Singapore		
Die Fab Line ID/Wafer Process ID:	2L313-698-CBB/CRA		

TECHNOLOGY/FAB PROCESS DESCRIPTION - R42LDHA			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6000Å Al/.5%Cu/1200Å TiW Metal 2: 500Å TiW/8000Å Al/.5%Cu/300Å TiW
Passivation Type and Materials:	3,000 TEOS + 6,000Å Si_3N_4		
Free Phosphorus contents in top glass layer(%):	0%		
Number of Transistors in Device:	8,000		
Number of Gates in Device	1,400		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Double Metal /0.35 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 70Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R42LDHA		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
24-lead TSSOP	OSE Taiwan (TAIWN-T)

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	Z2411
Package Outline, Type, or Name:	24-lead TSSOP
Mold Compound Name/Manufacturer:	Sumitomo EME7351LS
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated 85% Sn, 15% Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	8360
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-04837
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0mil
Thermal Resistance Theta JA °C/W:	94.2°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-35009
Name/Location of Assembly (prime) facility:	OSE Taiwan (TAIWN-T)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	OSE Taiwan (TAIWN-T), Cypress WA
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max=3.8V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=3.8V, 150°C	P
High Accelerated Saturation Test (HAST)	Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs., 30°C/60%RH+3IR-Reflow, 220°C+5, -0°C	P
Temperature Cycle	Precondition: JESD22 Moisture Sensitivity MSL 1 168 Hrs, 85C/85%RH+3IR-Reflow, 235°C+5, 0°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs., 30°C/60%RH+3IR-Reflow, 220°C+5, -0°C MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C	P
Pressure Cooker	Precondition: JESD22 Moisture Sensitivity MSL 1 168 Hrs, 85C/85%RH+3IR-Reflow, 235°C+5, 0°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs., 30°C/60%RH+3IR-Reflow, 220°C+5, -0°C 121°C, 100%RH	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Acoustic Microscopy	MSL3 Cypress Spec. 25-00104	P
Latchup Sensitivity	125C, 10V, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	2,550	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	471,668 DHRs	1	0 .7	170	12 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] **EFR failure Rate and FIT Rate based on QTP #024601 and QTP #98357**

RELIABILITY TEST DATA

QTP#: 98357

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: ACOUSTIC, MSL3							
CY7C1350-AC	CSPI-R	4815594	619807192	COMP	15	0	
CY7C1352-AC	CSPI-R	4812385	619805289	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.8V							
CY7C1350-AC	CSPI-R	4812418	619805770	48	750	0	
CY7C1350-AC	CSPI-R	4815594	619807192	48	288	0	
CY7C1350-AC	CSPI-R	4815594	619807192	48	396	0	
CY7C1352-AC	CSPI-R	4824383	619809153	48	66	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1352-AC	CSPI-R	4824383	619809153	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 4,400V							
CY7C1352-AC	CSPI-R	4824383	619809153	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 10V, +/-300mA							
CY7C1352-AC	CSPI-R	4824383	619809153	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 3.63V), PRECOND. 192 HRS 30C/60%RH, MSL3							
CY7C1350-AC	CSPI-R	4816713	619808643	128	48	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 3.8V							
CY7C1350-AC	CSPI-R	4812418	619805770	80	392	1	1 UNKNOWN CAUSE
CY7C1350-AC	CSPI-R	4812418	619805770	500	390	0	
CY7C1350-AC	CSPI-R	4815594	619807192	80	396	0	
CY7C1350-AC	CSPI-R	4815594	619807192	548	396	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, MSl3							
CY7C1352-AC	CSPI-R	4816713	619808642	168	45	0	
CY7C1352-AC	CSPI-R	4816713	619808642	288	45	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH, MSL3							
CY7C1350-AC	CSPI-R	4812418	619805769	300	45	0	
CY7C1350-AC	CSPI-R	4812418	619805770	300	45	0	
CY7C1350-AC	CSPI-R	4815594	619807192	300	45	0	

D35C/E35C/F35C base die platform (0.35 uM, 3 layers metal, CMOS, CSM-Singapore)

Test	Military or Industry Standard	Conditions	Test Points	Test Results	Comments
Life Test	MIL-STD-883 Method 1005	150°C/3.3V	168 332	0/116 0/116	Lot C1061-D35C
Life Test	MIL-STD-883 Method 1005	150°C/3.3V	72 596	0/116 0/116	Lot C1024-D35C
Life Test	MIL-STD-883 Method 1005	150°C/3.3V	168	0/116	Lot C1130-D35C
ESD	MIL-STD-883 Method 3015	HBM	2000V 3000V 4000V 5000V	0/3 0/3 0/3 0/3	Lot C1214-D35C
Latch-up	JESD78		200 Ma	0/5	Lot C1214-D35C
ESD	MIL-STD-883 Method 3015	HBM	2000V 3000V 4000V	0/3 0/3 0/2	Lot C1281-E35C
Latch-up	JESD78		200 mA	0/5	Lot C1281-E35C
ESD	MIL-STD-883 Method 3015	HBM	2000V 3000V 4000V	0/3 0/3 0/2	Lot C1189-F35C
Latch-up	JESD78		200 mA	0/5	Lot C1189-F35C

Reliability Test Data

QTP #: 0024601

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.8V, Vcc Max							
CY22356OC (7C822356A)	9220650	*610237934/5/6*	TAIWN-T	48	1050	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 3.8V, Vcc Max							
CY22356OC (7C822356A)	9220650	*610237934/5/6*	TAIWN-T	80	119	0	
CY22356OC (7C822356A)	9220650	*610237934/5/6*	TAIWN-T	500	119	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY22313ZC (7C822313A)	4221029	*610237124/5/6*	TAIWN-T	COMP	9	0	
CY22313ZC (7C822313A)	4221029	*610246619*	TAIWN-T	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY22313ZC (7C822313A)	4221029	*610237124/5/6*	TAIWN-T	COMP	9	0	
CY22313ZC (7C822313A)	4221029	*610246619*	TAIWN-T	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 10V, ±300mA							
CY22313ZC (7C822313A)	4221029	*610246619*	TAIWN-T	COMP	3	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 168 HR 85C/85%RH, MSL1							
CY22313ZC (7C822313A)	4221029	*610237124/5/6*	TAIWN-T	168	50	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 168 HRS 85C/85%RH, MSL1							
CY22313ZC (7C822313A)	4221029	*610237124/5/6*	TAIWN-T	300	49	0	
CY22313ZC (7C822313A)	4221029	*610237124/5/6*	TAIWN-T	500	49	0	
CY22313ZC (7C822313A)	4221029	*610237124/5/6*	TAIWN-T	1000	49	0	