AN217666

PSoC 6 MCU Interrupts

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AN217666 explains the interrupt architecture in PSoC 6 MCU and its configuration using PSoC Creator™ and PDL APIs. This document serves as a guide in developing projects that use interrupts. Advanced interrupt concepts such as interrupt latency, code optimization, and debug techniques are also explained.

Contents

1 Introduction

An interrupt is a hardware signal or an event that transfers the execution of a program from the normal flow to an alternate set of instructions. An interrupt frees the CPU from continuously polling for a specific event, and only notifies and engages the CPU when the event occurs. The alternate program flow is referred to as an interrupt service routine or ISR. An ISR is also called an interrupt handler. After the interrupt is serviced, the program flow is reverted back to the flow that was interrupted. In system-on-chip (SoC) architectures such as PSoC, interrupts are frequently used to communicate the status of on-chip peripherals to the CPU.

While *interrupts* refer to those events generated by peripherals external to the CPU such as timers, serial communication blocks, and port pin signals, an *exception* is an event generated by the CPU such as memory access faults and internal system timer events. PSoC 6 MCU supports interrupts and exceptions on both its ARM® Cortex®-M4 (CM4) and ARM Cortex-M0+ (CM0+) cores.

1.1 How to Use this Document

This document assumes that you are familiar with the PSoC 6 MCU architecture, and application development for PSoC devices using the Cypress PSoC Creator™ integrated design environment (IDE) and Peripheral Driver Library (PDL). For an introduction to PSoC 6 MCU, see AN210781 - Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity. If you are new to PSoC Creator or PDL, see the Related Resources section for links to some of the available resources.

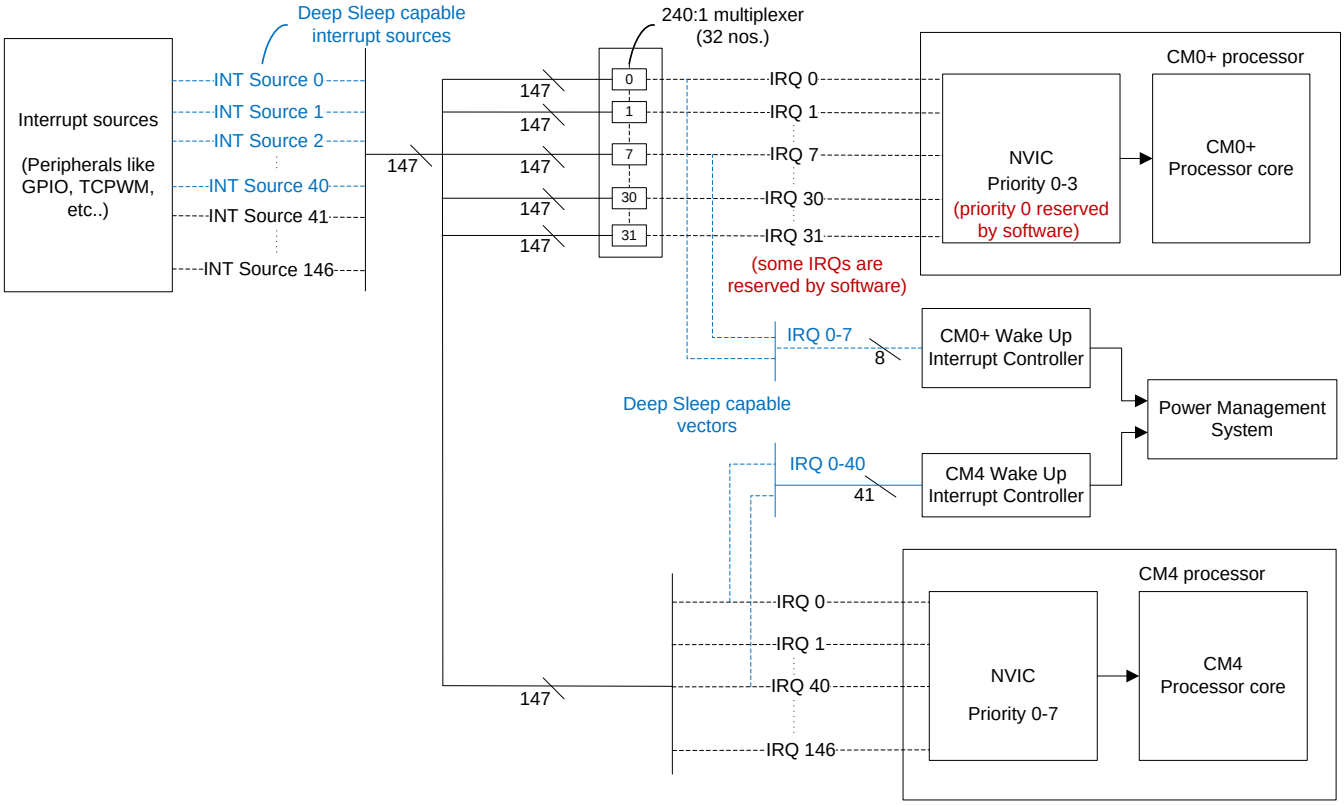
Note: Use PSoC Creator version 4.2 or higher for PSoC 6 MCU-based designs.

This document begins with a brief explanation of the PSoC 6 MCU interrupt architecture, with more details available in the PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual (TRM). To skip to an overview of writing firmware that uses interrupts, see Configuring Interrupts Using PDL or Configuring Interrupts Using PSoC Creator sections respectively. Code examples that show how to use interrupts for various peripherals are listed in the Related Resources section.

The Debugging Tips section provides a few tips on finding and resolving common issues encountered while using interrupts. More complex topics are covered in Advanced Interrupt Topics.

2 PSoC 6 MCU Interrupt Architecture

Figure 1. PSoC 6 MCU Interrupt Architecture



PSoC 6 MCU contains two processor cores: CM4 and CM0+. Interrupt signals to each CPU core are handled by the respective Nested Vectored Interrupt Controller (NVIC). The NVIC enables/disables any interrupt based on the user configuration. It also resolves the interrupt priority when multiple requests occur at the same time and supports nested interrupts to allow a higher-priority interrupt to be serviced before a lower-priority ISR.

There are 147 interrupt sources in a PSoC 6 MCU device. Natively, CM4 supports up to 240 interrupts, while CM0+ supports 32. For CM4, the 147 interrupt sources are directly mapped to its first 147 IRQ lines, i.e., INT source *n* is connected to IRQ *n*, where 'n' = 0 to 146. For CM0+, a 240:1 multiplexer is present in front of each of 32 IRQs and redirects any of the 147 interrupts to one of CM0+ IRQ lines. This enables any interrupt source to trigger any CM0+ IRQ. It is possible to route an interrupt source to both cores. An interrupt source can trigger interrupts on both cores, provided it is routed and the particular core's IRQ is enabled.

CM4 supports configurable interrupt priority from 0 to 7. CM0+ supports priority from 0 to 3.

Note: When using Cypress software (PDL or PSoC Creator), certain software restrictions apply. See Configuring Interrupts Using PDL for details.

PSoC 6 MCU also supports a wakeup interrupt controller (WIC) and multiple synchronization blocks. The WIC block allows the core to wake up from Sleep or Deep Sleep low-power modes using interrupts. The WIC block remains active while the NVIC, processor core, and other device peripherals shut down. When an interrupt triggers, the WIC activates the power management system, which restores the NVIC and the processor core along with other peripherals. Each core has independent WIC settings. In PSoC 6 MCU, the WIC block supports up to 41 interrupts that can wake up a core from Deep Sleep power mode. Table 1 lists the interrupt sources that can wake a core from Deep Sleep.

2.1 Types of Interrupts

There are two kinds of interrupt sources in PSoC 6 MCU:

- Fixed-function interrupt sources

  These are predefined interrupt sources from on-chip peripherals such as GPIO, TCPWM, SCB, and BLE Radio. Interrupts from fixed-function sources are generated from configurable events; for example, an interrupt on a rising edge signal on an input pin (GPIO), or an interrupt on a counter overflow (TCPWM).

- Universal Digital Block (UDB) interrupt sources

  UDBs consist of programmable logic (PLDs), datapaths, and flexible routing, which can be used to synthesize different digital functions such as Timer, PWM, UART, SPI and many more. In contrast to fixed-function interrupt sources, any digital signal generated in a UDB can trigger an interrupt. The signals are routed to the interrupt controller through the routing fabric known as Digital System Interconnect (DSI).

For a complete list of interrupt sources in PSoC 6 MCU, see Appendix A.

2.1.1 Level and Pulse Interrupts

Both CM0+ and CM4 NVICs support level and pulse signals on IRQ lines. The classification of an interrupt as level or pulse is based on the interrupt source. A fixed-function interrupt can only be configured as level. For the DSI sources, which include the UDB, the interrupt can be configured as either rising-edge triggered or level triggered. For more details on selecting the interrupt type, refer to the PSoC Creator Component datasheet or PDL API reference for the particular interrupt source.

For level interrupts, if the interrupt signal is still HIGH after completing the ISR, the interrupt is still pending and the ISR is executed again. Figure 2 illustrates the timing diagram for level-triggered interrupts, where the ISR is executed as long as the interrupt signal is HIGH.

For pulse interrupts, while the ISR is being executed by the CPU, one or more rising edges of the interrupt signal are logged as a single pending request. The pending interrupt is serviced again after the current ISR execution is complete. Figure 3 illustrates the timing diagram for pulse interrupts.

Figure 2. Level Interrupts

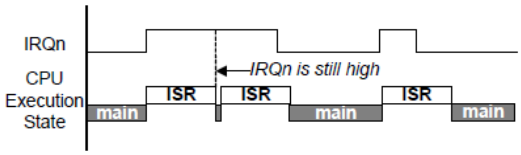
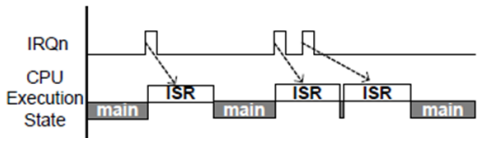


Figure 3. Pulse Interrupts



Note: The GPIO interrupt logic has additional circuitry to support interrupts on the rising edge, falling edge, and both edges**.** See the I/O System chapter in PSoC 6 MCU Architecture TRM for more information.

2.2 Interrupts and Power modes

PSoC 6 MCU has the following power modes: Active, Low-Power Active (LPACTIVE), Sleep, Low-Power Sleep (LPSLEEP), Deep Sleep, and Hibernate.

In Active and LPACTIVE modes, CPU cores execute code; all memory blocks and peripherals are available. LPACTIVE is similar to Active mode, with performance reductions for lower power consumption; peripherals and their interrupts are still available.

In all other power modes, CPU clocks are turned off and CPUs are in Sleep or Deep Sleep mode.

All peripherals available in Active and LPACTIVE modes are also available in the Sleep and LPSLEEP modes. Any peripheral interrupt, masked to the CPU, wakes up the CPU to Active mode.

Only a subset of peripherals operate in Deep Sleep mode. Interrupts from these peripherals cause a CPU to wake up to Active mode. Table 1 lists the peripherals. Each CPU has a Wakeup Interrupt Controller (WIC) to wake up the CPU from its Deep Sleep mode. Deep Sleep wakeup functionality is supported only on the first 8 IRQs (0 to 7) on CM0+ and first 41 IRQs (0 to 40) on CM4.

During Hibernate mode, all peripherals and clocks are turned off and only certain sources like Low Power Comparator, RTC, a dedicated WAKEUP pin, or an XRES event can wake up the device. The wakeup action is a device reset instead of an interrupt to the CPU. For more details on device power modes, refer to AN219528 - PSoC 6 MCU Low-Power Modes and Power Reduction Techniques or PSoC 6 MCU Architecture TRM.

Table 1. List of Deep Sleep Wakeup Capable Interrupts

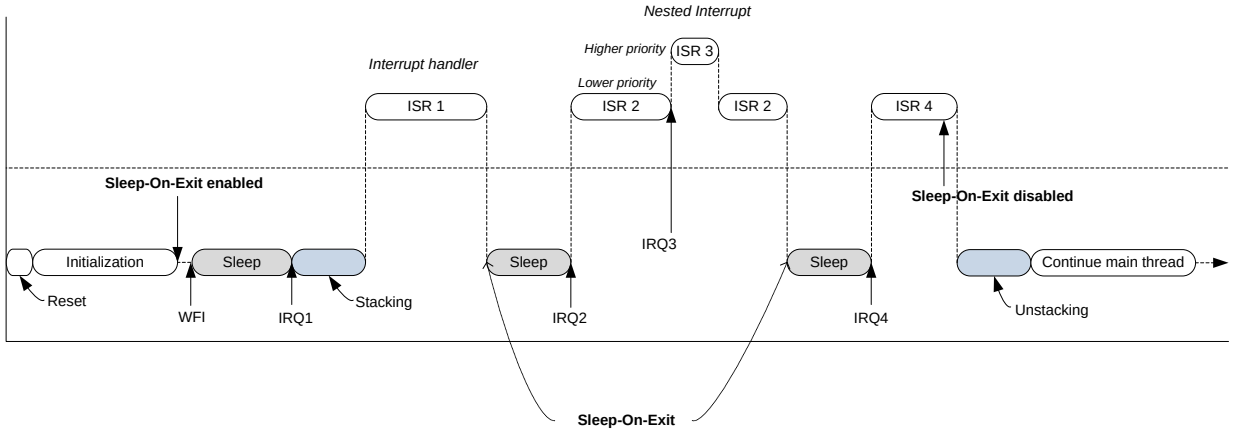
Interrupt Source	Interrupt Source Number
GPIO Port Interrupt (Ports 0–14)	0–14
GPIO All Ports	15
GPIO Supply Detect Interrupt	16
Low Power Comparator Interrupt	17
Serial Communication Block#8 Interrupt	18
Multi Counter Watchdog Timer	19, 20
Backup Domain Interrupt	21
Other combined Interrupts for SRSS	22
Continuous Time Block Interrupt	23
Bluetooth Radio Interrupt	24
Inter Process Communication Interrupt	25–40

CPU Sleep and Wakeup

There are two instructions that can cause the CPU to enter its sleep modes: the “Wait-for-Interrupt” [__WFI()] and “Wait-for-Event” [__WFE()]. When a WFI instruction is executed, the CPU enters Sleep or Deep Sleep (depending on the SLEEPDEEP bit of the SCR register) and wakes up on an interrupt request (with a higher priority than the current priority level) or on debug requests. The WFE instruction is similar to WFI but wakes up on the next interrupt *or* on events like Send Event (SEV instruction), external event, or debug signals. See AN219528 for more details on Sleep and Wakeup instructions.

Normally, when an ISR is done executing, CPU execution returns to where it was before the ISR. PSoC 6 MCU supports the “Sleep-on-Exit” feature where the CPU enters or returns to Sleep or Deep Sleep (a state similar to WFI) as soon as it completes ISR execution. As seen in Figure 4, when this feature is enabled, only one WFI instruction is needed to enter a sleep mode; the CPU returns to sleep after each ISR instead of the execution returning to main. The Sleep-on-Exit feature reduces the active cycles of the CPU and reduces the energy consumed by the stacking (PUSH to stack) and unstacking (POP from stack) of processes between interrupts. Nested interrupts are also supported when Sleep-on-Exit is enabled.

Figure 4. Sleep-on-Exit Function



The Sleep-on-Exit feature is enabled by setting SLEEPONEXIT bit of the SCR register. There is also a PDL function available; see Configuring Interrupts Using PDL.

3 Interrupt Configuration

This section lists the steps needed to set up interrupts on a PSoC 6 MCU device, without going into details of the software used to do them. These steps are common to both CM0+ and CM4 unless specified otherwise, and must be done for each CPU separately.

1. Out of device reset, all interrupts are disabled and interrupt priorities are set to zero.
2. Configure the priority level of the required IRQ in the NVIC.
3. Configure the interrupt path.

   Choose which interrupt source is connected to the desired IRQ of the CPU. For CM0+, configure one of the interrupt multiplexers to select the appropriate peripheral interrupt to be connected to the CPU. For CM4, this is not configurable. Interrupt source *n* is always connected to *IRQn*.
4. Configure the interrupt source (peripheral) and enable its interrupt.
5. Configure the vector table with the address of the ISR (vector). The vector table stores the entry addresses for each exception handler; see the Exception Vector table section in Interrupts chapter of PSoC 6 MCU Architecture TRM.
6. Optional: Clear pending interrupt states in the NVIC.

   If enabling a previously disabled interrupt, it is a good practice to clear the pending state of the NVIC before enabling the interrupt. This prevents any false trigger caused by previous interrupts that created a pending state.
7. Enable the interrupt in the NVIC.
8. Enable global interrupts. Interrupt configuration is complete.

An enabled interrupt is triggered when the hardware signal from the interrupt source is active and there is no higher priority interrupt that is executing. When this happens, CPU execution jumps to the location in its vector table that corresponds to the triggered interrupt. This location contains the address of the ISR associated with that interrupt.

The ISR executes the tasks required to handle the interrupt. Typically, the first thing an ISR does is clearing the interrupt source to avoid re-entering the ISR. When the ISR terminates, the core returns to the address it was executing before it was interrupted.

The following sections describe the software tools available for performing the steps described above.

3.1 Configuring Interrupts Using PDL

Peripheral Driver Library (PDL) v3.0 is a software development kit (SDK) that enables firmware development for PSoC 6 MCU devices. PDL API function calls are used to configure, initialize, enable, and use a peripheral driver. One such driver is System Interrupts (SysInt). SysInt provides structures and functions to configure and enable interrupt functionality. PDL also supports the CMSIS-Core libraries which include NVIC functions used for interrupt configuration.

These steps use PDL and NVIC APIs to set up an interrupt to trigger on a signal from a peripheral.

1. Configure the peripheral to generate the interrupt. For example, for a GPIO, configure the drive mode (pull up or pull down), interrupt signal generation on falling or rising edge, and unmask the interrupt. Refer to the PDL API reference documentation for your peripheral for this information.
2. Configure the interrupt using the structure provided by the SysInt API.

   The structure is defined in the PDL SysInt driver file *cy_sysint.h*:

```
* Initialization configuration structure for a single interrupt channel */
typedef struct {
    IRQn_Type       intrSrc;     /**< Interrupt source */
#if (CY_CPU_CORTEX_M0P)
    cy_en_intr_t    cm0pSrc;     /**< (CM0+ only) Maps cm0pSrc device interrupts to
intrSrc */
#endif
    uint32_t        intrPriority;   /**< Interrupt priority number (Refer to
__NVIC_PRIO_BITS) */
} cy_stc_sysint_t;
```

   This structure is used to configure the following (see Figure 5 for a quick summary):

   a. Interrupt Source (intrSrc)

      - These are the dedicated interrupt numbers as defined in the device header file *<cy8c63xx_xxx>.h*.
      - This selection depends on which CPU you want to assign the interrupt to.
      - For CM4, this number represents both the interrupt number of the source as well as the CPU IRQ number. Select the interrupt number of the peripheral interrupt you wish to route to the CPU. For example, to route Port 0 GPIO interrupt, assign a value of ioss_interrupts_gpio_0_IRQn (=0).
      - For CM0+, this number represents one of the 32 multiplexers available for routing an interrupt to CM0+. Because each multiplexer is connected to a dedicated CM0+ IRQ line, use this to select the target CM0+ IRQ number. For example, to use multiplexer #4 (CM0+ IRQ#4), use “NvicMux1_IRQn” (=4).

   b. CM0+ interrupt number (cm0pSrc)

      - This parameter is applicable only for CM0+. This represents the interrupt number of the source which is to be routed to the multiplexer selected using the `intrSrc` parameter. Select the interrupt number of the peripheral interrupt you wish to route to the CPU; for example, to route Port 0 GPIO interrupt, assign a value of “ioss_interrupts_gpio_0_IRQn” (=0).

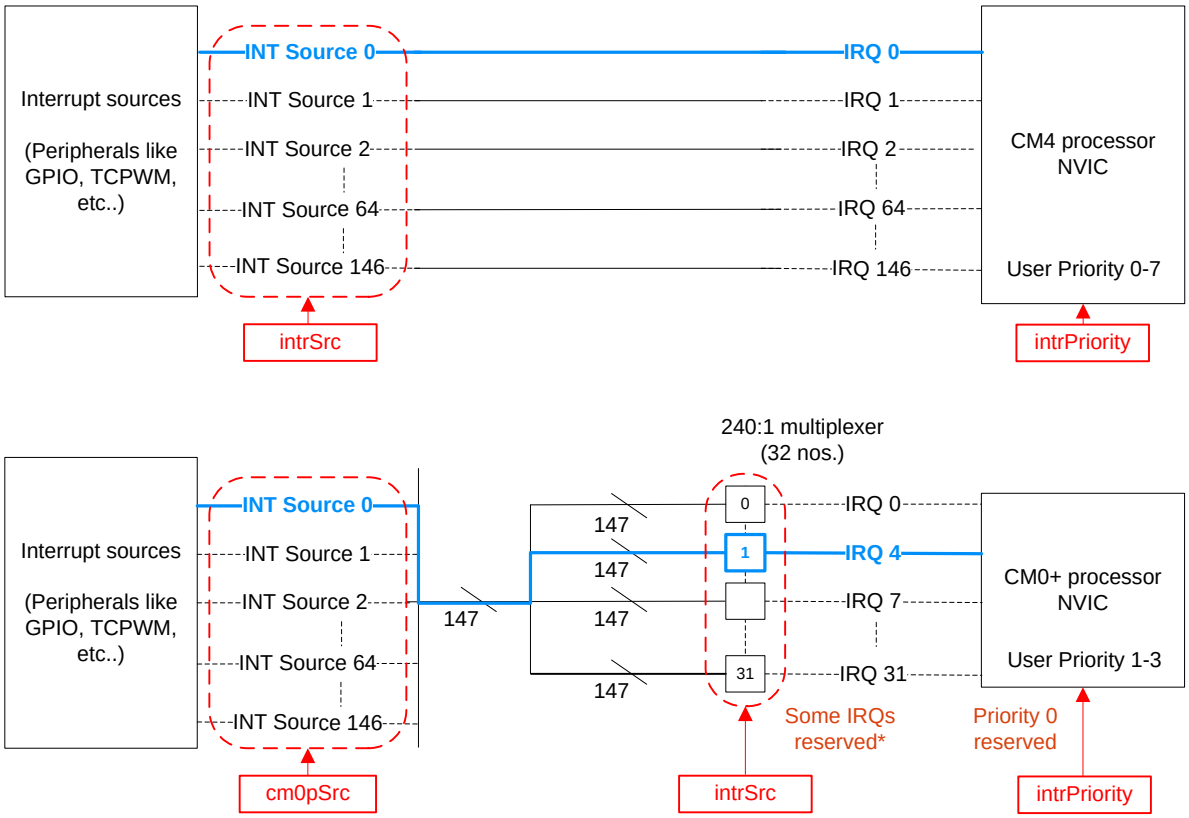
   c. Interrupt priority (intrPriority)

      - Set the priority of the interrupt. For CM4, supported priorities are 0 to 7. For CM0+, supported priorities are 0 to 3.

Notes:

- On CM0+, some IRQs are reserved for use by software and not available to the user. See “Configuration Considerations” under SysInt driver in PDL API reference documentation for the list of reserved IRQs.
- On CM0+, the interrupt priority 0 is reserved for system calls.

Figure 5. SysInt PDL Structure Parameters (highlighted in red) Used for Interrupt Configuration.
A sample configured path is highlighted in blue.



See *PDL API reference > SysInt > Configuration Considerations*

3. Call `Cy_SysInt_Init(&SysInt_SW_cfg_1, ISR_1_handler)`.

   Here, `SysInt_SW_cfg_1` is the name of the configured structure. `ISR_1_handler` is the name of the interrupt handler that executes when the interrupt triggers. This function applies the routing and priority configuration of the interrupt but does not enable it.

4. Call `NVIC_ClearPendingIRQ(SysInt_SW_cfg_1.intrSrc)` to clear any pending interrupts.

5. Call `NVIC_EnableIRQ(SysInt_SW_cfg_1.intrSrc)` to enable the interrupt.

6. Call the `__enable_irq()` function to enable global interrupts. This is safe to perform as the first step, as individual CPU interrupts have not been enabled yet. You can also perform this later but interrupts are disabled at startup unless this is called.

In addition to the PDL SysInt driver, the system power modes (SysPm) driver API enables the Sleep-on-Exit feature. If Sleep or Deep Sleep mode is used in the application along with interrupts, this feature enables the firmware to keep the system in a that sleep mode almost all the time, only wake up to execute the interrupt and then immediately go back to the same sleep mode. The program does not return to the main function and stays either in the interrupt handler or in the same sleep state unless the Sleep-on-Exit feature is disabled again.

```
Cy_SysPm_SleepOnExit(true);
```

3.2 Configuring Interrupts Using PSoC Creator

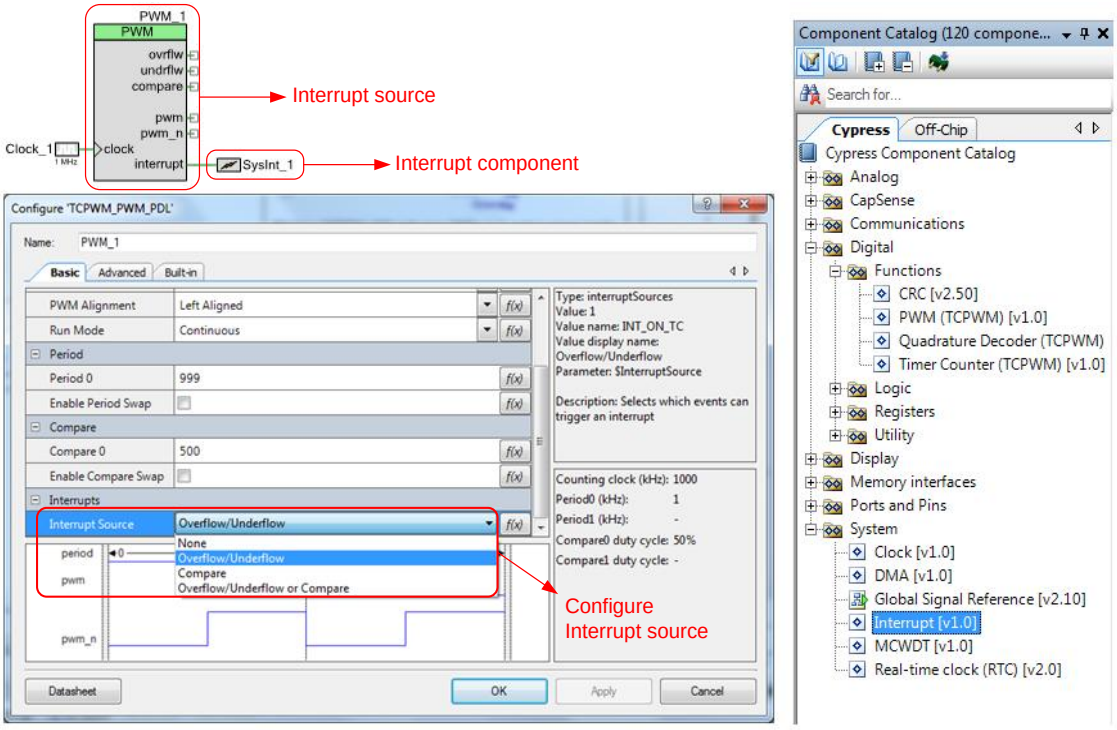
PSoC Creator provides a graphical interface for routing signals from peripherals to a CPU IRQ line. PSoC Creator provides an Interrupt (SysInt) Component**.** This component is a UI element on top of the SysInt PDL driver discussed in the previous section. Based on the configuration in the Component, PSoC Creator generates code to initialize peripherals, route interrupts, and populate the interrupt configuration structure. This reduces the amount of code you must write when setting up interrupts.

The following section shows steps to use PSoC Creator to configure an interrupt. See the Related Resources section for code examples.

3.2.1 Using the Schematic (TopDesign)

Drag and drop a Component from the Component Catalog onto the TopDesign. Use TopDesign to place and configure peripherals that provide a source of interrupt. Consult the Component datasheet for information on the particular peripheral's interrupt configuration. Some peripherals provide an interrupt terminal (e.g., TCPWM). Place an instance of the SysInt Component and connect it to the interrupt terminal of the peripheral.

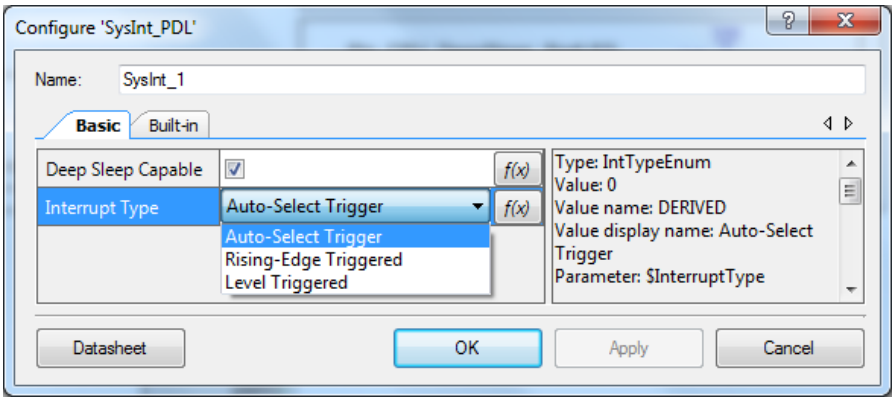
Figure 6. TopDesign with Interrupt Component



Some peripherals do not have an external interrupt terminal (e.g., SCB has interrupts built-in) or may have an option to expose it (e.g., UART).

The Interrupt Component has two configurable options as seen in Figure 7:

Figure 7. SysInt (Interrupt) Configuration



Deep Sleep Capable

Enable this checkbox if you want the interrupt to be assigned to a CPU IRQ line that is Deep-Sleep-capable. You must ensure that the interrupt source is also active and capable of providing the interrupt signal during Deep Sleep, failing which PSoC Creator throws an error when the project is built. Note that this option is significant only in case the interrupt is assigned to CM0+ which has 8 (IRQ 0-7) Deep Sleep slots to route to. The checkbox is provided only for guidance in automatically assigning an IRQ for the interrupt and can be overridden by manual assignment from the CyDWR window. For CM4, if the interrupt source is Deep-Sleep-capable (IRQ 0-40), disabling the checkbox has no effect on the Deep Sleep functionality of the interrupt.

Interrupt Type

There are three options available for Interrupt type in the Interrupt Component configuration: Auto-Select Trigger, Rising-Edge Triggered, and Level Triggered. The selection of a particular option depends on the interrupt source (fixed-function or UDB/DSI) and the application requirements. In most cases, leave the option to Auto-Select to let PSoC Creator derive the interrupt type from the nature of the interrupt source.

Choose only level-triggered for Fixed-function interrupt sources. Choose Level-triggered or Rising-Edge for UDB sources.

3.2.2 Using the Design-Wide Resource Window (CyDWR)

The design-wide resources window (.cydwr file) of the PSoC Creator project has an Interrupts tab. This tab lists the instance names of all interrupts used in the TopDesign schematic along with their interrupt numbers.

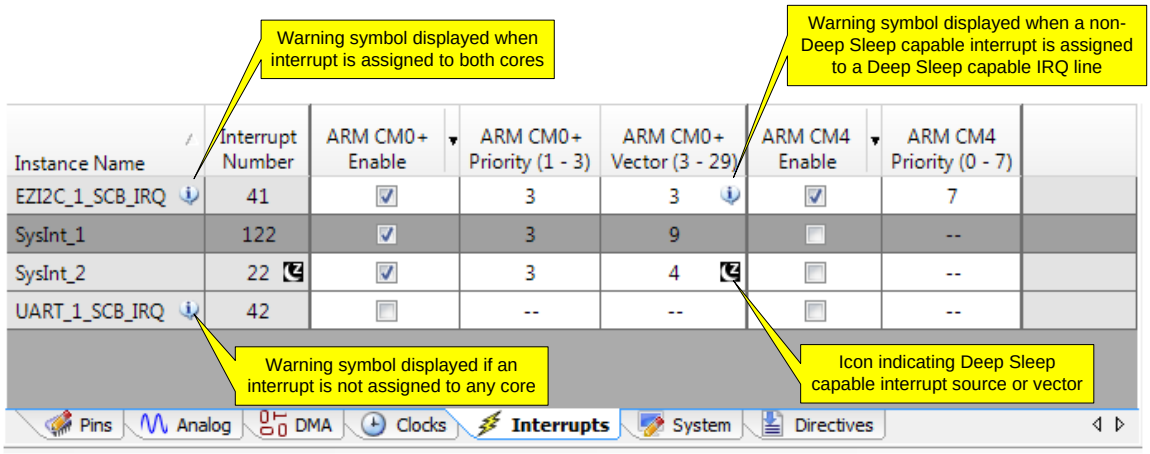
Each interrupt can be allocated to either CM0+ or CM4 or both the CPUs using the ‘ARM CMx Enable’ checkbox. Unless specified otherwise, all interrupts are assigned to CM4 by default. **Though possible, it is not advised to assign an interrupt to both cores unless an application requires it. A warning icon appears in the Instance name column if both cores handle the same interrupt**. A tooltip description of the warning can be viewed on hovering the mouse pointer over the icon.

For CM0+, also assign a CPU IRQ line using the ‘ARM CM0+ Vector’ column. Note that **some CM0+ IRQs are reserved**. PSoC Creator does not allow assigning to these IRQs and will display a warning if done so. There is no option to select the vector for CM4 as these are directly mapped to the corresponding interrupt numbers.

Once assigned to the CPU, assign the priority using the corresponding priority field. CM0+ priority is in the range of 1 to 3, (**priority 0 is reserved** for system calls). CM4 priority is in the range 0 to 7. For both cores, priority 0 corresponds to the highest priority and higher numbers denote lower priorities.

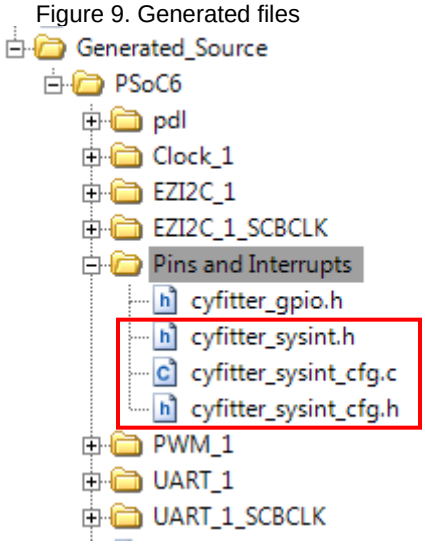
A Deep-Sleep-capable interrupt source or IRQ is indicated using an icon . An info icon appears if a non-Deep-Sleep-capable interrupt is assigned to a Deep-Sleep-capable IRQ line. A build is required to refresh the interrupt numbers and icons.

Figure 8. Interrupts Assignment in CyDwr



3.2.3 Using PSoC Creator Generated Code and PDL

Figure 9. Generated files



Building the project generates code for use in the application. The **Pins and Interrupts** folder contains files with code generated using the information entered in the Interrupts tab in CyDWR.

cyfitter_sysint.h contains macros with information on interrupt number, its CPU core assignment, and priority.

cyfitter_sysint_cfg.c/h declares and pre-populates instances of SysInt PDL configuration structure using the CyDWR information.

The configuration structure for each interrupt is conditionally defined based on the CPU assignment.

The steps to enable interrupts in firmware are similar to the ones listed in the PDL section but fewer in number.

1. Call the `__enable_irq()` API to enable global interrupts.
2. Call `Cy_SysInt_Init(&SysInt_1_cfg, ISR_1_handler)`

- Where `SysInt_1_cfg` is the name of the auto-generated structure from the *cyfitter_sysint_cfg.c* file. `ISR_1_handler` is the name of the interrupt handler that executes when the interrupt triggers. The handler function can reside in the respective CPU's *main.c* to which the interrupt is assigned. If the handler exists outside *main.c*, that file must be compiled and linked into the executable for the core that handles the ISR.

- This step configures the interrupt (routing, priority, and interrupt handler assignment) but does not enable it.

3. Call `NVIC_ClearPendingIRQ(SysInt_1_cfg.intrSrc)` to clear any pending interrupts.
4. Call `NVIC_EnableIRQ(SysInt_1_cfg.intrSrc)` to enable the interrupt.

- You can use PSoC Creator to generate code, and import that into a preferred IDE. AN219434 – Importing PSoC Creator Code into an IDE for a PSoC 6 MCU Project describes how to do that. It is recommended that you use PSoC Creator to set up and configure interrupts in PSoC 6 MCU, export the project to the IDE you prefer and continue developing firmware code with the IDE preferred.

4 Debugging Tips

This section provides tips on trouble-shooting and debugging interrupts. The following are some of the frequently encountered cases:

a. Interrupt is not triggered

- Ensure that the interrupt source and global interrupt are enabled.
- Ensure that the interrupt vector is initialized with correct ISR.
- Check whether other interrupt sources are triggered repeatedly, thus consuming the entire CPU bandwidth.

b. Interrupt is triggered repeatedly

This can happen in multiple cases: Insert breakpoints in the ISR and elsewhere in the program which is expected to execute repeatedly (for example, the super-loop in the main function). If the program is not entering the main function, interrupt is triggered repeatedly.

- The interrupt line from a fixed-function source is connected to a SysInt Component configured to level type.
- Resolution: Clear the interrupt source to resolve this behavior.
- A digital output from the Component (not the interrupt line) is connected to a SysInt Component configured to level type.
- Resolution: Configure the Interrupt Component to rising edge to get one interrupt per rising edge.

c. Execution of the ISR is taking longer than expected

This can happen if other high-priority interrupts are triggered during the execution of the ISR.

Resolution: Increase the priority of the interrupt relative to other interrupt sources.

The PSoC 6 BLE Pioneer Kit has the KitProg2 onboard programmer/debugger. PSoC Creator supports debugging one core at a time (either CM0+ or CM4).

The debug mode is useful for checking interrupts as given below:

- To check if an interrupt is executing, add a breakpoint at one of the instructions in the ISR.
- Use Breakpoint Hit Count to detect the number of times an interrupt is triggered. This is particularly useful to check if the interrupt signal has glitches causing the interrupt to trigger multiple times. To see Breakpoint Hit Count, right-click on the breakpoint, select Hit Count and observe current hit count.
- Use the Call Stack window of the debugger to check program flow to learn when a particular ISR is executed. You can also use it to check if a high-priority interrupt occurred during the execution of a low-priority ISR.

As an alternative to the debugger, you can also use a pin to do the following:

- Check if the CPU is entering the ISR.
- Measure the ISR execution time. This can be done, for example, by asserting the pin in the beginning of the ISR and de-asserting the pin before returning from the ISR. The time for which the pin is HIGH can be measured using an oscilloscope to give the duration of ISR execution.

5 Advanced Interrupt Topics

5.1 Exceptions

Exceptions are the events that cause the processor to suspend the currently executing code and branch to a handler. Interrupts are a subset of exceptions. Besides interrupts, exceptions exist for operating system applications and fault handling.

Exception	Exception Number	Exception Priority	CPUs Supporting the Exception	Description
Reset	1	-3	Both CM0+ and CM4	This exception can occur due to multiple reasons, such as power-on-reset (POR), external reset signal on XRES pin, or watchdog reset. Cortex-M4 execution begins only after CM0+ deasserts the M4 reset. The reset exception address in the SRAM vector table will never be used because the device comes out of reset with the flash vector table selected. The register configuration to select the SRAM vector table can be done only as part of the startup code in flash after the reset is de-asserted.
Nonmaskable Interrupt (NMI)	2	-2	Both CM0+ and CM4	Both cores have their own NMI exception. NMI can be triggered by the following: Any of the interrupt sources, by setting NMIPENDSET bit or using System Calls. NMI exception handler address is automatically initialized to the system call API located in SROM (at 0x0000000C) by the boot code. The value should be retained by the user during vector table relocations; otherwise, no system call will be executed.
HardFault Exception	3	-1	Both CM0+ and CM4	HardFault exception occurs when executing an undefined instruction or accessing an invalid memory addresses.
SVCall Exception	11	Configurable	Both CM0+ and CM4	Supervisor Call (SVCall) is an always-enabled exception caused when the CPU executes the SVC instruction as part of the application code. The SVC instruction enables the application to issue a supervisor call that requires privileged access to the system.
PendSV	14	Configurable	Both CM0+ and CM4	PendSV exception is normally software-generated. PendSV is another supervisor call related exception similar to SVCal.
SysTick Exception	15	Configurable	Both CM0+ and CM4	SysTick is a 24-bit decrementing counter that generates periodic interrupts.
Memory Management Fault Exception	4	Configurable	Only CM4	A memory management fault is an exception that occurs because of a memory protection-related fault.
Bus Fault Exception	5	Configurable	Only CM4	A Bus Fault is an exception that occurs because of a memory-related fault for an instruction or data memory transaction.
Usage Fault Exception	6	Configurable	Only CM4	A Usage Fault is an exception that occurs because of a fault related to instruction execution.

Notes:

- Exception priority that are configurable can be configured from priority 0-3 for CM0+ and 0-7 for CM4.
- Interrupts are also part of exceptions. Interrupt vector number 0 (i.e., IRQ 0) corresponds to the exception number 16, and so on.

5.2 Interrupt Latency

Interrupt latency is defined as the time delay between the assertion of an interrupt and the execution of the first instruction in its ISR. CM0+ has a latency of 15 clock cycles (worst case); CM4 has a latency of 12 clock cycles (worst case). Some peripherals generate additional cycles due to synchronization circuit between the peripherals and CPUs. Table 2 provides the number of CPU clock cycle delays for various peripherals in PSoC 6 MCU.

Table 2. Synchronization Delay for Various Peripherals

Interrupt Source	Synchronization Delay
TCPWM, DMA , USB, I2S, PDM – PCM, CDS	0 clock cycles
SCB, GPIO, LPComp, RTC, WDT, SMIF, BLE	2 clock cycles

When both CPUs are in Sleep/Deep Sleep power mode, there is a need for additional two clock cycles required for synchronization.

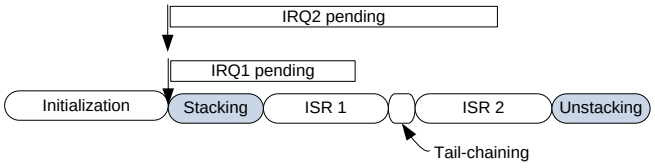
Context switching affects the latency and involves the following steps:

1. Current instruction execution is completed.
2. The processor pushes the current Program Counter (PC), Link Register (LR), Program Status Register (PSR), and some of the general-purpose registers (Program and Status Register (PSR), Return Address, Link Register (LR or R14), R12, R3, R2, R1, and R0) to the stack.
3. The processor reads the vector address from the NVIC and updates it to the PC.
4. The processor updates the NVIC registers.

Thus, the latency varies depending on the current instruction being executed. To make the process efficient, both CM0+ and CM4 processors implement the following two schemes:

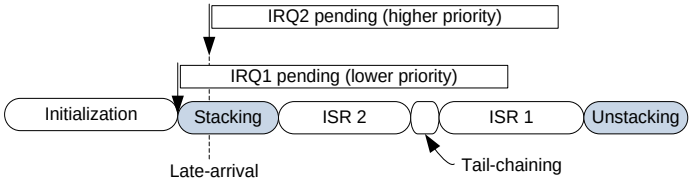
Tail Chaining: If an interrupt is in the pending state while the processor is executing another interrupt handler, unstacking is skipped when the execution ends for the first interrupt and the handler for the pending interrupt is immediately executed. This saves the time of restoring the registers from the stack and pushing the same registers again to stack. This is useful for nested interrupts, as seen in the following section, and for reducing the latency of low-priority interrupts.

Figure 10. Tail Chaining



Late Arrival: If a higher-priority interrupt occurs during the stacking process of a lower-priority interrupt, the processor jumps to the higher-priority interrupt handler instead of a lower-priority one. The processor reads the vector address of the higher-priority interrupt at the end of the stacking process. Once the higher-priority interrupt handler execution is completed, the vector address for the pending lower-priority interrupt handler is fetched and executed. This reduces the latency for a higher-priority interrupt by entering the lower priority ISR and pushing the register values to the stack.

Figure 11. Late Arrival



5.3 Nested Interrupts

NVIC automatically handles nested interrupts without any software overhead. If a higher-priority interrupt is asserted during the execution of a lower-priority interrupt handler, some of the general-purpose registers are pushed to stack, processor core reads the vector address from NVIC and jumps to the higher-priority interrupt handler. After the execution is completed, the processor restores the register values and execution resumes for the lower-priority interrupt.

5.4 Code Optimization

An important performance requirement in interrupt-based applications is the ISR code execution time. In some applications, the critical code in the ISR must be executed within a particular time of receiving the interrupt request. Also, interrupt execution should not take too much time and stall the main code execution or other interrupts. To meet these requirements, use the following guidelines:

- Avoid calls to lengthy functions in the ISR. Functions such as Character LCD display routines or printing long strings to a UART terminal takes long time to execute, thus blocking the execution of other low-priority interrupts. The recommended technique is to move non-critical function calls to the main code and just set a flag variable in the ISR. The main code periodically checks the flag and if set, clears it and calls the function.
- Assign proper priority to the interrupts. In applications with multiple interrupts, give a higher priority to more time-critical interrupts.

  Although AN89610 – PSoC 4 and PSoC 5LP ARM Cortex Code Optimization targets a different CPU architecture, it is a useful reference for general compiler topics.

6 Related Resources

- AN210781 – Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity

  Introduces PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity, a dual-core ARM Cortex-M4 and Cortex-M0+ based Programmable System-on-Chip
- AN219434 – Importing PSoC Creator Code into an IDE for a PSoC 6 MCU Project

  Shows how to import PSoC Creator generated code into your preferred IDE for PSoC 6 MCU firmware
- CE212736 – PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity - Find Me

  Demonstrates a simple BLE immediate alert service (IAS)-based Find Me profile using PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity.
- CE219521 – PSoC 6 MCU - GPIO Interrupt

  Demonstrates how to configure a GPIO to generate an interrupt using PSoC 6 MCU.
- CE219339 – PSoC 6 MCU - MCWDT and RTC Interrupts (Dual core)

  Demonstrates how to configure peripherals to generate interrupts on multiple CPU cores in PSoC 6 MCU.
- PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual

  Provides in depth detail of functional blocks in PSoC 63 with BLE.
- AN89610 – PSoC 4 and PSoC 5LP ARM Cortex Code Optimization

  Reference for general topics on compilers and code optimization.

For the PSoC 6 MCU Family

- The PSoC 6 MCU home page
- The PSoC 6 MCU community

For PDL v3.0

- Peripheral Driver Library v3.0 User Guide (installed with the PDL)
- Peripheral Driver Library API Reference (installed with the PDL)

For PSoC Creator

- PSoC Creator Quick Start Guide
- PSoC Creator User Guide

Appendix A. Interrupt Sources in PSoC 6 MCU

Interrupt Source	Details	Interrupt Number
GPIOs	Each port consists of a maximum of eight pins. Each pin can generate an interrupt, but the vector address is common for all pins in a port. Firmware must identify the pin that caused the interrupt. PSoC 6 MCU enables interrupt trigger on the rising edge, falling edge, or both edges of the GPIO signal. This interrupt can wake the device from sleep, deep-sleep modes.	0 to 14
	There is a GPIO All Ports interrupt that allows combining all port interrupts into a single vector. Firmware must identify the port that caused the interrupt.	15
	There is a GPIO Supply Detect Interrupt that can be used to detect the supply ramping up or ramping down.	16
LPComp	Like GPIOs, an interrupt can be triggered on the rising edge, falling edge, or both edges of the comparator output signal. LPComp can also wake the device from Sleep, Deep Sleep, and Hibernate power modes.	17
Multi Counter Watchdog Timer (MCWDT) interrupt	MCWDT configures two 16-bit counters and one 32-bit counter capable of generating periodic interrupts. MCWDT can wake the CPU from Deep Sleep power mode.	19, 20
Backup domain interrupt	Backup domain interrupt includes the RTC ALARM1, RTC ALARM2, and RTC century overflow interrupt. This can be used to wake the CPU from Sleep, Deep Sleep, and Hibernate power modes.	21
Other combined Interrupts for SRSS	The following cases generate this interrupt: WDT interrupt, Low Voltage Detect (LVD) interrupt, and clock calibration interrupt. WDT interrupt occurs when the watchdog counter value matches the preset Counter Match value. Missing two interrupts will cause a watchdog reset. Low-voltage detect (LVD) interrupt when the device supply voltage drops below a threshold. Clock calibration interrupt is triggered when clock calibration is complete. These are capable of waking the CPU from Deep Sleep.	22
CTBm Interrupt (all CTBms)	This block provides continuous time analog functionality. It generates interrupts on event such as comparator triggers.	23
Bluetooth Radio interrupt	Bluetooth sub-system interrupt	24
IPC Interrupt	IPC interrupts could be triggered when an IPC release or notify event occurs.	25 to 40
SCB	PSoC 6 MCU supports 9 SCBs which can be configured as SPI, I^2C or UART. One SCB interrupt amongst the 8 SCBs is Deep-Sleep-capable. The following events generate an interrupt in a SCB. • TX FIFO has less entries than specified. TX FIFO is not full/ full/ overflow/ underflow. RX FIFO has more entries than the value specified, RX FIFO is full/not empty. • SPI : SPI interrupts are triggered when SPI master transfer done, SPI Bus Error, SPI slave deselected after any EZSPI transfer occurred. • I2C: I^2C master lost arbitration, received NACK, received ACK, sent STOP, I^2C bus error, I^2C slave lost arbitration, received NACK, received ACK, received STOP, received START, address matched. • UART Interrupts : TX received a NACK in SmartCard mode, TX done, Arbitration lost, frame error in received data frame, parity error in received data frame, LIN baud rate detection is completed, LIN break detection is successful.	41 to 48 (Interrupt 18 is Deep-Sleep-capable SCB)
CSD (Capsense) interrupt	CSD, used for touch applications, generates an interrupt when the sensor scan is complete.	49
DMA Interrupt	DMA interrupt can be generated when the data transfer is completed.	50 to 81
CPUSS Fault Structure Interrupt #0	This interrupt occurs when there is a protection unit access violation.	82, 83
CRYPTO Accelerator Interrupt	Crypto Interrupt is generated in the following cases: When a FIFO event is activated, FIFO overflows, true random number generator is initialized, true random number generator has generated a data value of the specified bit size, pseudo random number generator has generated a data value, instruction decoder encounters an instruction with a non-defined operation code, instruction decoder encounters an instruction with a non-defined condition code, when a AHB-Lite bus error is observed, true random number generator monitor adaptive proportion test detects a repetition of a specific bit value, true random number generator monitor adaptive proportion test detects a disproportionate occurrence of a specific bit value.	84

Interrupt Source	Details	Interrupt Number
FLASH Macro Interrupt	Flash controller has a timer that generates interrupts.	85
CM0+ CTI #0	CTI triggers are used to communicate events between debug components.	86, 87
CM4 CTI #0	CTI triggers are used to communicate events between debug components.	88, 89
TCPWM	The TCPWM block can be configured to work as a 16- or 32-bit timer, counter, or PWM. It can generate interrupts on terminal count, input capture signal, or a compare true event.	90 to 121
UDB Interrupt #0	Any digital signal generated in a UDB can trigger an interrupt. Signals are routed to the interrupt controller through the routing fabric known as Digital System Interconnect (DSI).	122 to 137
I2S Audio interrupt	Interrupt can be generated in the following cases. Less entries in the TX FIFO than the value specified, TX FIFO is not full, TX FIFO is empty, attempt to write to a full TX FIFO, attempt to read from an empty TX FIFO, triggers when the Tx watchdog event occurs, more entries in the RX FIFO than the value specified , RX FIFO is not empty, RX FIFO is full, attempt to write to a full RX FIFO, attempt to read from an empty RX FIFO, triggers when the Rx watchdog event occurs.	139
PDM/PCM Audio interrupt	More entries in the RX FIFO than the value specified ,RX FIFO is not empty, attempt to write to a full RX FIFO, attempt to read from an empty RX FIFO	140
Energy Profiler interrupt	This interrupt occurs on a profiling counter overflow.	141
Serial Memory Interface interrupt	This interrupt is activated when TX data FIFIO is activated, RX data FIFO is activated, alignment error, FIFIO overflow.	142
USB Interrupt	The USB block has a predefined set of 13 interrupt trigger events that can be mapped to either one of the three interrupts. Events such as USB Start of Frame (SOF), USB bus reset, data endpoint events, control endpoint events, Arbiter Interrupt Event, and Link Power Management (LPM) event generate interrupts.	143-145
Consolidated interrupt for all DACs	Interrupt can be generated when DAC buffer is empty. This interrupt can be used by the CPU to transfer the next value to the DAC.	146

Document History

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**	5839225	ARVI/ JSLN	09/15/2017	New application note

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