Military Memory

Q3 2017

Cypress Roadmap

Military Memory Portfolio

Military Memory | Single-Event Latch-Up Immune

	Fast Async SRAM	Sync SRAM		Nonvolatile SRAM	F-RAM™	NOR Flash	
	ECC[1]	NoBL®[2], ECC	QDR®[3]II+/IV	Serial/Parallel I/O	Serial/Parallel I/O, ECC	Serial I/O, ECC	Parallel I/O, ECC
64Mb-1Gb			**CY7C41xKV13** **144Mb**; 667–1066 MHz, 1.3 V, x18/x36, Burst 2, M[4] **CYRS26xKV18** **144Mb**, 1.8 V, 450 MHz, x18/x36, Burst 2/4, M **CYPT154xAV18** **72Mb**, 1.8 V, 250 MHz, x18/x36; Burst 2/4, M			**S70/79FL-S** Q118 **1Gb**; 3.0 V, 133-MHz QSPI, Auto E, M **S25FL-S** Q417 **512Mb**; 3.0 V, 133-MHz QSPI, Auto E, M **S25FL-S** Q417 **128Mb/256Mb**; 3.0 V, 133-MHz QSPI, Auto E, M	**S29GL-S** **128Mb-512Mb**; 3.0 V 130ns, x16, Auto E[5], M **S29GL-S** Q317 **128Mb-512Mb**; 3.0 V 130ns, x16, Auto E, M
1Mb-36Mb	**CY7S106x** Q417 **16Mb**, 1.8–5.0 V, 10 ns, x8/x16/x32, Auto E, M **CY7S105x** **8Mb**, 1.8–5.0 V, 10 ns, x8/x16/x32, Auto E, M **CY7S104x** **4Mb**, 1.8–5.0 V, 12 ns, x8/x16, Auto E, M	**CY7C144/6xK** **36Mb**, 133–250 MHz, 2.5 V/3.3 V, x18/x36, M **CY7C137/8xK** **18Mb**, 100–250 MHz, 2.5 V/3.3 V, x18/x36, M **CY7C136xK** **9Mb**, 100–250 MHz, 2.5 V/3.3 V, x18/x36, M		**CY14B116x** **16Mb**; 1.8–3.0 V, 25 ns/45 ns x8/x16/x32, M, RTC[6] **CY14B104x** **4Mb**, 1.8–3.0 V, 25 ns/45 ns x8/x16, Auto E, M **CY14B101x** **1Mb**, 1.8–3.0 V, 25 ns/45 ns x8/x16, SPI, Auto E, M, RTC	**CY15B102N** **2Mb**, 2.0–3.6 V, 60 ns, x16, Auto E, M **CY15B102Q** Q417 **2Mb**, 2.0–3.6 V, 40-MHz SPI, Auto E, M **FM25V10** **1Mb**; 2.0–3.6 V, 40-MHz SPI, Auto E, M		**S29GL-S** Q417 **64Mb**; 130 ns/15 ns, 3.0 V, x16, Auto E, M
64Kb-256Kb				**STK14C88-5** Q219 **256Kb**; 5.0 V, 35 ns/45 ns, x8; QML-Q[7] **STK12C68-5** Q219 **64Kb**; 5.0 V, 35 ns/55 ns, x8; QML-Q			

[1] Error-correcting code
[2] No Bus Latency
[3] Quad Data Rate
[4] Military Temperature: −55°C to +125°C
[5] AEC-Q100 -40°C to +125°C
[6] Real-time clock
[7] Qualified Manufacturers List Level Q, per MIL-PRF-38535

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

CYPRESS EMBEDDED IN TOMORROW™

256Kb Military nvSRAM

Applications

Military communication and real-time controls, avionics real-time controls and high-reliability data logging

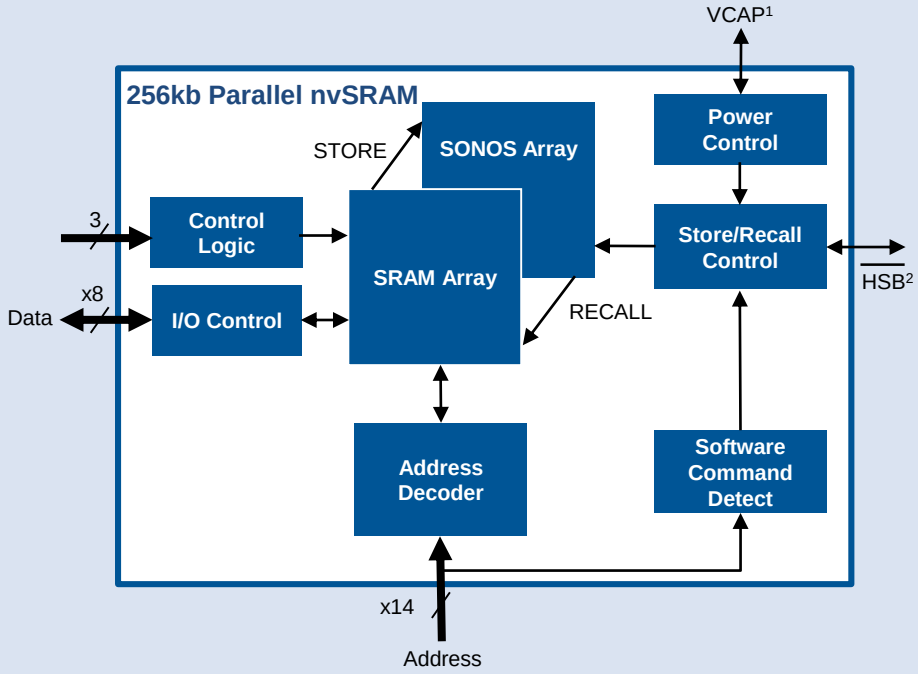
Features

- **Fast Non-Volatile Memory**
  - Access time (35 ns, 45 ns, or 55 ns)
  - Available in parallel interface for 64Kb and 256Kb densities
  - Unlimited read/write endurance
  - One million store cycles on power fail
- **Specifications**
  - 100 years data retention at +85°C
  - Qualified Manufacturers List Level Q (QML-Q certified) per MIL-PRF-38535
  - Military temperature grade: -55°C to +125°C
- **Packages: Ceramic 32-pin DIP, ceramic 32-pin LCC, 28-pin SOIC and 32-pin SOIC**

Collateral

Datasheets: STK12C68
STK14C88

STK14C88: 256Kb nvSRAM



Availability

Sampling, Production: Now
EOL/Last Time Ship: Q2'19

[1] External capacitor connection
[2] Hardware STORE busy

72Mb QDR®[1]-II+ SRAM

Applications

Payload processing and reconfigurable computing platforms

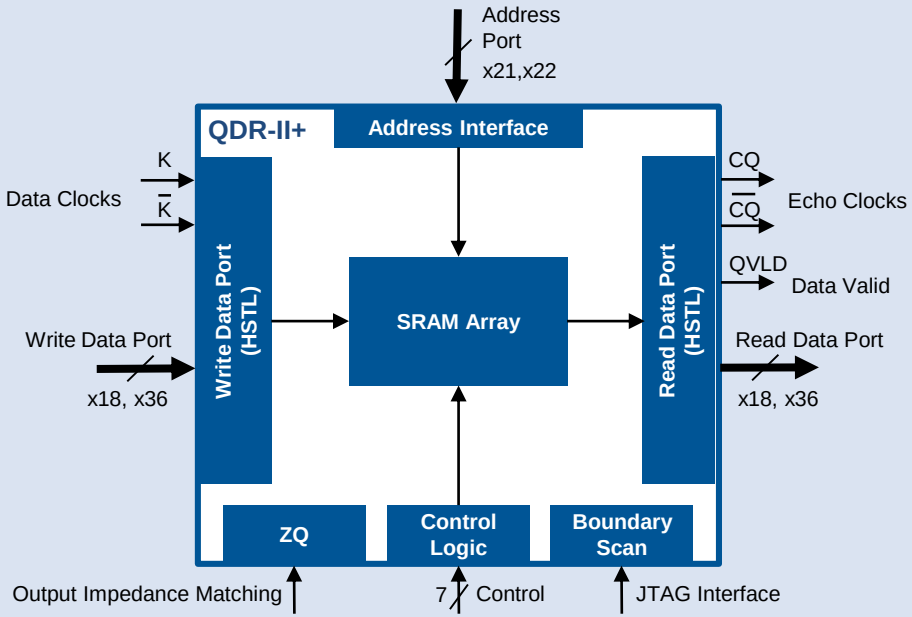
Features

- **High Performance Memory**
  - Maximum frequency of operation/throughput: 250 MHz/36 Gbps
  - Two independent unidirectional data ports for read and write enable concurrent transactions
  - Maximum throughput with double data rate (DDR) data ports
  - Output impedance matching input (ZQ): Matches the device outputs to system data bus impedance
  - Bit-interleaving to eliminate multi-bit errors
  - I/O signaling standards: 1.5–1.8 V (HSTL)
- **Specifications**
  - Burst sizes: 2 or 4
  - Bus-width configurations: x18 or x36
  - Military temperature grade: -55°C to +125°C
- **Controllers available for Altera/Xilinx/Microsemi FPGAs**
- **Package: 165-pin CCGA[2]**

Collateral

Datasheets: CYPT1542AV18/CYPT1544AV18
CYPT1543AV18/CYPT1545AV18

CYPT154XAV18: Military QDR®II+ SRAM



Availability

Sampling: Now
Production: Now

[1] Quad Data Rate: Four data transfers per clock cycle
[2] Ceramic column grid array package

QDR®-IV SRAM

Applications

Switches and routers, high-performance computing, test equipment, military and aerospace systems

Features

- **Highest Performance Memory**
  - Available in two options: High Performance (RTR 1334 MT/s) and Extreme Performance (RTR 2132 MT/s)
  - Two independent, bidirectional double data rate (DDR)[1] data ports
  - Error-correcting code (ECC) to detect and correct single-bit errors (<0.01 FIT/Mb[2])
  - On-die termination (ODT) to reduce board complexity
  - De-skew training[3] to improve signal-capture timing
- **Specifications**
  - I/O Levels: 1.2–1.25 V (HSTL/SSTL) and 1.1–1.2 V (POD[4])
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55°C to +125°C
- **RoHS[5]-Compliant Packages**
  - 361-ball flip-chip ball grid array (FCBGA)

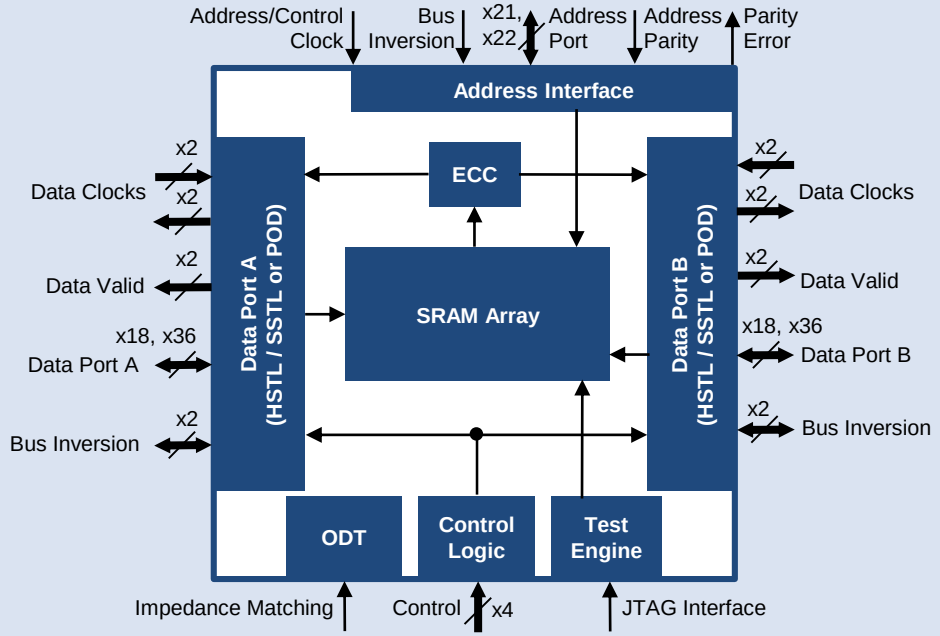
Collateral

Datasheets: CY7C4021KV13/CY7C4041KV13

Family Table

Option	Density	MPN	Maximum Frequency	RTR
QDR-IV HP	72Mb 144Mb	CY7C40x1KV13 CY7C41x1KV13	667 MHz	1,334 MT/s
QDR-IV XP	72Mb 144Mb	CY7C40x2KV13 CY7C41x2KV13	1,066 MHz	2,132 MT/s

QDR-IV



Availability

Production: Now

[1] Two data transfers per clock cycle
[2] The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data
[3] An iterative algorithm for assessing and eliminating the skew (differences in arrival times) between data signals
[4] Pseudo open drain: Signaling interface that uses strong pull-down and weak pull-up

Synchronous SRAM with On-Chip ECC

Applications

Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

Features

- **New Features**
  - Available in two modes[1]: Pipeline and Flow-Through
  - SCD and DCD deselect options[2]
  - Error-correcting code (ECC) to detect and correct single-bit errors
- **Specifications**
  - Voltage options: 2.5V and 3.3V
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55°C to +125°C
- **Packages: 165-ball BGA (with and without leaded balls) and 100-pin TQFP**

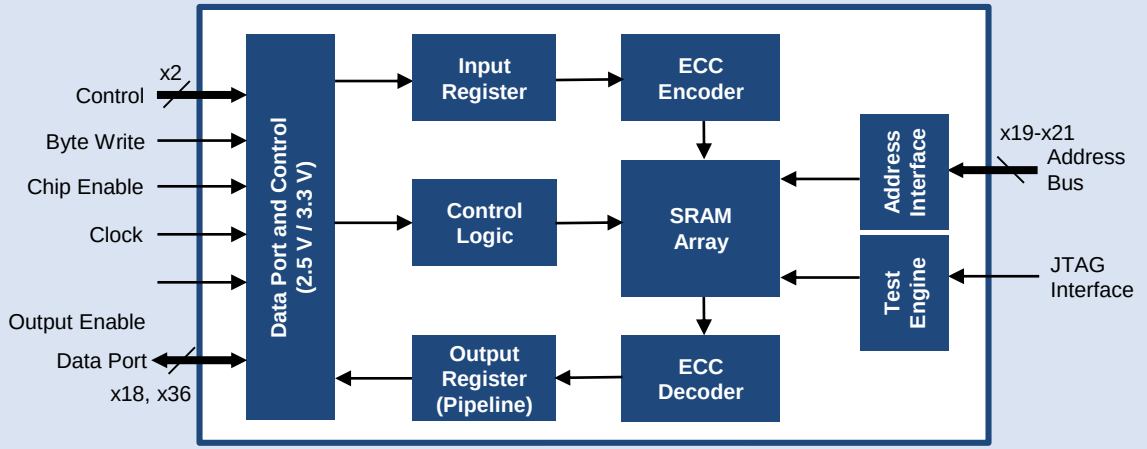
Collateral

Datasheets: CY7C135XKV33/CY7C136XKV33
CY7C137XKV33/CY7C138XKV33
CY7C144XKV33/CY7C146XKV33

Family Table

Option	Density	MPN	RTR	FIT/Mb[3]
Standard Sync with ECC Pipeline	9Mb 18Mb 36Mb	CY7C1360/2K CY7C1370/2K CY7C1440/2K	250 MT/s	<0.01
Standard Sync with ECC Flow-Through	9Mb 18Mb 36Mb	CY7C1361/3K CY7C1371/3K CY7C1441/3K	133 MT/s	<0.01

Synchronous SRAM with ECC



Availability

Production: Now

[1] Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
[2] Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
[3] The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data

Fast SRAM Family with PowerSnooze[1]

Applications

Programmable logic controller, handheld devices, multifunction printers, computation servers and automotive

Features

- **Error Detection and Correction**
  - Error-correcting code (ECC) logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- **Specifications**
  - Access time: 10 ns
  - Deep-sleep current: 15 µA for 4Mb
  - Bus-width configurations: x8, x16 and x32
  - Industrial and automotive temperature grades
  - Military temperature grade: -55°C to +125°C
- **Packages: 48-ball BGA (with and without leaded balls)**

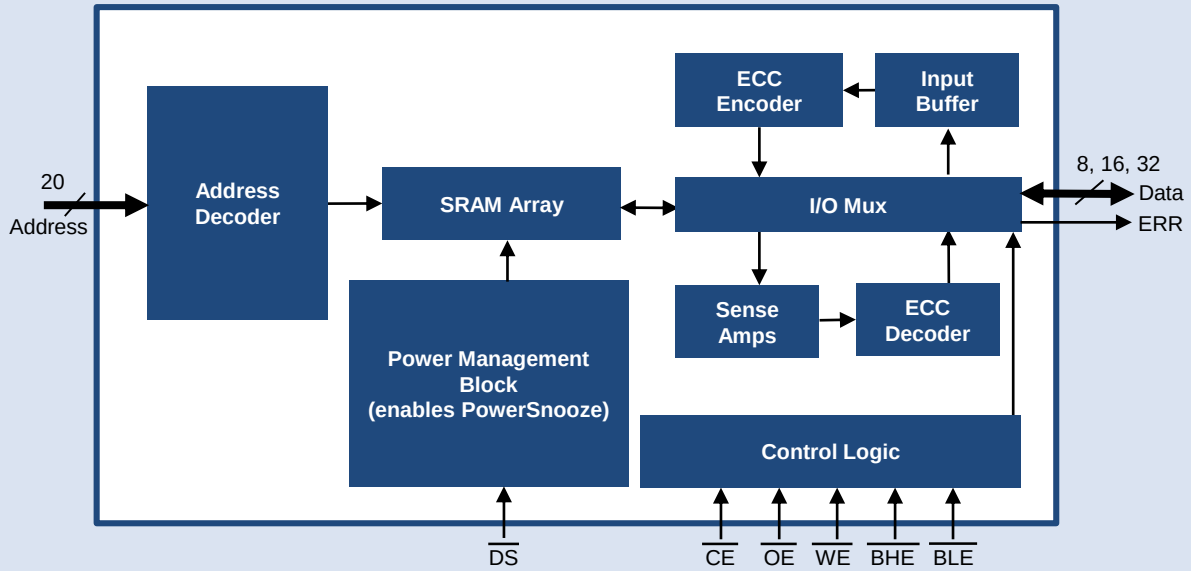
Collateral

Datasheets: CY7S1049G/CY7C1049G
CY7S1059H/CY7C1059H
CY7S1069G/CY7C1069G

Family Table

Density	MPN	Access Time	Deep Sleep Current (maximum at 85ºC)
4Mb	CY7S104x	10 ns	15 µA
8Mb	CY7S105x	10 ns	22 µA
16Mb	CY7S106x	10 ns	22 µA

Fast SRAM with PowerSnooze



Availability

Sampling: Now
Production: Q4'17 (16Mb)

[1] A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode

16Mb Parallel nvSRAM

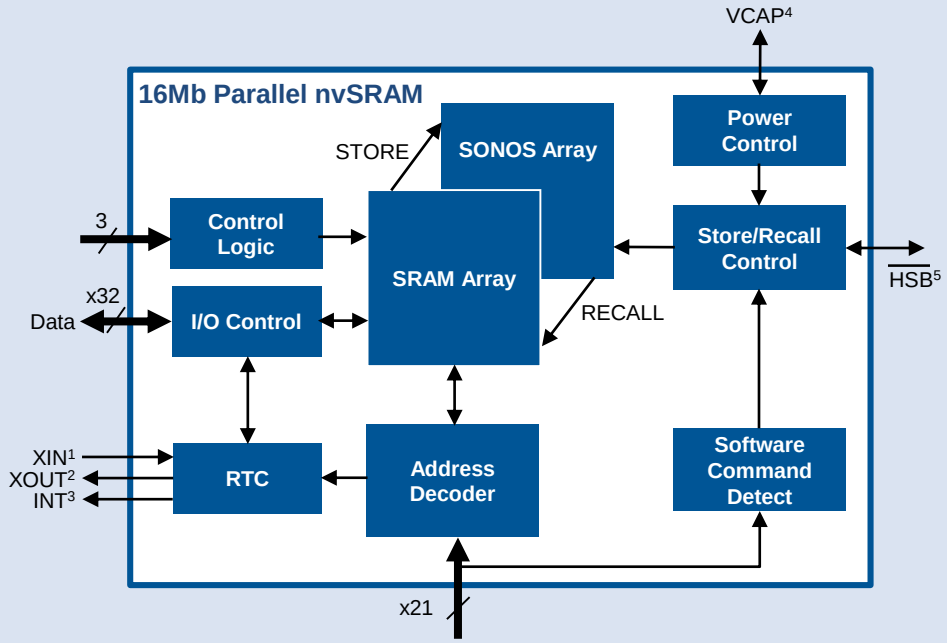
Applications

Industrial automation, programmable logic controllers. gaming machines, industrial data logging, telecom equipment, networking and storage

Features

- **Fast Non-Volatile Memory**
  - Access time (25 ns)
  - Optional real-time clock (RTC) functionality
  - Available in parallel and Open NAND Flash Interface (ONFI) Version 1.0 interfaces
  - Unlimited read/write endurance
  - One million store cycles on power fail
- **Specifications**
  - 100 years data retention at +85°C
  - Qualified Manufacturers List Level Q (QML-Q certified) per MIL-PRF-38535
  - Military temperature grade: -55°C to +125°C
- **Packages: Ceramic 32-pin DIP, ceramic 32-pin LCC, 28-pin SOIC and 32-pin SOIC**

CY14B116: 16Mb nvSRAM



Collateral

Datasheet: CY14X116L/CY14X116N/CY14X116S

Availability

Sampling: Now
Production: Contact Sales

[1] Crystal connection input
[2] Crystal connection output
[3] Interrupt output/calibration/square wave
[4] External capacitor connection
[5] Hardware STORE busy

2Mb Military SPI F-RAM

Applications

Multifunction printers, industrial controls and automation, medical wearables, test and measurement equipment, smart meters, aerospace and defense applications, missiles and launchers

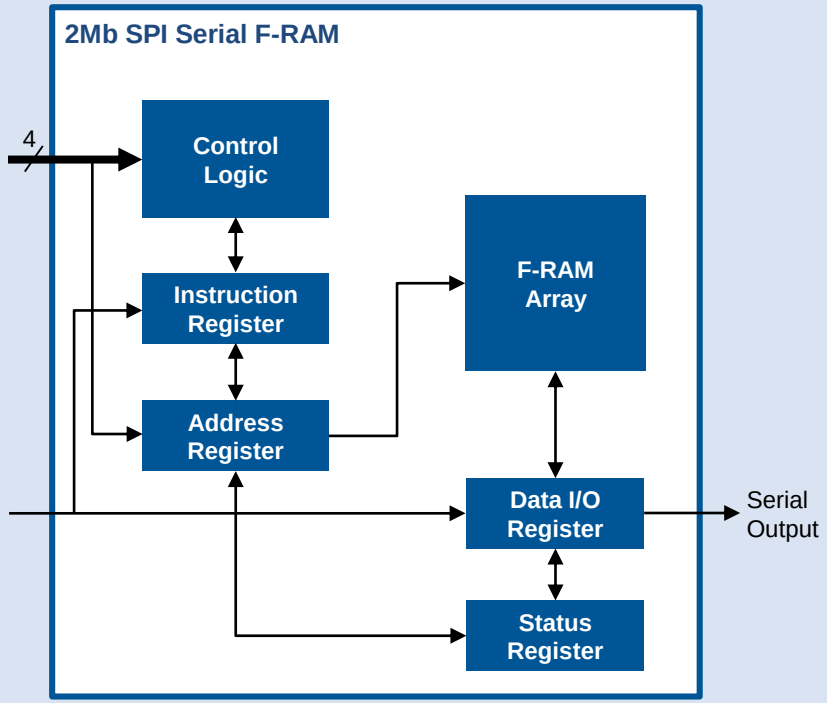
Features

- **Ultra-Low Power Memory**
  - 40-MHz SPI interface
  - 100-trillion read/write cycle endurance
- **Specifications**
  - Operating voltage range: 2.0–3.6 V
  - Low (20-µA) sleep current at +125°C
  - 100 years data retention at +85°C
  - Military temperature grade: -55°C to +125°C
- **Packages: 8-pin TDFN and 8-pin SOIC**

Collateral

Datasheet: CY15B102Q

CY15B102Q: 2Mb SPI F-RAM



Availability

Sampling: Now
Production: Q4'17

64Mb/128Mb/256Mb/512Mb/1Gb Parallel NOR Flash

Applications

Military systems boot memory
Avionics boot memory

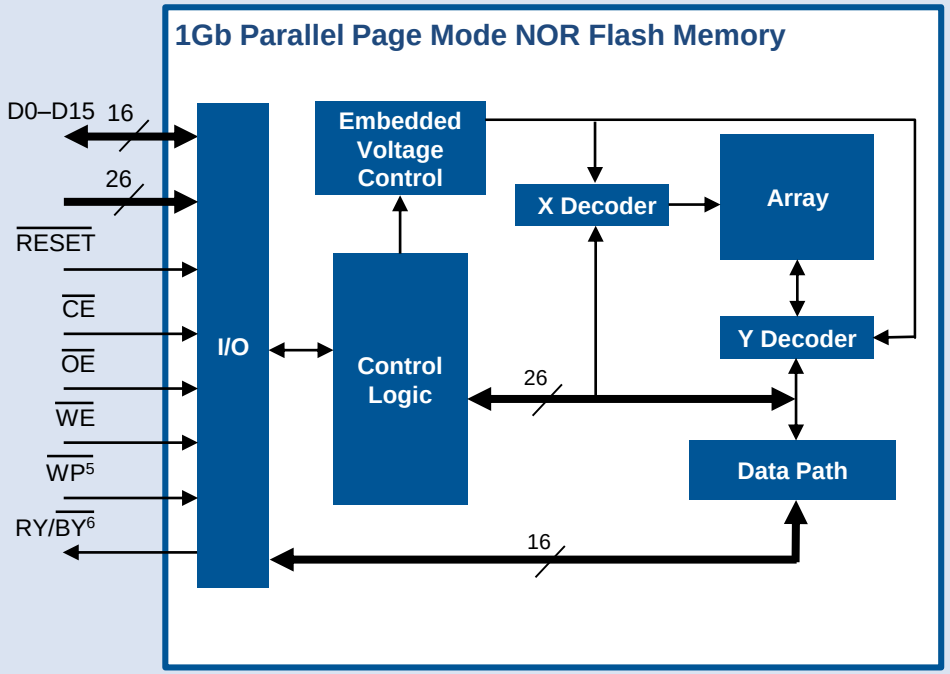
Features

- **High-Reliability Boot Flash Memory**
  - 100 program[1]/sector erase[2] endurance cycles[3] at +125°C
  - >10 years data retention at +125°C
- **Specifications**
  - Operating voltage range: 2.7–3.6 V
  - Initial access time: 120 ns
  - Page access time: 15 ns
  - Program time (512B): 0.4 ms (typical)
  - Sector erase time (128KB): 410 ms (typical)
  - Military temperature grade: -55°C to +125°C
- **Packages: 56-pin TSOP (14 x 20 mm), 64-ball fortified[4] BGA (9 x 9 mm and 13 x 11 mm, with and without leaded balls)**

Collateral

Datasheet: S29GLXXXS (128M/256M/512M/1G)

S29GLXXXS: Parallel NOR Flash



Availability

Samples: Now
Production: Q3'17 (128Mb/256Mb/512Mb)/Q4'17 (64Mb)

[1] The operation required to change a NOR Flash memory cell state from "1" to "0"
[2] The operation in which all the bytes in a sector of NOR Flash memory are erased simultaneously prior to programming
[3] The number of times a NOR Flash memory sector can be programmed or erased before it wears out
[4] Fortified BGA supports a 1-mm ball pitch
[5] Write protect input
[6] Ready/busy output

128Mb/256Mb/512Mb/1Gb SPI NOR Flash

Applications

Military systems boot memory
Avionics boot memory

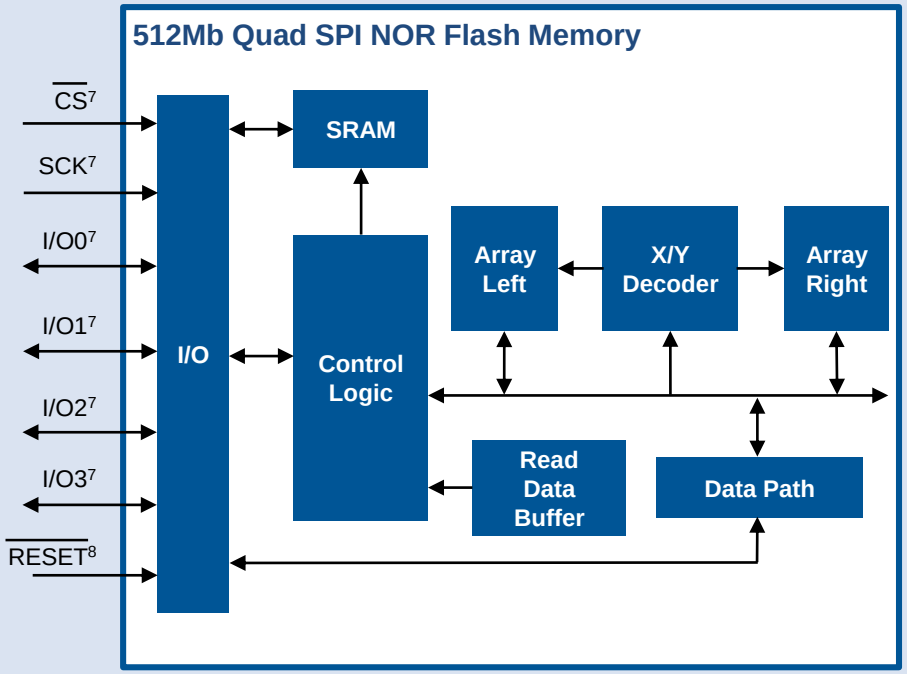
Features

- **High-Reliability Boot Flash Memory**
  - 100 program[1]/sector erase[2] endurance cycles[3] at +125°C
  - >10 years data retention at +125°C
- **Specifications**
  - Operating voltage range: 2.7–3.6 V
  - Single data rate (SDR)[4] clock rate: 104-MHz quad input/output (QIO)[5]
  - Double data rate (DDR)[6] clock rate: 80-MHz QIO
  - Program time (512B): 0.340 ms (typical)
  - Sector erase time (256KB): 520 ms (typical)
  - Military temperature grade: -55°C to +125°C
- **Packages: 24-ball BGA (6 x 8 mm, with and without leaded balls)**

Collateral

Datasheets: S25FL512S (512Mb)
S25FL128/256S (128Mb/256Mb)

S25/70/79FLXXXS: 512Mb QSPI NOR Flash



Availability

Sampling: Now
Production: Q4'17 (128/256/512Mb)/Q1'18 (1Gb)

[1] The operation required to change a NOR Flash memory cell state from "1" to "0"
[2] The operation in which all the bytes in a sector of NOR flash memory are erased simultaneously
[3] The number of times a NOR Flash memory sector can be programmed/erased before it wears out
[4] A mode of data transfer in which data is transferred once per clock cycle
[5] An interface that transfers addresses or data on four I/O's simultaneously
[6] A mode of data transfer in which data is transferred twice per clock cycle
[7] Signals used for standard Quad (x4) SPI interface. Refer to the S25FL512S datasheet for signal definitions in the x1 and x2 mode.
[8] RESET# is an optional signal available on 16-pin-SOIC and BGA packages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