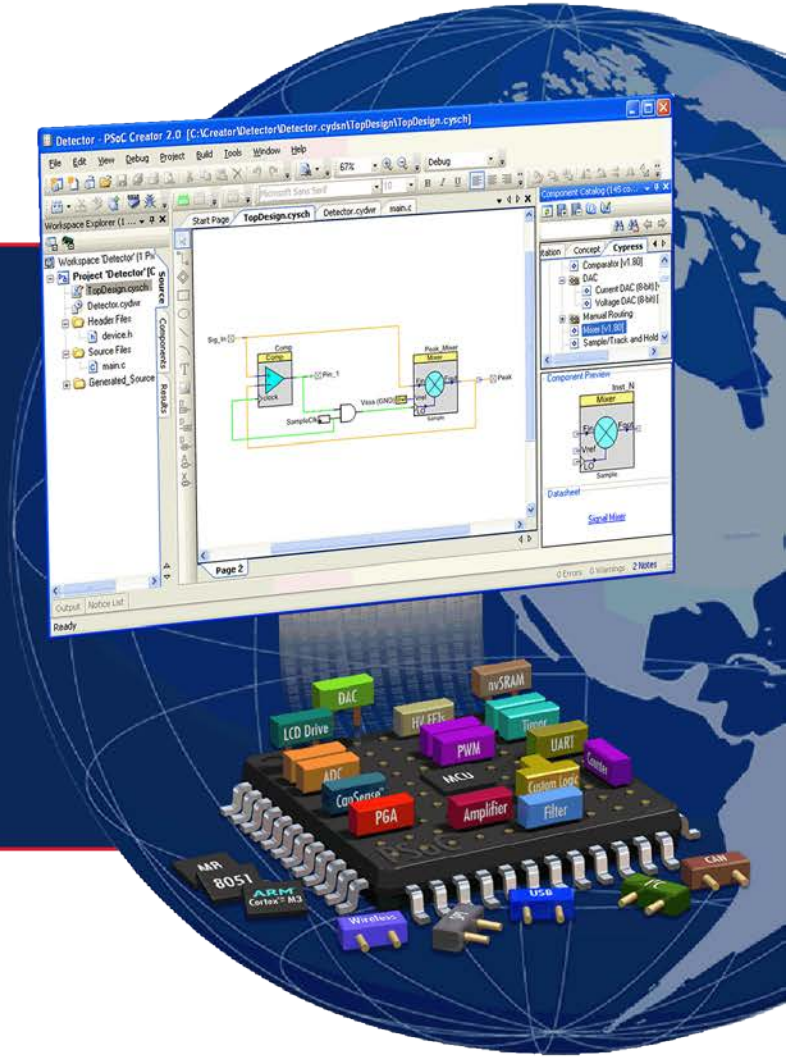
Cypress Roadmap:

Military Memory



Q1 2017

Military Memory Portfolio

Military Temperature | Single Event Latch-up Immune

	Fast Async SRAM	Sync SRAM		Nonvolatile SRAM	F-RAM™	NOR Flash
	ECC[1]	NoBL®[2], ECC	QDR®[3]II+/IV	Serial/Parallel I/O	Serial/Parallel I/O, ECC	Serial/Parallel I/O, ECC
64Mb-1Gb			**CY7C41xKV13** **144Mb**; 667-1066 MHz, 1.3 V, x18/x36, Burst 2, M[4] **CYRS26xKV18** **144Mb**, 1.8 V, 450 MHz, x18/x36, Burst 2/4, M **CYPT154xAV18** **72Mb**, 1.8 V, 250 MHz, x18/x36; Burst 2/4, M			**S29GL-S** Q217 **128Mb-1Gb**; 100 ns/15 ns, 3.0 V, x16, Auto E[5], M **S25FL-S** Q317 **128Mb-512Mb**; 3.0 V, 133-MHz/80 MHz, Auto E, M **S25FS-S** **128Mb-512Mb**; 1.8 V, 133-MHz QSPI, Auto E, M
1Mb-36Mb	**CY7S106x** **16Mb**, 1.8-5.0 V, 10 ns, x8/x16/x32, Auto E, M **CY7S105x** **8Mb**, 1.8-5.0 V, 10 ns, x8/x16/x32, Auto E, M **CY7S104x** **4Mb**, 1.8-5.0 V, 12 ns, x8/x16, Auto E, M	**CY7C144/6xK** **36Mb**, 133-250 MHz, 2.5 V/3.3 V, x18/x36, M **CY7C137/8xK** **18Mb**, 100-250 MHz, 2.5 V/3.3 V, x18/x36, M **CY7C136xK** **9Mb**, 100-250 MHz, 2.5 V/3.3 V, x18/x36, M		**CY14B116x** **16Mb**; 1.8-3.0 V, 25 ns/45 ns, x8/x16/x32, M, RTC[6] **CY14B104x** **4Mb**, 1.8-3.0 V, 25 ns/45 ns, x8/x16, Auto E, M **CY14B101x** **1Mb**, 1.8-3.0 V, 25 ns/45 ns, x8/x16, SPI Auto E, M, RTC	**CY15B102N** **2Mb**, 2.0-3.6 V, 60 ns, x16, Auto E, M **CY15B102Q** **2Mb**, 2.0-3.6 V, 40-MHz SPI, Auto E, M **FM25V10** **1Mb**; 2.0-3.6 V, 40-MHz SPI, Auto E, M	
64Kb-256Kb				**STK14C88-5** **256Kb**; 5.0 V, 35 ns/45 ns, x8; QML-Q[7] **STK12C68-5** **64Kb**; 5.0 V, 35 ns/55 ns, x8; QML-Q		

[1] Error-correcting code
[2] No Bus Latency
[3] Quad Data Rate
[4] Military Temperature: −55°C to +125°C
[5] AEC-Q100 -40°C to +125°C
[6] Real-time clock
[7] Qualified Manufacturers List Level Q, per MIL-PRF-38535

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

256Kb Military nvSRAM

Applications

Military communication
Military real-time controls
Avionics real-time controls
High-reliability data logging

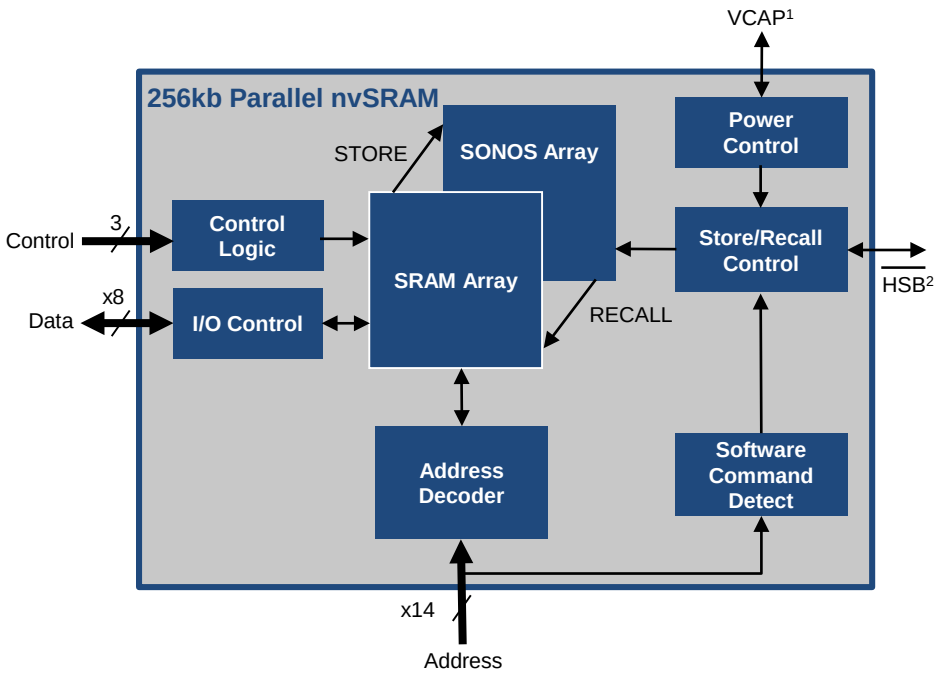
Features

Fast access time (35 ns, 45 ns, or 55 ns)
Available in parallel interface for 64Kb and 256Kb densities
Unlimited read/write endurance
One million store cycles on power fail
100 years data retention at +85°C
Qualified Manufacturers List Level Q (QML-Q certified) per MIL-PRF-38535
Military temperature grade: -55°C to +125°C
Packages: Ceramic 32-pin DIP, ceramic 32-pin LCC, 28-pin SOIC and 32-pin SOIC

Collateral

Datasheets: STK12C68
STK14C88

Block Diagram



Availability

Sampling: Now
Production: Now

[1] External capacitor connection
[2] Hardware STORE busy

72Mb QDR®[1]-II+ SRAM

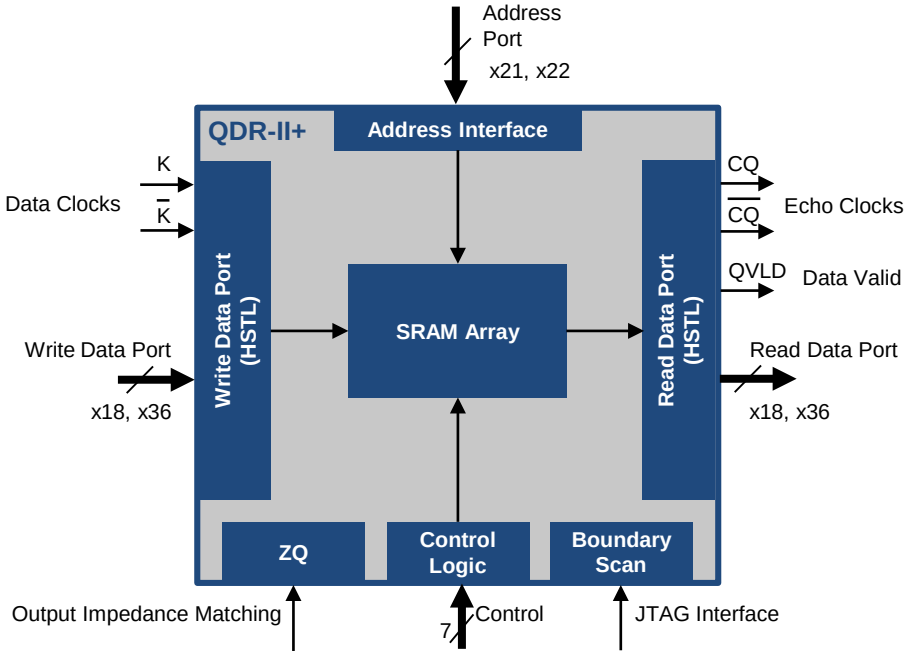
Applications

Military communication
Military real-time control
Avionics real-time control

Features

Maximum frequency of operation/throughput: 250 MHz/36 Gbps
Burst sizes: 2 or 4
Bus-width configurations: x18 or x36
Military temperature grade: -55°C to +125°C
Two independent unidirectional data ports for read and write enable concurrent transactions
Maximum throughput with double data rate (DDR) data ports
Output impedance matching input (ZQ): Matches the device outputs to system data bus impedance
Bit-interleaving to eliminate multi-bit errors
I/O signaling standards: 1.5-1.8 V (HSTL)
Controllers available for Altera/Xilinx/Microsemi FPGAs
Package: 165-pin CCGA[2]

Block Diagram



Collateral

Datasheets: CYPT1542AV18/CYPT1544AV18
CYPT1543AV18/CYPT1545AV18

Availability

Sampling: Now
Production: Now

[1] Quad Data Rate: Four data transfers per clock cycle
[2] Ceramic column grid array package

QDR®[1]-IV SRAM

Applications

High-performance computing
Military and aerospace systems
Test and measurement

Features

Available in two options: QDR-IV HP (RTR 1,334 MT/s) and QDR-IV XP (RTR 2,132 MT/s)
Two independent, bidirectional DDR[2] data ports
Embedded error-correcting code (ECC) to reduce soft error rate to <0.01 failure-in-time (FIT) per megabit
Bus inversion to reduce simultaneous switching I/O noise
On-die termination (ODT) to reduce board complexity
De-skew training to improve signal-capture timing
I/O levels: 1.2-1.25 V (HSTL/SSTL), 1.1-1.2 V (POD[3])
Military temperature grade: -55°C to +125°C
Package: 361-ball FCBGA[4]
Bus widths: x18 or x36

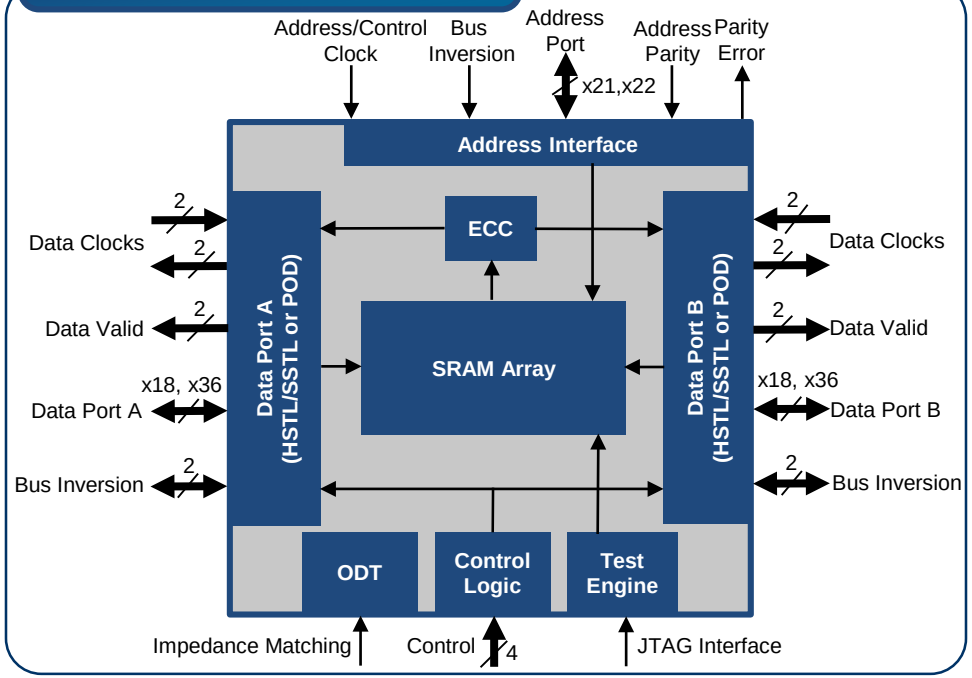
Collateral

Datasheet: CY7C4021KV13/CY7C4041KV13

Family Table

Option	Density	MPN	Max. Frequency	RTR
QDR-IV HP	72Mb 144Mb	CY7C40x1KV13 CY7C41x1KV13	667 MHz	1,334 MT/s
QDR-IV XP	72Mb 144Mb	CY7C40x2KV13 CY7C41x2KV13	1,066 MHz	2,132 MT/s

Block Diagram



Availability

Sampling: Now
Production: Contact Sales

[1] Quad Data Rate: Four data transfers per clock cycle
[2] Double Data Rate: Two data transfers per clock cycle
[3] Pseudo Open Drain: Signaling interface that uses strong pull-down and weak pull-up drive strength
[4] Flip-chip ball grid array

Sync SRAM With On-Chip ECC

Applications

Avionics engine controls
Radar and signal processing
Test equipment
Military and aerospace systems

Features

Available in flow-through and pipeline modes[1]
Single-cycle (SCD)[2] and double-cycle (DCD)[2] deselect options
Bus-width configurations: x18 or x36
Two voltage options: 2.5 V and 3.3 V
Military temperature grade: -55°C to +125°C
Error-correcting code (ECC) to detect and correct single-bit errors
Packages: 165-ball BGA and 100-pin TQFP
Industry-standard, RoHS[3]-compliant packages

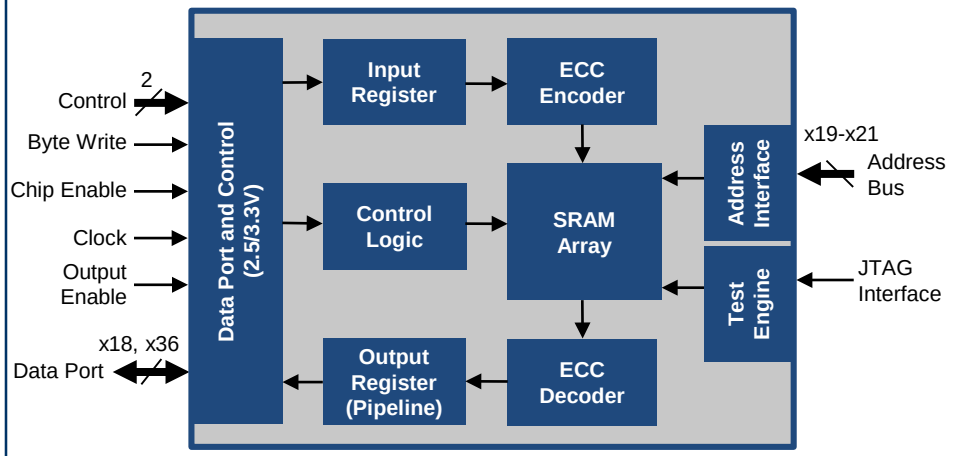
Collateral

Datasheets: CY7C135XKV33/CY7C136XKV33
CY7C137XKV33/CY7C138XKV33
CY7C144XKV33/CY7C146XKV33

Family Table

Option	Density	MPN	RTR	FIT/Mb[4]
Standard Sync with On-Chip ECC Pipeline	9Mb 18Mb 36Mb	CY7C1360/2K CY7C1370/2K CY7C1440/2K	250 MT/s	<0.01
Standard Sync with On-Chip ECC Flow-Through	9Mb 18Mb 36Mb	CY7C1361/3K CY7C1371/3K CY7C1441/3K	133 MT/s	<0.01

Block Diagram



Availability

Sampling: Now
Production: Now

[1] Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
[2] Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
[3] Restriction of Hazardous Substances: A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components
[4] Failures-in-Time (FIT) per Megabit of Data (FIT/Mb): The projected failure rate of a device where one FIT/Mb equals one failure per billion device hours per megabit of data

Fast SRAM With PowerSnooze™[1]

Applications

Avionics engine controls
Military helicopter controls
Military/commercial aircraft flight controls

Features

Access time: 10 ns or 12 ns (see Family Table)
PowerSnooze™: Additional power-savings (deep-sleep) mode
Deep-sleep current: 22 µA for 16Mb (see Family Table)
Multiple bus-width configurations: x8, x16 and x32
Wide I/O operating voltage range: 1.8-5.0 V
Military temperature grade: -55°C to +125°C
Industry-standard, RoHS[2]-compliant and leaded BGA packages
Error-correcting code (ECC) to detect/correct single-bit errors
Bit-interleaving to avoid multi-bit errors

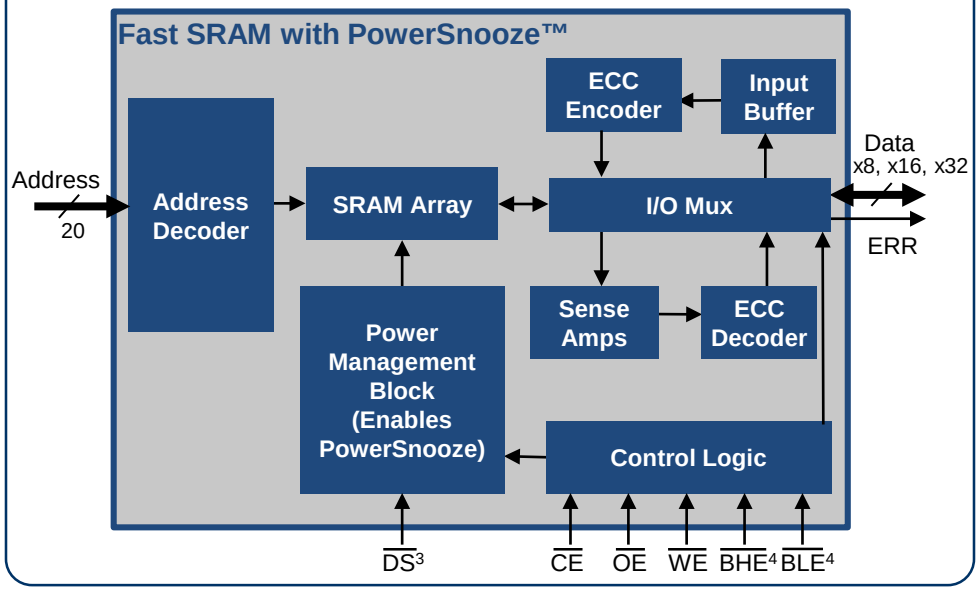
Collateral

Datasheets: CY7S1049G/CY7C1049G
CY7S1059H/CY7C1059H
CY7S1069G/CY7C1069G

Family Table

Density	MPN	Access Time (85°C/125°C)	Deep Sleep Current (Max at 85°C)
4Mb	CY7S104x	10/12 ns	15 µA
8Mb	CY7S105x	10/12 ns	22 µA
16Mb	CY7S106x	10/12 ns	22 µA

Block Diagram



Availability

Sampling: Now
Production: Contact Sales

[1] A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode. For example, the 12-ns 16Mb offering has a deep-sleep current of ≤1.37 µA/Mb and a standby current of ≤1.87 mA/Mb
[2] Restriction of Hazardous Substances: A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components
[3] Deep sleep power mode
[4] Byte high enable (BHE)/Byte low enable (BLE)

16Mb Parallel nvSRAM

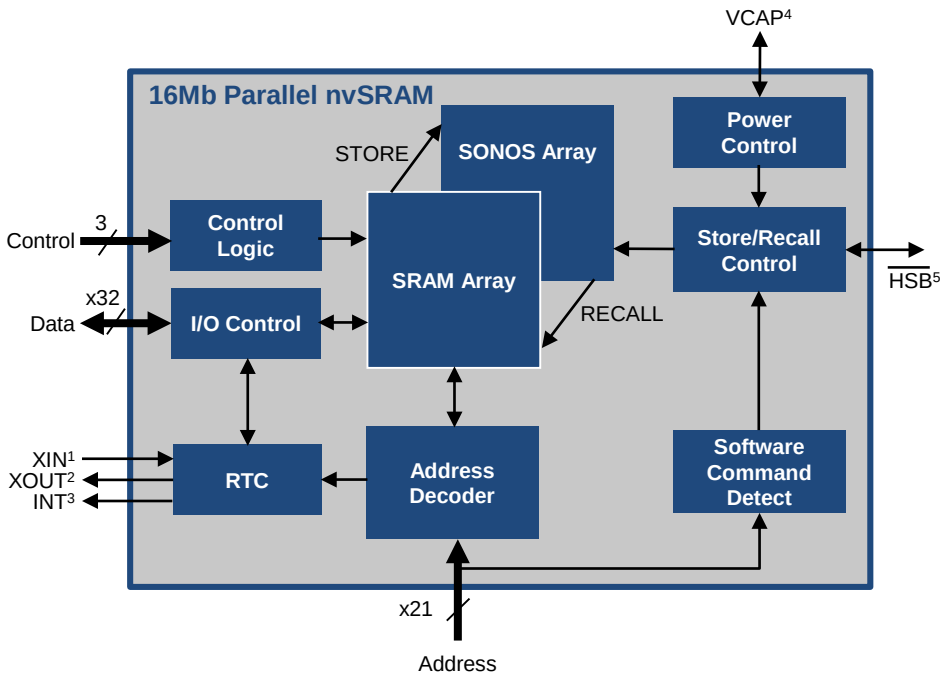
Applications

Industrial automation
Programmable logic controllers
Gaming machines
Industrial data logging
Networking and storage
Telecom equipment

Features

Fast access time (25 ns)
Available in parallel and Open NAND Flash Interface (ONFI) version 1.0 interfaces
Unlimited read/write endurance
One million store cycles on power fail
20 years data retention at +85°C
Optional real-time clock (RTC) functionality
Military temperature grade: -55°C to +125°C
Packages: 44-pin TSOP-II, 48-pin TSOP-I, 54- pin TSOP-II, 165-ball FBGA

Block Diagram



Collateral

Datasheet: CY14X116L/CY14X116N/CY14X116S

Availability

Sampling: Now
Production: Contact Sales

[1] Crystal connection input
[2] Crystal connection output
[3] Interrupt output/calibration/square wave
[4] External capacitor connection
[5] Hardware STORE busy

2Mb SPI Serial F-RAM

Applications

Multifunction printers
Industrial controls and automation
Medical wearables
Test and measurement equipment
Smart meters
Aerospace and defense applications
Missiles and launchers

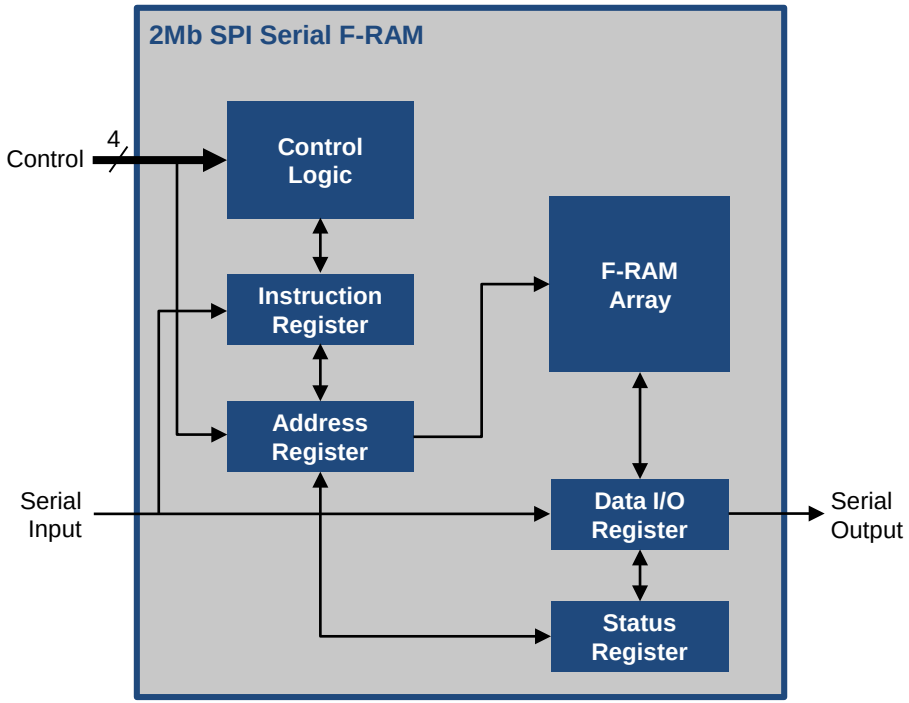
Features

40-MHz SPI interface
100-trillion read/write cycle endurance
Operating voltage range: 2.0-3.6 V
Low (20-µA) sleep current at +125°C
100 years data retention at +85°C
Military temperature grade: -55°C to +125°C
Packages: 8-pin TDFN and 8-pin SOIC

Collateral

Datasheet: CY15B102Q

Block Diagram



Availability

Sampling: Now
Production: Contact Sales

128Mb/256Mb/512Mb/1Gb Parallel NOR Flash Memory

Applications

Military systems boot memory
Avionics boot memory

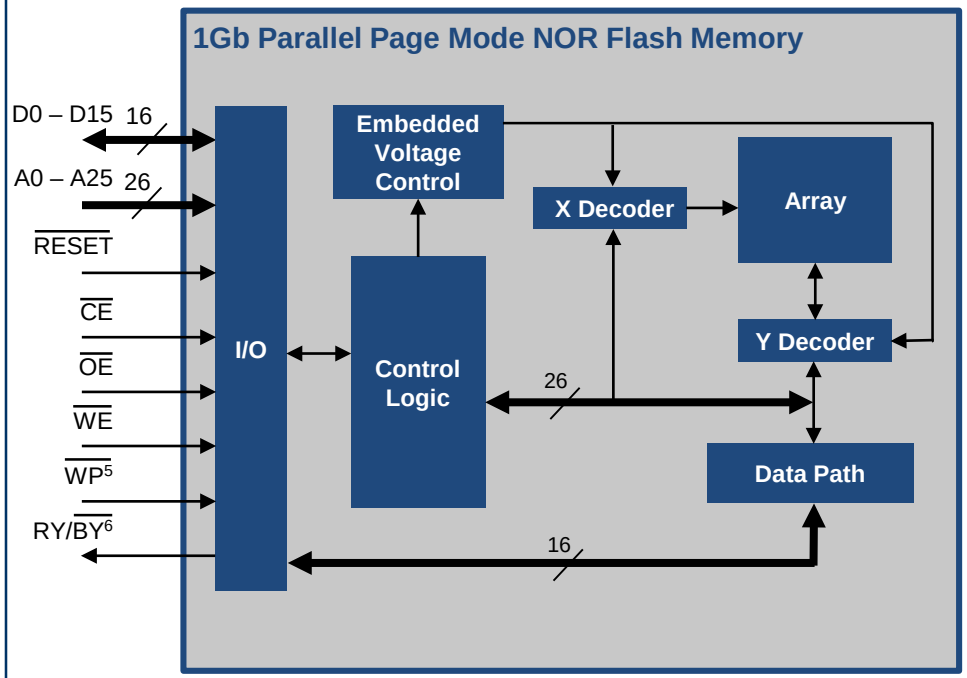
Features

Operating voltage range: 2.7 V to 3.6 V
100 program[1]/sector erase[2] endurance cycles[3] at +125°C
>10 years data retention at +125°C
Initial access time: 100 ns
Page access time: 15 ns
Program time (512B): 0.34 ms (typical)
Sector erase time (128KB): 275 ms (typical)
Military temperature grade: -55°C to +125°C
Packages: 56-pin TSOP (14 x 20 mm), 64-ball fortified[4] BGA (9 x 9 and 13 x 11 mm)

Collateral

Datasheet: S29GLXXXS (128M/256M/512M/1G)

Block Diagram



Availability

Sampling: Now
Production: Contact Sales

[1] The operation required to change a NOR Flash memory cell state from “1” to “0”
[2] The operation in which all the bytes in a sector of NOR Flash memory are erased simultaneously prior to programming
[3] The number of times a NOR Flash memory sector can be programmed or erased before it wears out
[4] Fortified BGA supports a 1-mm ball pitch
[5] Write protect input
[6] Ready/busy output

128Mb/256Mb/512Mb SPI NOR Flash Memory

Applications

Military systems boot memory
Avionics boot memory

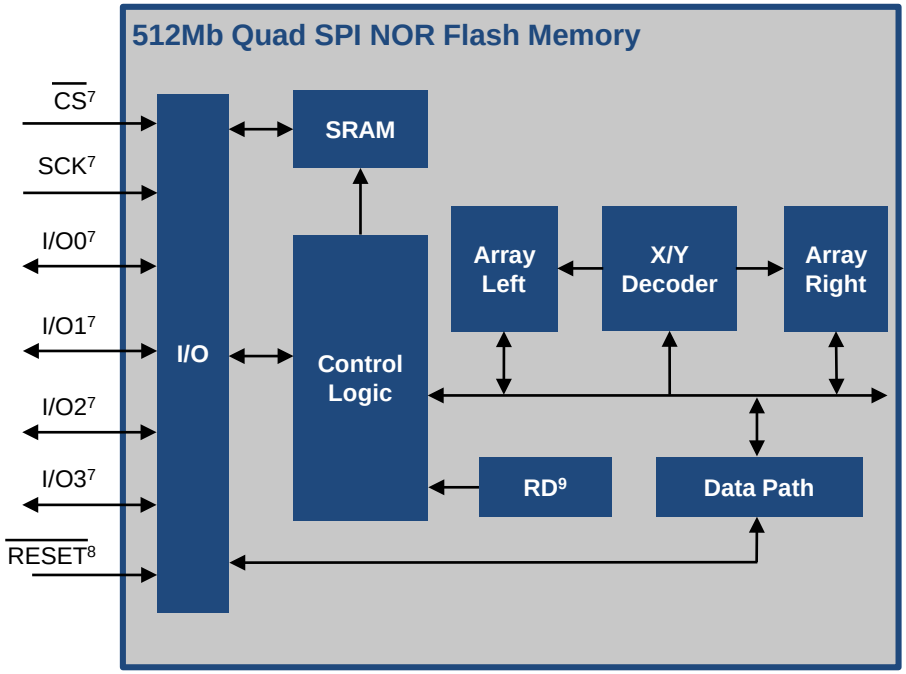
Features

Operating voltage range: 2.7-3.6 V
100 program[1]/sector erase[2] endurance cycles[3] at +125°C
>10 years data retention at +125°C
SDR[4] clock rate: 104-MHz QIO[5]
DDR[6] clock rate: 80-MHz QIO
Program time (512B): 0.340 ms (typical)
Sector erase time (256KB): 520 ms (typical)
Military temperature grade: -55°C to +125°C
Packages: 16-pin SOIC 300 mil and 24-ball BGA (6x8 mm)

Collateral

Datasheet: S25FL512S (512Mb)
S25FL128/256S (128Mb/256Mb)

Block Diagram



Availability

Sampling: Now
Production: Contact Sales

[1] The operation required to change a NOR Flash memory cell state from "1" to "0"
[2] The operation in which all the bytes in a sector of NOR flash memory are erased simultaneously prior to programming
[3] The number of times a NOR Flash memory sector can be programmed/erased before it wears out
[4] Single Data Rate: A mode of data transfer in which data is transferred once per clock cycle
[5] Quad Input/Output (QIO): An interface that transfers addresses or data on four I/O's simultaneously
[6] Double Data Rate: A mode of data transfer in which data is transferred twice per clock cycle
[7] Signals used for standard Quad (x4) SPI interface. Refer to the S25FL512S datasheet for signal definitions in the x1 and x2 mode.
[8] RESET# is an optional signal available on 16-pin-SOIC and BGA packages.
[9] Read data buffer