PRELIMINARY

CYW43364

Single-Chip IEEE 802.11 b/g/n MAC/ Baseband/Radio

The Cypress CYW43364 is a highly integrated single-chip solution and offers the lowest RBOM in the industry for Internet of Things (IoT) and a wide range of other portable devices. The chip includes a 2.4 GHz WLAN IEEE 802.11 b/g/n MAC/baseband/radio. In addition, it integrates a power amplifier (PA) that meets the output power requirements of most handheld systems, a low-noise amplifier (LNA) for best-in-class receiver sensitivity, and an internal transmit/receive (iTR) RF switch, further reducing the overall solution cost and printed circuit board area.

The WLAN host interface supports SDIO v2.0 mode, providing a raw data transfer rate up to 200 Mbps when operating in 4-bit mode at a 50 MHz bus frequency.

Using advanced design techniques and process technology to reduce active and idle power, the CYW43364 is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It includes a power management unit that simplifies the system power topology while maximizing battery life.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM43364	CYW43364
BCM43364KUBG	CYW43364KUBG

Features

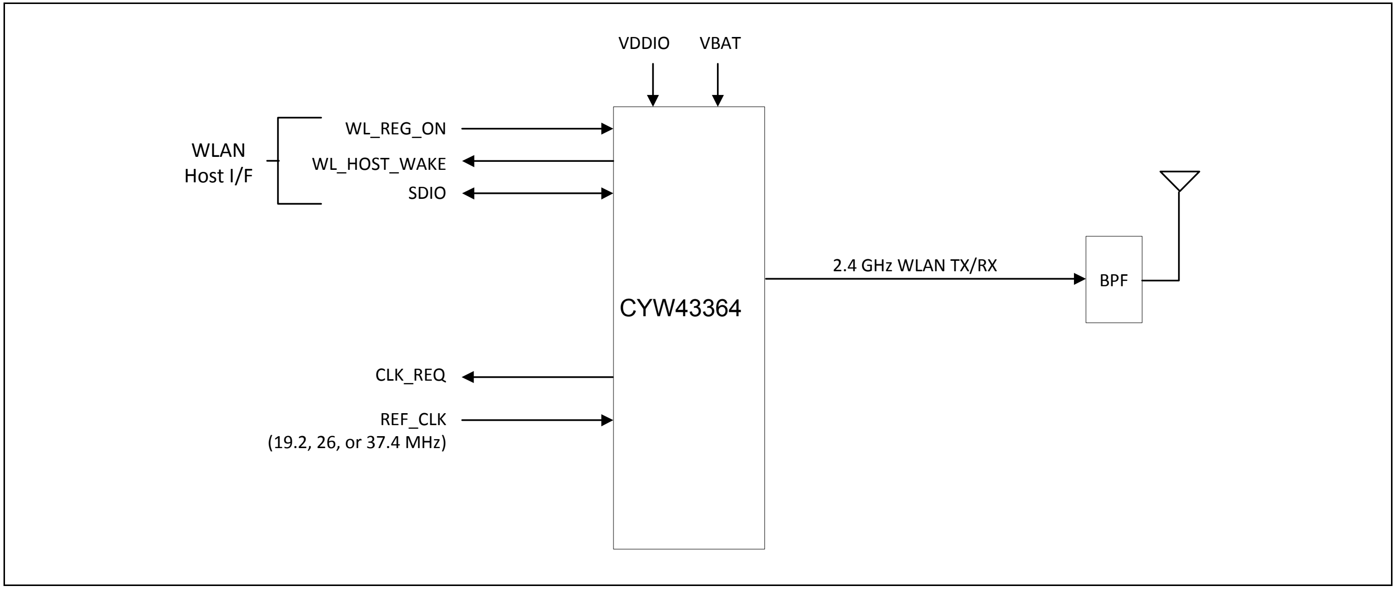
IEEE 802.11x Key Features

- Single-band 2.4 GHz IEEE 802.11b/g/n.
- Support for 2.4 GHz Cypress TurboQAM® data rates (256-QAM) and 20 MHz channel bandwidth.
- Integrated iTR switch supports a single 2.4 GHz antenna.
- Supports explicit IEEE 802.11n transmit beamforming.
- Tx and Rx low-density parity check (LDPC) support for improved range and power efficiency.
- Supports standard SDIO v2.0 host interface.
- Supports space-time block coding (STBC) in the receiver.
- Integrated ARM Cortex-M3 processor and on-chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field-upgrade with future features. On-chip memory includes 512 KB SRAM and 640 KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN.

General Features

- Support diversity antenna.
- Supports a battery voltage range from 3.0V to 4.8V with an internal switching regulator.
- Programmable dynamic power management.
- 4 Kbit one-time programmable (OTP) memory for storing board parameters.
- Can be routed on low-cost 1-x-1 PCB stack-ups.
- 74-ball WLBGA package (4.87 mm × 2.87 mm, 0.4 mm pitch).
- Security:
  - WPA and WPA2 (Personal) support for powerful encryption and authentication.
  - AES in WLAN hardware for faster data encryption and IEEE 802.11i compatibility.
  - Reference WLAN subsystem provides Cisco Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0).
  - Reference WLAN subsystem provides Wi-Fi protected setup (WPS).
- Worldwide regulatory support: Global products supported with worldwide homologated design.

Figure 1. CYW43364 System Block Diagram



Contents

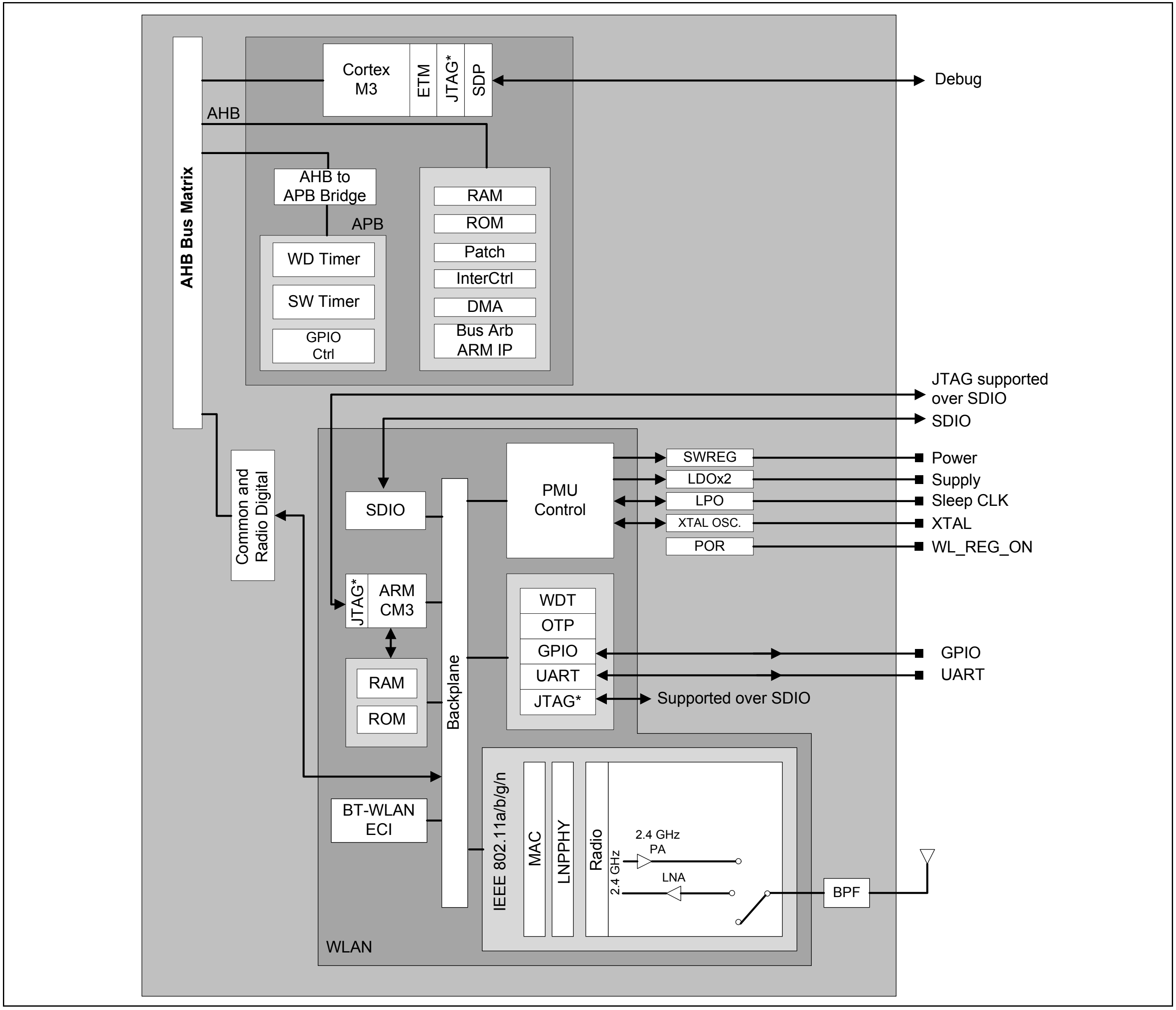
1. Overview

1.1 Overview

The Cypress CYW43364 provides the highest level of integration for IoT and wireless automation system, with integrated IEEE 802.11 b/g/n. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. The CYW43364 is designed to address the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 on page 4 shows the interconnection of all the major physical blocks in the CYW43364 and their associated external interfaces, which are described in greater detail in subsequent sections.

Figure 2. CYW43364 Block Diagram



1.2 Features

The CYW43364 supports the following WLAN features:

- IEEE 802.11b/g/n single-band radio with an internal power amplifier, LNA, and T/R switch
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- WLAN host interface options:
  - SDIO v2.0, including default and high-speed timing.

1.3 Standards Compliance

The CYW43364 supports the following standards:

- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The CYW43364 will support the following future drafts/standards:

- IEEE 802.11r — Fast Roaming (between APs)
- IEEE 802.11k — Resource Management
- IEEE 802.11w — Secure Management Frames
- IEEE 802.11 Extensions:
- IEEE 802.11e QoS Enhancements (as per the WMM specification is already supported)
- IEEE 802.11i MAC Enhancements
- IEEE 802.11r Fast Roaming Support
- IEEE 802.11k Radio Resource Measurement

The CYW43364 supports the following security features and proprietary protocols:

- Security:
  - WEP
  - WPA Personal
  - WPA2 Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - WAPI
  - AES (Hardware Accelerator)
  - TKIP (host-computed)
  - CKIP (SW Support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
- IEEE 802.15.2 Coexistence Compliance — on silicon solution compliant with IEEE 3-wire requirements.

2. Power Supplies and Power Management

2.1 Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW43364. All regulators are programmable via the PMU to simplify the power supply.

A single VBAT (3.0V to 4.8V DC maximum) and VDDIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the CYW43364.

The WL_REG_ON control signal is used to power up the regulators and take the respective circuit blocks out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when WL_REG_ON is deasserted. The CLDO and LNLDO can be turned on and off based on the dynamic demands of the digital baseband.

The CYW43364 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, LPLDO1 provides the CYW43364 with all required voltage, further reducing leakage currents.

Notes:

VBAT should be connected to the LDO_VDDBAT5V and SR_VDDBAT5V pins of the device.

VDDIO should be connected to the SYS_VDDIO and WCC_VDDIO pins of the device.

2.2 CYW43364 PMU Features

The PMU supports the following:

- VBAT to 1.35Vout (170 mA nominal, 370 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (250 mA nominal, 450 mA maximum 800 mA peak maximum) LDO3P3
- 1.35V to 1.2Vout (100 mA nominal, 150 mA maximum) LNLDO
- 1.35V to 1.2Vout (80 mA nominal, 200 mA maximum) CLDO with bypass mode for deep sleep
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wake-up timing from extremely low power-consumption mode.

Figure 3 on page 7 and Figure 4 on page 8 show the typical power topology of the CYW43364.

Figure 3. Typical Power Topology (1 of 2)

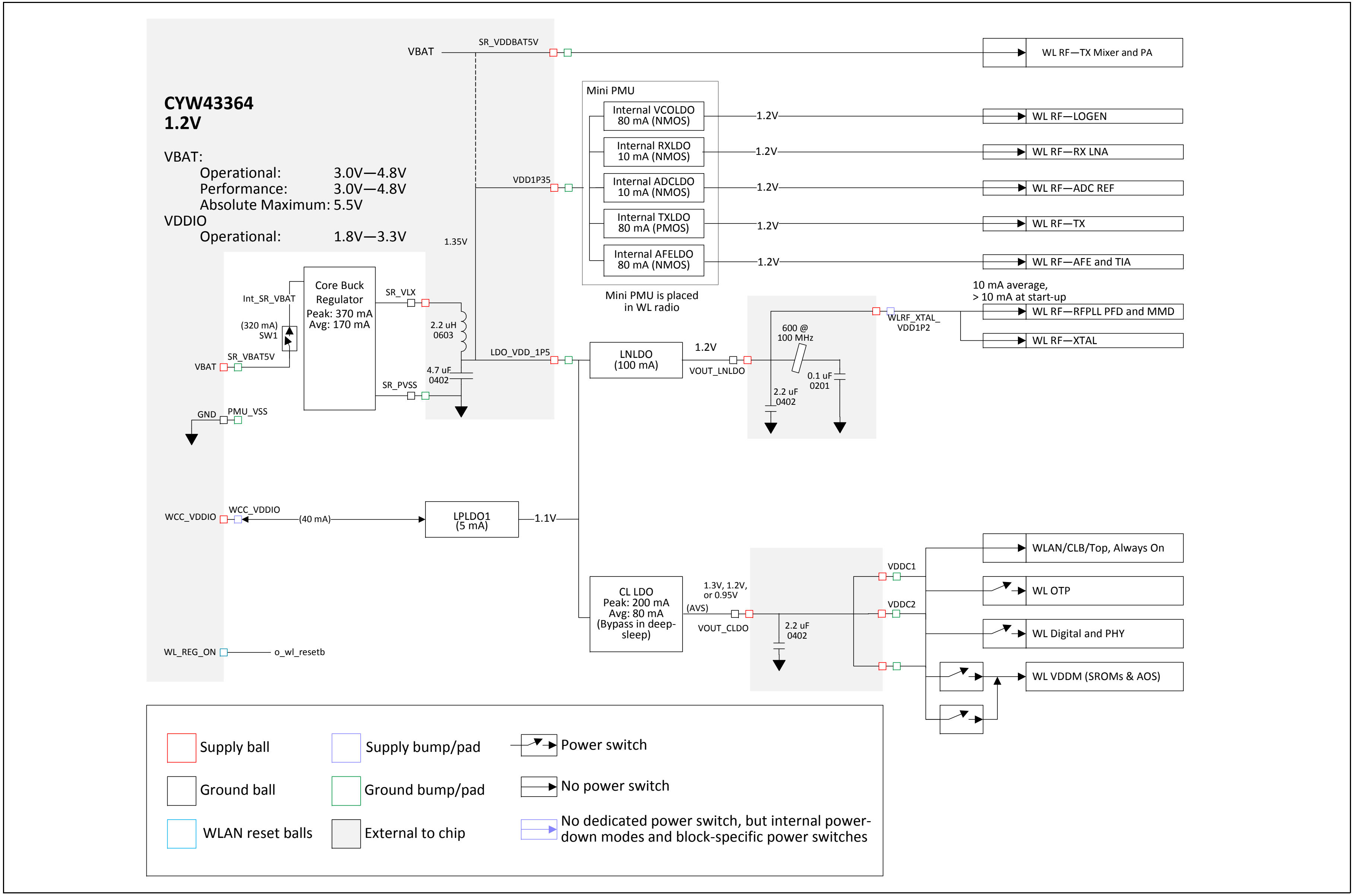
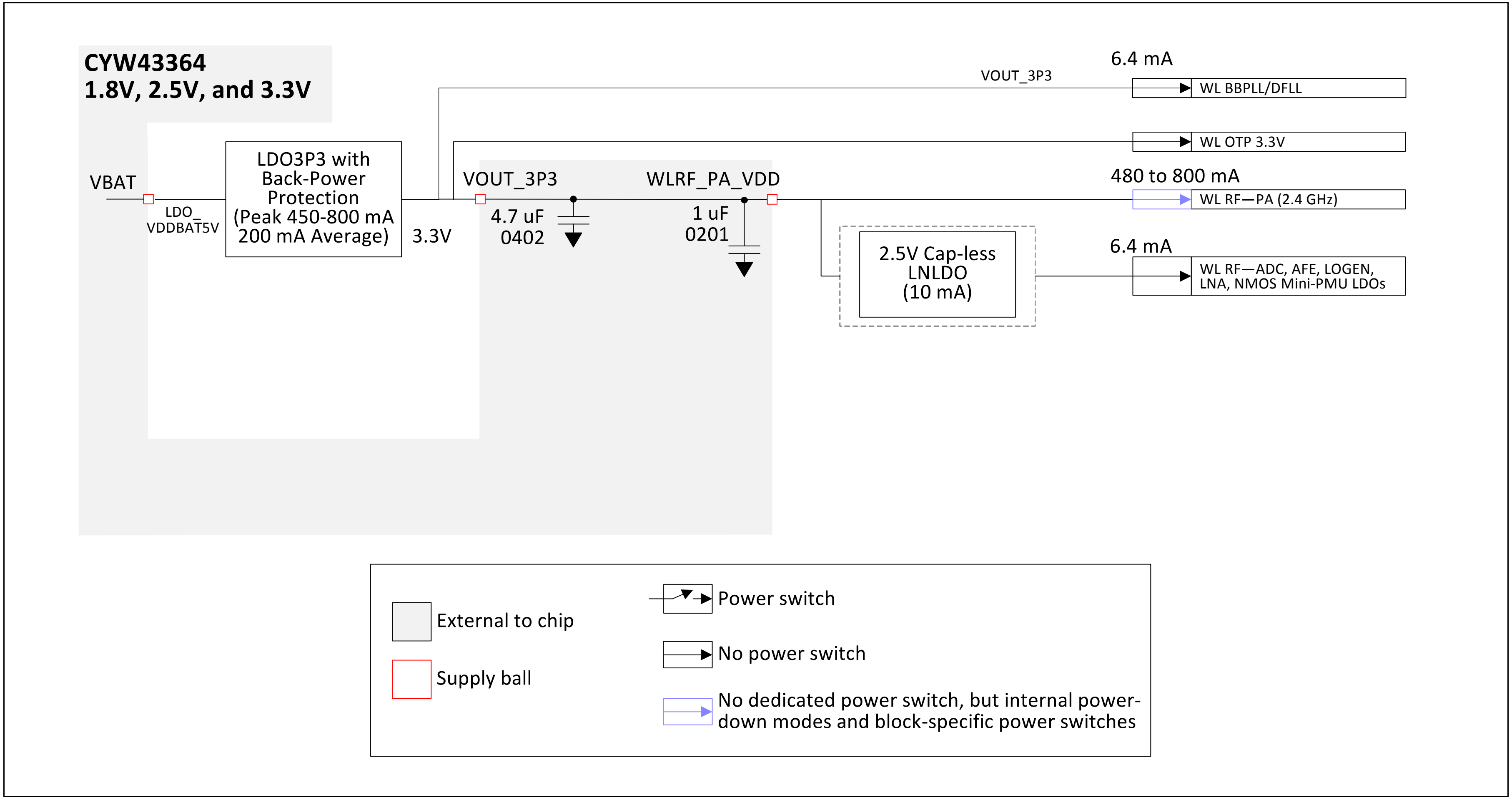


Figure 4. Typical Power Topology (2 of 2)



2.3 WLAN Power Management

The CYW43364 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW43364 integrated RAM is a high volatile memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW43364 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW43364 into various power management states appropriate to the operating environment and the activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at the 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW43364 WLAN power states are described as follows:

- Active mode: All WLAN blocks in the CYW43364 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode: The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW43364 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode: Most of the chip, including analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved to retention memory in the always-on domain before the digital core is powered off. To avoid lengthy hardware reinitialization, the logic states in the digital core are restored to their pre-deep-sleep settings when a wake-up event is triggered by an external interrupt, a host resume through the SDIO bus, or by the PMU timers.
- Power-down mode: The CYW43364 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is used to minimize system power consumption. It enables and disables various system resources based on a computation of required resources and a table that describes the relationship between resources and the time required to enable and disable them.

Resource requests can derive from several sources: clock requests from cores, the minimum resources defined in the *ResourceMin* register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of the following four states:

- enabled
- disabled
- transition_on
- transition_off

The timer value is 0 when the resource is enabled or disabled and nonzero during state transition. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can transition immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can transition immediately from enabled to disabled. The terms *enable sequence* and *disable sequence* refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are nonzero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW43364 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the CYW43364 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW43364 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the CYW43364, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW43364 to be fully integrated in an embedded device and to take full advantage of the lowest power-savings modes.

When the CYW43364 is powered on from this state, it is the same as a normal power-up, and the device does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

The CYW43364 has two signals (see Table 2) that enable or disable the WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 14.: "Power-Up Sequence and Timing," on page 50.

Table 2. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU to power-up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

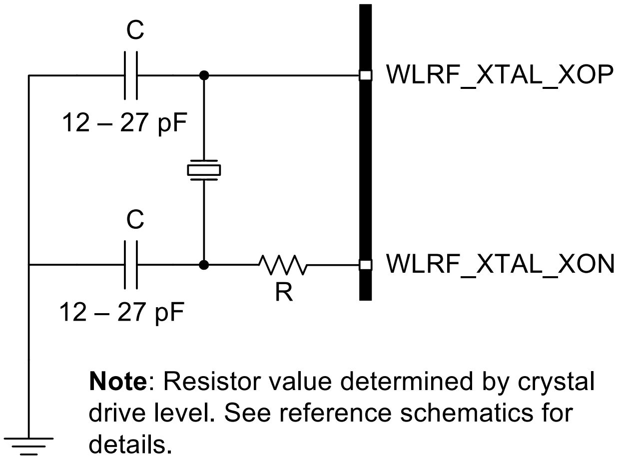
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW43364 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 5. Consult the reference schematics for the latest configuration.

Figure 5. Recommended Oscillator Configuration



Note: Resistor value determined by crystal drive level. See reference schematics for details.

The CYW43364 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing so that it can operate using numerous frequency references. The frequency reference can be an external source such as a TCXO or a crystal interfaced directly to the CYW43364.

The default frequency reference setting is a 37.4 MHz crystal or TCXO. The signal requirements and characteristics for the crystal interface are shown in Table 3 on page 12.

Note: Although the fractional-N synthesizer can support many reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

3.2 TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the phase noise requirements listed in Table 3 on page 12.

If the TCXO is dedicated to driving the CYW43364, it should be connected to the WLRF_XTAL_XOP pin through an external capacitor with value ranges from 200 pF to 1000 pF as shown in Figure 6.

Figure 6. Recommended Circuit to Use with an External Dedicated TCXO

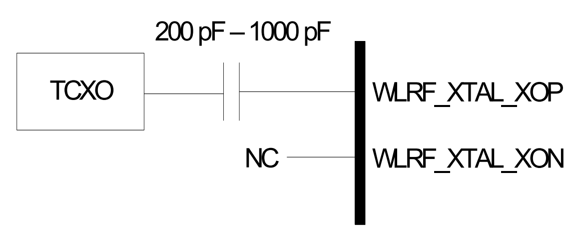


Table 3. Crystal Oscillator and External Clock Requirements and Performance

Parameter	Conditions/Notes	Crystal			External Frequency Reference			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency	–	–	37.4[a]	–	–	–	–	MHz
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Input Impedance (WLRF_XTAL_XOP)	Resistive	–	–	–	10k	100k	–	Ω
	Capacitive	–	–	–	–	–	7	pF
WLRF_XTAL_XOP input voltage	AC-coupled analog signal	–	–	–	400[b]	–	1260	mV_{p-p}
WLRF_XTAL_XOP input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WLRF_XTAL_XOP input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
Frequency tolerance Initial + over temperature	–	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[c, d, e] (IEEE 802.11 b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase Noise[c, d, e] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
Phase Noise[c, d, e] (256-QAM)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–140	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–147	dBc/Hz

[a] The frequency step size is approximately 80 Hz. The CYW43364 does not auto-detect the reference clock frequency; the frequency is specified in the software and/or NVRAM file.

[b] To use 256-QAM, a 800 mV minimum voltage is required.

[c] For a clock reference other than 37.4 MHz, 20 × log10(f/37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.

[d] Phase noise is assumed flat above 100 kHz.

[e] The CYW43364 supports a 26 MHz reference clock sharing option. See the phase noise requirement in the table.

3.3 External 32.768 kHz Low-Power Oscillator

The CYW43364 uses a secondary low-frequency sleep clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 4 on page 13.

Note: The CYW43364 will auto-detect the LPO clock. If it senses a clock on the EXT_SLEEP_CLK pin, it will use that clock. If it doesn't sense a clock, it will use its own internal LPO.

- To use the internal LPO: Tie EXT_SLEEP_CLK to ground. Do not leave this pin floating.
- To use an external LPO: Connect the external 32.768 kHz clock to EXT_SLEEP_CLK.

Table 4. External 32.768 kHz Sleep-Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square wave or sine wave	–
Input impedance[a]	>100	kΩ
	<5	pF
Clock jitter	<10,000	ppm

[a] When power is applied or switched off.

4. WLAN System Interfaces

4.1 SDIO v2.0

The CYW43364 WLAN section supports SDIO version 2.0. for both 1-bit (25 Mbps) and 4-bit modes (100 Mbps), as well as high speed 4-bit mode (50 MHz clocks—200 Mbps). It has the ability to map the interrupt signal on a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided.

SDIO mode is enabled using the strapping option pins. See Table 9 on page 30 for details.

Three functions are supported:

- Function 0 standard SDIO function. The maximum block size is 32 bytes.
- Function 1 backplane function to access the internal System-on-a-Chip (SoC) address space. The maximum block size is 64 bytes.
- Function 2 WLAN function for efficient WLAN packet transfer through DMA. The maximum block size is 512 bytes.

4.1.1 SDIO Pin Descriptions

Table 5. SDIO Pin Descriptions

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2	NC	Not used
DATA3	Data line 3	NC	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

Figure 7. Signal Connections to SDIO Host (SD 4-Bit Mode)

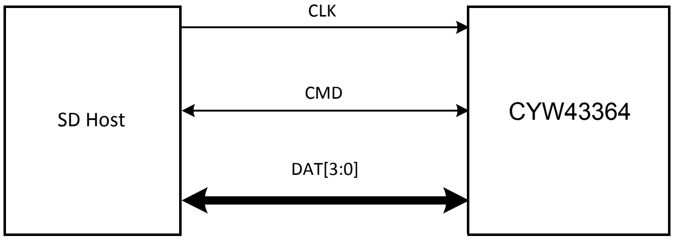
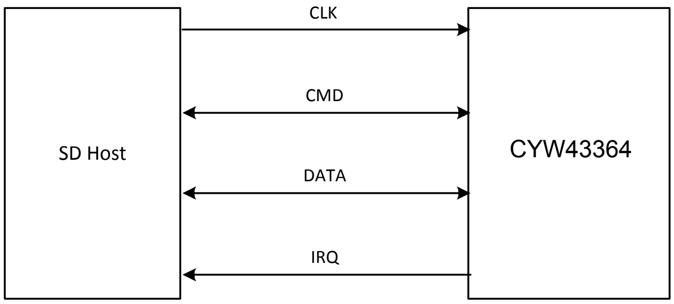


Figure 8. Signal Connections to SDIO Host (SD 1-Bit Mode)



5. Wireless LAN MAC and PHY

5.1 MAC Features

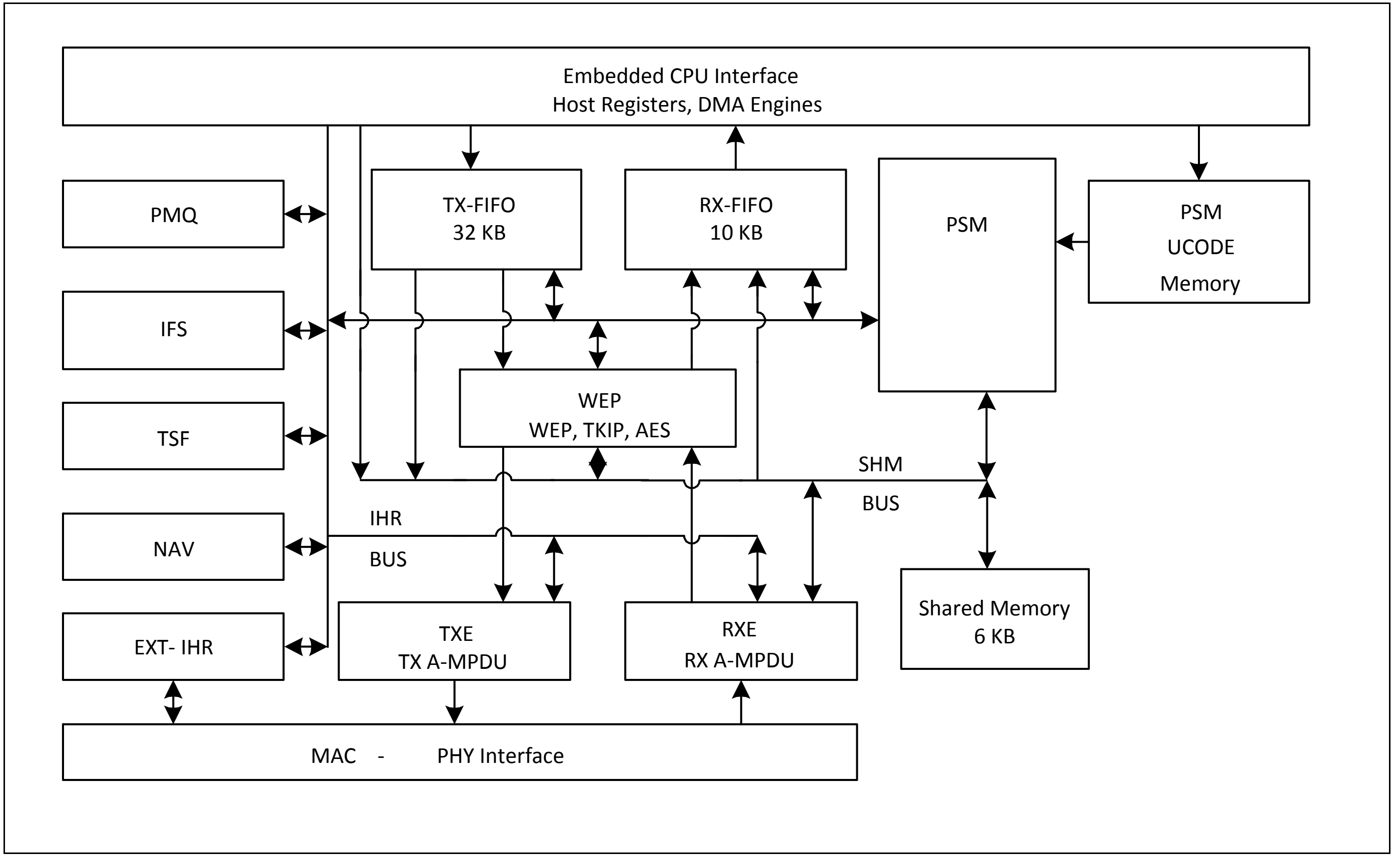
The CYW43364 WLAN MAC supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

- Transmission and reception of aggregated MPDUs (A-MPDU).
- Support for power management schemes, including WMM power-save, power-save multipoll (PSMP) and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies.
- Interframe space timing support, including RIFS.
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware off-load for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management.
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support.

5.1.1 MAC Description

The CYW43364 WLAN MAC is designed to support high throughput operation with low-power consumption. In addition, several power-saving modes that have been implemented allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 9 on page 15.

Figure 9. WLAN MAC Architecture



The following sections provide an overview of the important modules in the MAC.

PSM

The programmable state machine (PSM) is a microcoded engine that provides most of the low-level control to the hardware to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow-control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are collocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, an instruction literal, or a program stack. For ALU operations, the operands are obtained from shared memory, scratch-pad memory, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad memory, or IHRs.

There are two basic branch instructions: conditional branches and ALU-based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs) or on the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, as well as the MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, and WPA2 AES-CCMP.

Based on the frame type and association information, the PSM determines the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the transmit engine (TXE) to encrypt and compute the MIC on transmit frames and the receive engine (RXE) to decrypt and verify the MIC on receive frames. WAPI is also supported.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RX FIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RX FIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple back-off engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The back-off engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the back-off counters. When the back-off counters reach 0, the TXE gets notified so that it may commence frame transmission.

In the event of multiple back-off counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power-saving mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires, the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration, ensuring that the TSF is synchronized to the network.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is a programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

5.2 PHY Description

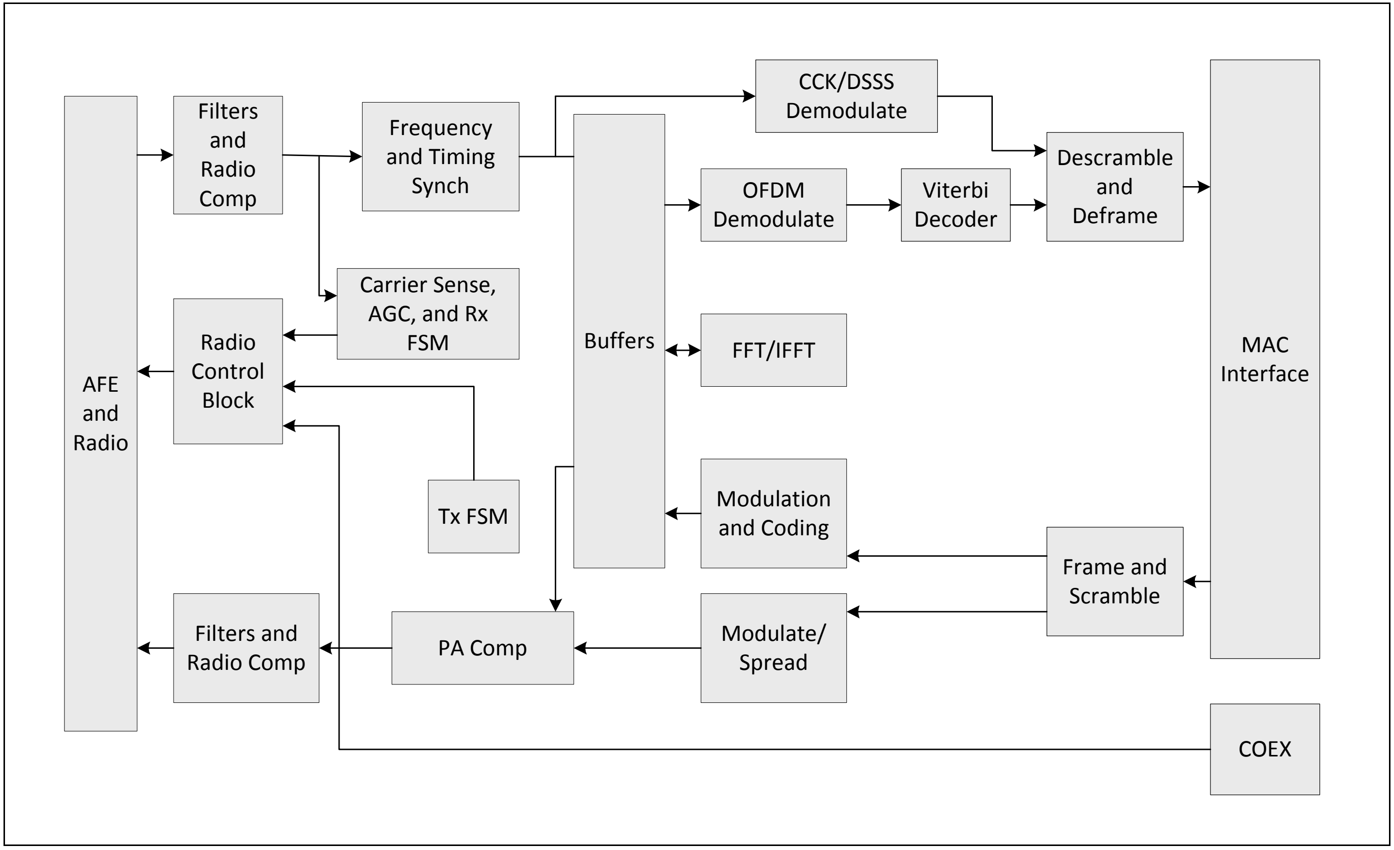
The CYW43364 WLAN digital PHY is designed to comply with IEEE 802.11b/g/n single stream to provide wireless LAN connectivity supporting data rates from 1 Mbps to 96 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to meet specification requirements in the presence of interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the filters, FFT, and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, and channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/IEEE 802.11b hybrid networks.

5.2.1 PHY Features

- Supports the IEEE 802.11b/g/n single-stream standards.
- Supports explicit IEEE 802.11n transmit beamforming.
- Supports optional Greenfield mode in TX and RX.
- Tx and Rx LDPC for improved range and power efficiency.
- Supports IEEE 802.11h/d for worldwide operation.
- Algorithms achieving low power, enhanced sensitivity, range, and reliability.
- Automatic gain control scheme for blocking and nonblocking application scenarios for cellular applications.
- Closed-loop transmit power control.
- Designed to meet FCC and other regulatory requirements.
- Support for 2.4 GHz Cypress TurboQAM data rates and 20 MHz channel bandwidth.

Figure 10. WLAN PHY Block Diagram



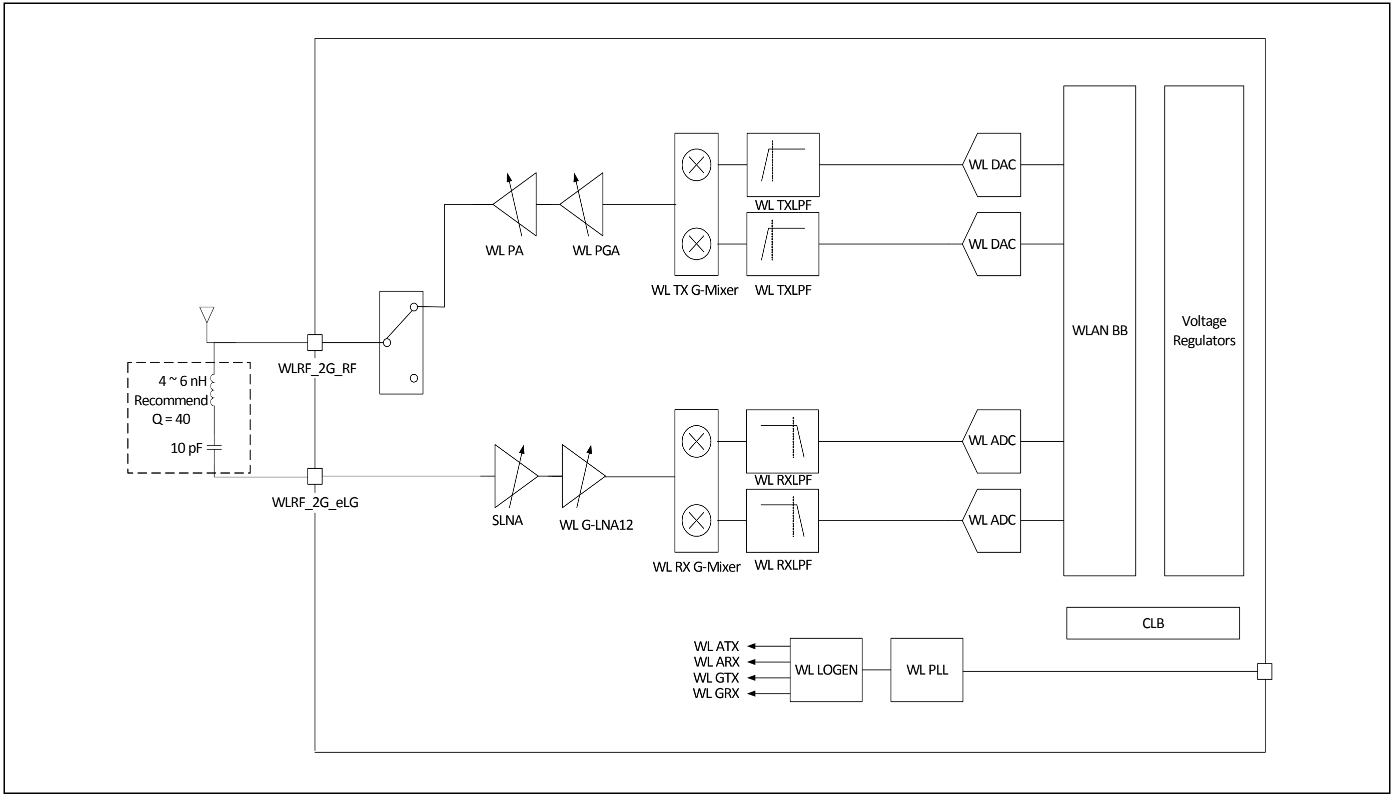
The PHY is capable of fully calibrating the RF front-end to extract the highest performance. On power-up, the PHY performs a full calibration suite to correct for IQ mismatch and local oscillator leakage. The PHY also performs periodic calibration to compensate for any temperature related drift, thus maintaining high-performance over time. A closed-loop transmit control algorithm maintains the output power at its required level and can control TX power on a per-packet basis.

6. WLAN Radio Subsystem

The CYW43364 includes an integrated WLAN RF transceiver that has been optimized for use in 2.4 GHz Wireless LAN systems. It is designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions. Improvements to the radio design include shared TX/RX baseband filters and high immunity to supply noise.

Figure 11 shows the radio functional block diagram.

Figure 11. Radio Functional Block Diagram



6.1 Receive Path

The CYW43364 has a wide dynamic range, direct conversion receiver. It employs high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band.

6.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band. A linear on-chip power amplifier is included, which is capable of delivering high output powers while meeting IEEE 802.11b/g/n specifications without the need for an external PA. This PA is supplied by an internal LDO that is directly supplied by VBAT, thereby eliminating the need for a separate PALDO. Closed-loop output power control is integrated.

6.3 Calibration

The CYW43364 features dynamic on-chip calibration, eliminating process variation across components. This enables the CYW43364 to be used in high-volume applications because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically during normal radio operation. Automatic calibration examples include baseband filter calibration for optimum transmit and receive performance and LOFT calibration for leakage reduction. In addition, I/Q calibration, R calibration, and VCO calibration are performed on-chip.

7. CPU and Global Functions

7.1 WLAN CPU and Memory Subsystem

The CYW43364 includes an integrated ARM Cortex-M3 processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debugging. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M with support for the Thumb-2 instruction set. ARM Cortex-M3 provides a 30% performance gain over ARM7TDMI.

At 0.19 µW/MHz, the Cortex-M3 is the most power efficient general purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for code and data access (ICode/DCode and system buses). ARM Cortex-M3 supports extensive debug features including real-time tracing of program execution.

On-chip memory for the CPU includes 512 KB SRAM and 640 KB ROM.

7.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 4096-bit One-Time Programmable (OTP) memory, which is read by system software after a device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address, can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP memory programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package. Documentation on the OTP development process is available on the Cypress customer support portal (http://community.cypress.com/).

7.3 GPIO Interface

Five general-purpose I/O (GPIO) pins are available on the CYW43364 that can be used to connect to various external devices.

GPIOs are tristated by default. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. They can also be programmed to have internal pull-up or pull-down resistors.

GPIO_0 is normally used as a WL_HOST_WAKE signal.

The CYW43364 supports 2-wire, 3-wire, and 4-wire coexistence configurations using GPIO_1 through GPIO_4. The signal functions of GPIO_1 through GPIO_4 are programmable to support the three coexistence configurations.

7.4 External Coexistence Interface

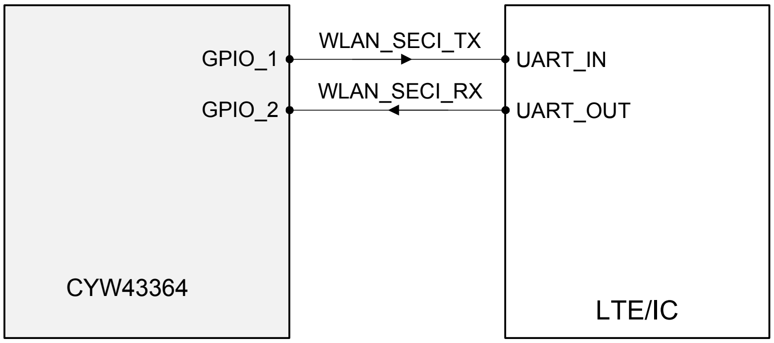
The CYW43364 supports 2-wire, 3-wire, and 4-wire coexistence interfaces to enable signaling between the device and an external colocated wireless device in order to manage wireless medium sharing for optimal performance. The external colocated device can be any of the following ICs: GPS, WiMAX, LTE, or UWB. An LTE IC is used in this section for illustration.

7.4.1 2-Wire Coexistence

Figure 12 shows a 2-wire LTE coexistence example. The following definitions apply to the GPIOs in the figure:

- GPIO_1: WLAN_SECI_TX output to an LTE IC.
- GPIO_2: WLAN_SECI_RX input from an LTE IC.

Figure 12. 2-Wire Coexistence Interface to an LTE IC



Note: WLAN_SECI_OUT and WLAN_SECI_IN are multiplexed on the GPIOs.

7.4.2 3-Wire and 4-Wire Coexistence Interfaces

Figure 13 and Figure 14 show 3-wire and 4-wire LTE coexistence examples, respectively. The following definitions apply to the GPIOs in the figures:

- For the 3-wire coexistence interface:
- GPIO_2: WLAN priority output to an LTE IC.
- GPIO_3: LTE_RX input from an LTE IC.
- GPIO_4: LTE_TX input from an LTE IC.

For the 4-wire coexistence interface:

- GPIO_1: WLAN priority output to an LTE IC.
- GPIO_2: LTE frame sync input from an LTE IC. This GPIO applies only to the 4-wire coexistence interface.
- GPIO_3: LTE_RX input from an LTE IC.
- GPIO_4: LTE_TX input from an LTE IC.

Figure 13. 3-Wire Coexistence Interface to an LTE IC

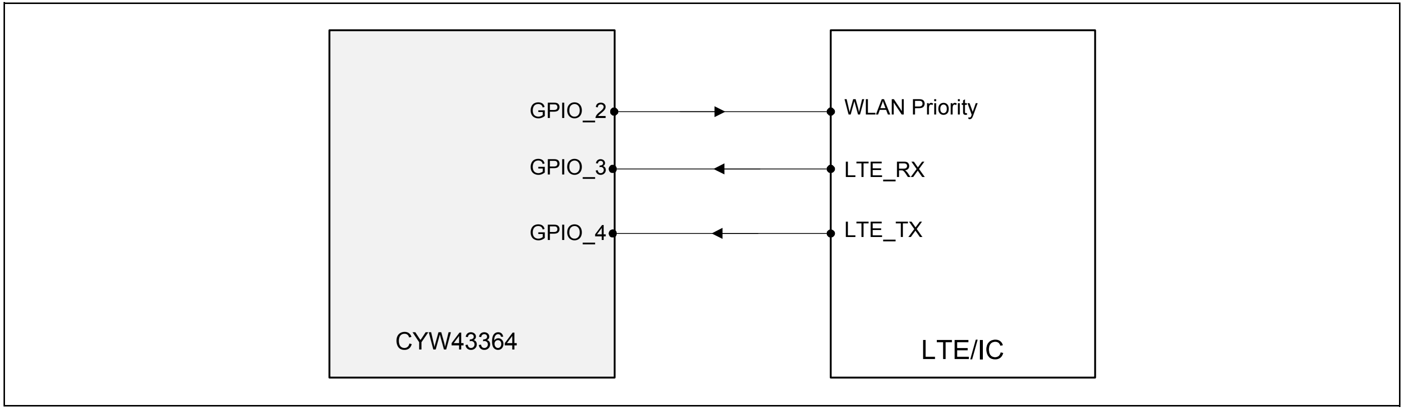
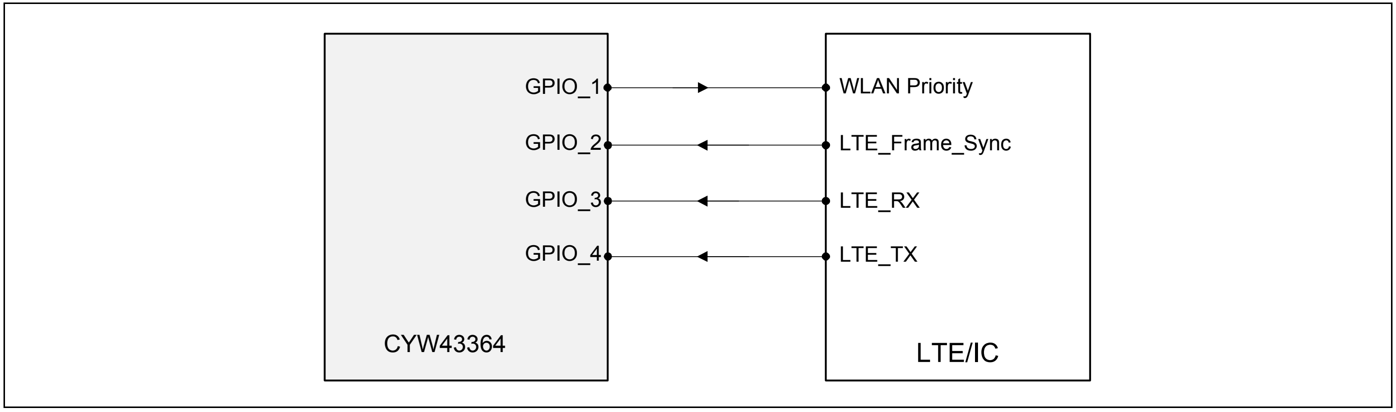


Figure 14. 4-Wire Coexistence Interface to an LTE IC



7.5 JTAG Interface

The CYW43364 supports the IEEE 1149.1 JTAG boundary scan standard over SDIO for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Cypress to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

7.6 UART Interface

One UART interface can be enabled by software as an alternate function on the JTAG pins. UART_RX is available on the JTAG_TDI pin, and UART_TX is available on the JTAG_TDO pin.

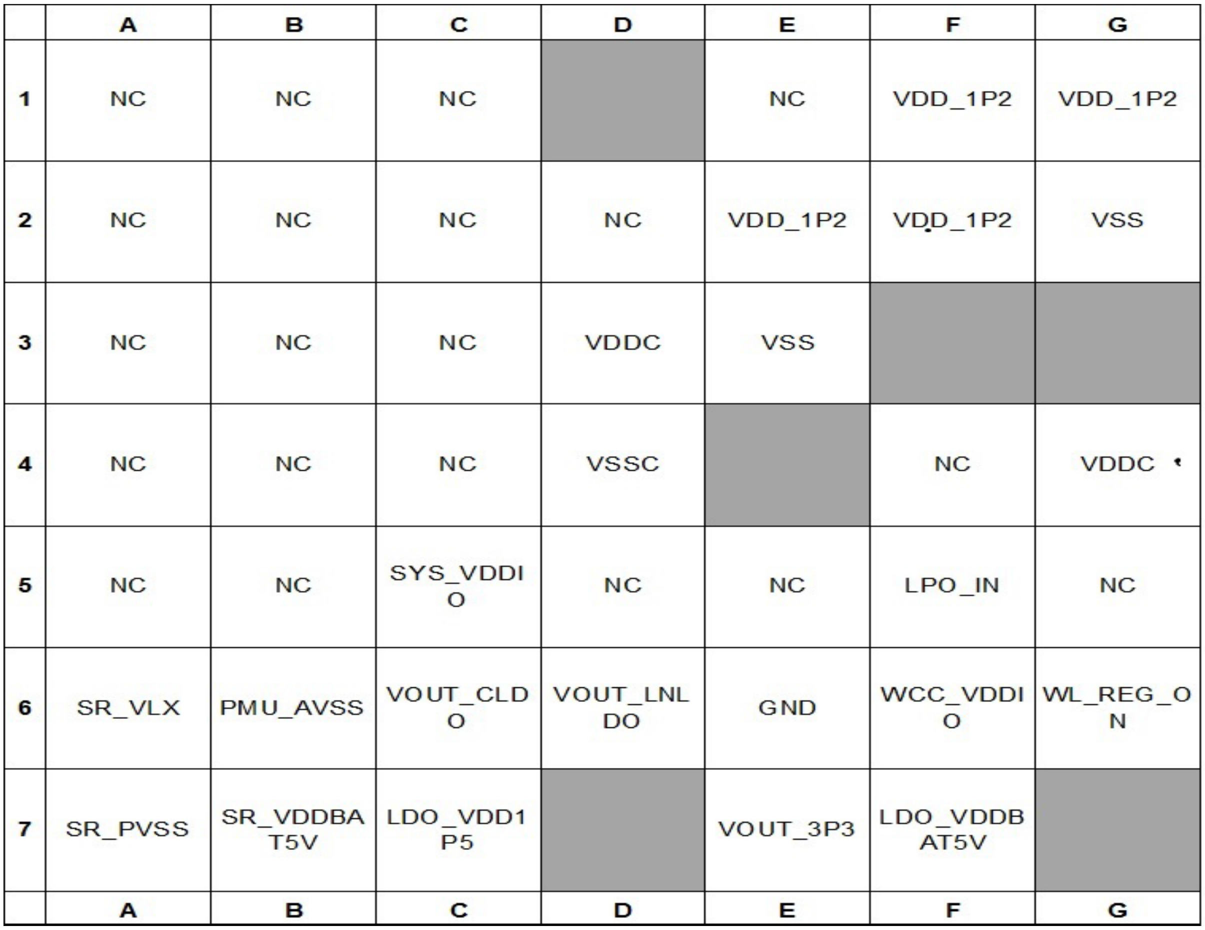
The UART is primarily for debugging during development. By adding an external RS-232 transceiver, this UART enables the CYW43364 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and it provides a FIFO size of 64 × 8 in each direction.

8. Pinout and Signal Descriptions

8.1 Ball Map

Figure 15 shows the 74-ball WLBGA ball map.

Figure 15. 74-Ball WLBGA Ball Map (Bottom View)



	A	B	C	D	E	F	G
1	NC	NC	NC		NC	VDD_1P2	VDD_1P2
2	NC	NC	NC	NC	VDD_1P2	VDD_1P2	VSS
3	NC	NC	NC	VDDC	VSS		
4	NC	NC	NC	VSSC		NC	VDDC
5	NC	NC	SYS_VDDIO	NC	NC	LPO_IN	NC
6	SR_VLX	PMU_AVSS	VOUT_CLDO	VOUT_LNLDO	GND	WCC_VDDIO	WL_REG_ON
7	SR_PVSS	SR_VDDBAT5V	LDO_VDD1P5		VOUT_3P3	LDO_VDDBAT5V	
	A	B	C	D	E	F	G

8.2 WLBGA Ball List in Ball Number Order with X-Y Coordinates

Table 6 provides ball numbers and names in ball number order. The table includes the X and Y coordinates for a top view with a (0,0) center.

Table 6. CYW43364 WLBGA Ball List — Ordered By Ball Number

Ball Number	Ball Name	X Coordinate	Y Coordinate
A1	NC	–1200.006	2199.996
A2	NC	–799.992	2199.996
A3	NC	–399.996	2199.996
A4	NC	0	2199.996
A5	NC	399.996	2199.996
A6	SR_VLX	799.992	2199.978
A7	SR_PVSS	1199.988	2199.978
B1	NC	–1200.006	1800
B2	NC	–799.992	1800
B3	NC	–399.996	1800
B4	NC	0	1800
B5	NC	399.996	1800
B6	PMU_AVSS	799.992	1799.982
B7	SR_VBAT5V	1199.988	1799.982
C1	NC	–1200.006	1399.995
C2	NC	–799.992	1399.986
C3	NC	–399.996	1399.995
C4	NC	0	1399.995
C5	SYS_VDDIO	399.996	1399.986
C6	VOUT_CLDO	799.992	1399.986
C7	LDO_VDD15V	1199.988	1399.986
D2	NC	–799.992	999.99
D3	VDDC	–399.996	999.999
D4	VSSC	0	999.999
D5	NC	399.996	999.99
D6	VOUT_LNLDO	799.992	999.99
E1	NC	–1199.988	599.994
E2	VDD_1P2	–799.992	599.994
E3	VSS	–399.996	599.994
E5	NC	399.996	599.994
E6	GND	799.992	599.994
E7	VOUT_3P3	1199.988	599.994
F1	VDD_1P2	–1199.988	199.998
F2	VDD_1P2	–799.992	199.998
F4	NC	0	199.998
F5	LPO_IN	399.996	199.998
F6	WCC_VDDIO	800.001	199.998
F7	LDO_VBAT5V	1199.988	199.998

Table 6. CYW43364 WLBGA Ball List — Ordered By Ball Number

Ball Number	Ball Name	X Coordinate	Y Coordinate
G1	VDD_1P2	–1199.988	–199.998
G2	VSS	–799.992	–199.998
G4	VDDC	0	–199.998
G5	NC	399.996	–199.998
G6	WL_REG_ON	800.001	–199.998
H1	VDDB_PA	–1199.988	–599.994
H2	VSS	–799.992	–599.994
H3	VSS	–399.996	–599.994
H4	WLRF_AFE_GND	0	–599.994
H5	NC	399.996	–599.994
H6	GPIO_1	800.001	–599.994
H7	SDIO_DATA_1	1200.006	–599.994
J1	WLRF_2G_eLG	–1199.988	–999.99
J2	WLRF_LNA_GND	–799.992	–999.99
J3	WLRF_GPIO	–399.996	–999.99
J5	VSSC	399.996	–999.999
J6	GPIO_0	800.001	–999.999
J7	SDIO_DATA_3	1200.006	–999.999
K1	WLRF_2G_RF	–1199.988	–1399.986
K2	WLRF_GENERAL_GND	–799.992	–1399.986
K4	GPIO_3	0	–1399.995
K5	GPIO_4	399.996	–1399.995
K6	SDIO_DATA_0	800.001	–1399.995
L2	WLRF_PA_GND	–799.992	–1799.982
L3	WLRF_VCO_GND	–399.996	–1799.982
L4	WLRF_XTAL_GND	0	–1799.982
L5	GPIO_2	399.996	–1799.991
L6	SDIO_CMD	800.001	–1799.991
L7	SDIO_DATA_2	1200.006	–1799.991
M1	WLRF_PA_VDD	–1199.988	–2199.978
M2	WLRF_VDD_1P35	–799.992	–2199.978
M3	WLRF_XTAL_VDD1P2	–399.996	–2199.978
M4	WLRF_XTAL_XOP	0	–2199.978
M5	WLRF_XTAL_XON	399.996	–2199.978
M6	CLK_REQ	800.001	–2199.996
M7	SDIO_CLK	1200.006	–2199.996

8.3 WLBGA Ball List Ordered By Ball Name

Table 7 provides the ball numbers and names in ball name order.

Table 7. CYW43364 WLBGA Ball List — Ordered By Ball Name

Ball Name	Ball Number
CLK_REQ	M6
GND	E6
GPIO_0	J6
GPIO_1	H6
GPIO_2	L5
GPIO_3	K4
GPIO_4	K5
LDO_VDD1P5	C7
LDO_VDDBAT5V	F7
LPO_IN	F5
NC	A1
NC	A2
NC	A3
NC	A4
NC	A5
NC	B1
NC	B2
NC	B3
NC	B4
NC	B5
NC	C1
NC	C2
NC	C3
NC	C4
NC	D2
NC	D5
NC	E1
NC	E5
NC	F4
NC	G5
NC	H5
PMU_AVSS	B6
SDIO_CLK	M7
SDIO_CMD	L6
SDIO_DATA_0	K6
SDIO_DATA_1	H7
SDIO_DATA_2	L7
SDIO_DATA_3	J7
SR_PVSS	A7
SR_VDDBAT5V	B7
SR_VLX	A6
SYS_VDDIO	C5
VDD_1P2	E2
VDD_1P2	F1
VDD_1P2	F2
VDD_1P2	G1
VDDB_PA	H1
VDDC	D3
VDDC	G4
VOUT_3P3	E7
VOUT_CLDO	C6
VOUT_LNLDO	D6
VSS	E3
VSS	G2
VSS	H2
VSS	H3
VSSC	D4
VSSC	J5
WCC_VDDIO	F6
WL_REG_ON	G6
WLRF_2G_eLG	J1
WLRF_2G_RF	K1
WLRF_AFE_GND	H4
WLRF_GENERAL_GND	K2
WLRF_GPIO	J3
WLRF_LNA_GND	J2
WLRF_PA_GND	L2
WLRF_PA_VDD	M1
WLRF_VCO_GND	L3
WLRF_VDD_1P35	M2
WLRF_XTAL_GND	L4
WLRF_XTAL_VDD1P2	M3
WLRF_XTAL_XON	M5
WLRF_XTAL_XOP	M4

8.4 Signal Descriptions

Table 8 provides the WLBGA package signal descriptions.

Table 8. WLBGA Signal Descriptions

Signal Name	WLBGA Ball	Type	Description
RF Signal Interface			
WLRF_2G_RF	K1	O	2.4 GHz WLAN RF output port.
SDIO Bus Interface			
SDIO_CLK	M7	I	SDIO clock input.
SDIO_CMD	L6	I/O	SDIO command line.
SDIO_DATA_0	K6	I/O	SDIO data line 0.
SDIO_DATA_1	H7	I/O	SDIO data line 1.
SDIO_DATA_2	L7	I/O	SDIO data line 2. Also used as a strapping option (see Table 11 on page 31).
SDIO_DATA_3	J7	I/O	SDIO data line 3.
Note: Per Section 6 of the SDIO specification, 10 to 100 kΩ pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO host pull-ups.			
WLAN GPIO Interface			
WLRF_GPIO	J3	I/O	Test pin. Not connected in normal operation.
Clocks			
WLRF_XTAL_XON	M5	O	XTAL oscillator output.
WLRF_XTAL_XOP	M4	I	XTAL oscillator input.
CLK_REQ	M6	O	External system clock request—Used when the system clock is not provided by a dedicated crystal (for example, when a shared TCXO is used). Asserted to indicate to the host that the clock is required.
LPO_IN	F5	I	External sleep clock input (32.768 kHz). If an external 32.768 kHz clock cannot be provided, pull this pin low. However, BLE will be always on and cannot go to deep sleep.
No Connect			
NC_A1	A1	I	No connect.
NC_A2	A2	O	No connect.
NC_A3	A3	I/O	No connect.
NC_A4	A4	I/O	No connect.
NC_A5	A5	I/O	No connect.
NC_B1	B1	I/O	No connect.
NC_B2	B2	I	No connect.
NC_B3	B3	I/O	No connect.
NC_B4	B4	O	No connect.
NC_B5	B5	I/O	No connect.
NC_C1	C1	I/O	No connect.
NC_C2	C2	O	No connect.

Table 8. WLBGA Signal Descriptions (Cont.)

Signal Name	WLBGA Ball	Type	Description
NC_C3	C3	O	No connect.
NC_C4	C4	I	No connect.
NC_D2	D2	O	No connect.
NC_E1	E1	I	No connect.
NC_F4	F4	I/O	No connect.
NC_G5	G5	I/O	No connect.
NC_H5	H5	I/O	No connect.
NC_E5	E5	N/A	Not used. Do not connect to this pin.
NC_D5	D5	N/A	Not used. Do not connect to this pin.
Miscellaneous			
WL_REG_ON	G6	I	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
GND_E6	E6	I	Tie pin E6 to ground.
GPIO_0	J6	I/O	Programmable GPIO pins. This pin becomes an output pin when it is used as WLAN_HOST_WAKE/ out-of-band signal.
GPIO_1	H6	I/O	Programmable GPIO pins.
GPIO_2	L5	I/O	Programmable GPIO pins.
GPIO_3	K4	I/O	Programmable GPIO pins.
GPIO_4	K5	I/O	Programmable GPIO pins.
WLRF_2G_eLG	J1	I	Connect to an external inductor. See the reference schematic for details.
Integrated Voltage Regulators			
SR_VDDBAT5V	B7	I	SR VBAT input power supply.
SR_VLX	A6	O	CBUCK switching regulator output. See Table 20 on page 42 for details of the inductor and capacitor required on this output.
LDO_VDDBAT5V	F7	I	LDO VBAT.
LDO_VDD1P5	C7	I	LNLDO input.
VOUT_LNLDO	D6	O	Output of low-noise LNLDO.
VOUT_CLDO	C6	O	Output of core LDO.
VDDB_PA	H1	I	Connect to VOUT_3P3.
VDD_1P2	G1	I	Connect to VOUT_LNLDO.
VDD_1P2	F2	I	Connect to VOUT_LNLDO.
VDD_1P2	F1	I	Connect to VOUT_LNLDO.
VDD_1P2	E2	I	Connect pin E2 to VOUT_LNLDO.
Power Supplies			
WLRF_XTAL_VDD1P2	M3	I	XTAL oscillator supply.
WLRF_PA_VDD	M1	I	Power amplifier supply.
WCC_VDDIO	F6	I	VDDIO input supply. Connect to VDDIO.

Table 8. WLBGA Signal Descriptions (Cont.)

Signal Name	WLBGA Ball	Type	Description
SYS_VDDIO	C5	I	VDDIO input supply. Connect to VDDIO.
WLRF_VDD_1P35	M2	I	LNLDO input supply.
VDDC	D3, G4	I	Core supply for WLAN.
VOUT_3P3	E7	O	3.3V output supply. See the reference schematic for details.
Ground			
VSS_H2	H2	I	Connect to ground.
VSS_G2	G2	I	Connect to ground.
VSS_H3	H3	I	Connect to ground.
VSS_E3	E3	I	Connect to ground.
PMU_AVSS	B6	I	Quiet ground.
SR_PVSS	A7	I	Switcher-power ground.
VSSC	D4, J5	I	Core ground for WLAN.
WLRF_AFE_GND	H4	I	AFE ground.
WLRF_LNA_GND	J2	I	2.4 GHz internal LNA ground.
WLRF_GENERAL_GND	K2	I	Miscellaneous RF ground.
WLRF_PA_GND	L2	I	2.4 GHz PA ground.
WLRF_VCO_GND	L3	I	VCO/LO generator ground.
WLRF_XTAL_GND	L4	I	XTAL ground.

8.5 WLAN GPIO Signals and Strapping Options

The pins listed in Table 9 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to ground using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 9. GPIO Functions and Strapping Options

Pin Name	WLBGA Pin #	Default	Function	Description
SDIO_DATA_2	L7	1	WLAN host interface select	This pin selects the WLAN host interface mode. The default is SDIO.

8.6 Chip Debug Options

The chip can be accessed for debugging via the JTAG interface, multiplexed on the SDIO_DATA_0 through SDIO_DATA_3 (and SDIO_CLK) I/O depending on the bootstrap state of GPIO_1 and GPIO_2.

Table 10 shows the debug options of the device.

Table 10. Chip Debug Options

JTAG_SEL	GPIO_2	GPIO_1	Function	SDIO I/O Pad Function
0	0	0	Normal mode	SDIO
0	0	1	JTAG over SDIO	JTAG
0	1	1	SWD over GPIO_1/GPIO_2	SDIO

8.7 I/O States

The following notations are used in Table 11:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 11. I/O States

Name	I/O	Keeper	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down (WL_REG_ON=0 BT_REG_ON=don't care)	Out-of-Reset; (WL_REG_ON=1; BT_REG_ON=don't care)	(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs are Present	(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs are Present	Power Rail
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (200k)	Input; PD (200k)	–	–
CLK_REQ	I/O	Y	Open drain or push-pull (programmable). Active high.	Open drain or push-pull (programmable). Active high	PD	Open drain, active high.	Open drain, active high.	Open drain, active high.	WCC_VDDIO
SDIO_DATA_0	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO
SDIO_DATA_1	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO
SDIO_DATA_2	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO
SDIO_DATA_3	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO
SDIO_CMD	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO
SDIO_CLK	I	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	Input	WCC_VDDIO
JTAG_SEL	I	Y	PD	PD	High-Z, NoPull	Input, PD	PD	Input, PD	WCC_VDDIO
GPIO_0	I/O	Y	TBD	Active mode	High-Z, NoPull[a]	Input, SDIO OOB Int, NoPull	Active mode	Input, NoPull	WCC_VDDIO
GPIO_1	I/O	Y	TBD	Active mode	High-Z, NoPull[a]	Input, PD	Active mode	Input, Strap, PD	WCC_VDDIO
GPIO_2	I/O	Y	TBD	Active mode	High-Z, NoPull[a]	Input, GCI GPIO[7], NoPull	Active mode	Input, Strap, NoPull	WCC_VDDIO
GPIO_3	I/O	Y	TBD	Active mode	High-Z, NoPull[a]	Input, GCI GPIO[0], PU	Active mode	Input, PU	WCC_VDDIO
GPIO_4	I/O	Y	TBD	Active mode	High-Z, NoPull[a]	Input, GCI GPIO[1], PU	Active mode	Input, PU	WCC_VDDIO

Table 11. I/O States (Cont.)

Name	I/O	Keeper	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down (WL_REG_ON=0 BT_REG_ON=don't care)	Out-of-Reset; (WL_REG_ON=1; BT_REG_ON=don't care)	(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs are Present	(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs are Present	Power Rail

Note:

1. Keeper column: N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in the Power-down state.
2. If there is no keeper, and it is an input and there is Nopull, then the pad should be driven to prevent leakage due to a floating pad (e.g., SDIO_CLK).
3. In the Power-down state (xx_REG_ON = 0): High-Z; NoPull => The pad is disabled because power is not supplied.
4. Depending on whether the PCM interface is enabled and the configuration is master or slave mode, it can be either an output or input.
5. Depending on whether the I^{2}S interface is enabled and the configuration is master or slave mode, it can be either an output or input.
6. The GPIO pull states for the Active and Low-Power states are hardware defaults. They can all be subsequently programmed as pull-ups or pull-downs.
7. Regarding GPIO pins, the following are the pull-up and pull-down values for both 3.3V and 1.8V VDDIO:

	Minimum (kΩ)	**Typical (kΩ)**	**Maximum (kΩ)**
3.3V VDDIO pull-downs:	51.5	44.5	38
3.3V VDDIO pull-ups:	37.4	39.5	44.5
1.8V VDDIO pull-downs:	64	83	116
1.8V VDDIO pull-ups:	65	86	118

a. The GPIO pull states for the active and low-power states are hardware defaults. They can all be subsequently programmed as a pull-up or pull-down.

9. DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

9.1 Absolute Maximum Ratings

Caution: The absolute maximum ratings in Table 12 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Excluding VBAT, operation at the absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 12. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	VBAT	–0.5 to +6.0[a]	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
Maximum undershoot voltage for I/O[b]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[b]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	125	°C

a. Continuous operation at 6.0V is supported.
b. Duration not to exceed 25% of the duty cycle.

9.2 Environmental Ratings

The environmental ratings are shown in Table 13.

Table 13. Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient temperature (T_A)	–30 to +70°C [a]	°C	Operation
Storage temperature	–40 to +125°C	°C	–
Relative humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed, but specifications require derating at extreme temperatures (see the specification tables for details).

9.3 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 14. ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human Body Model Contact Discharge per JEDEC EID/JESD22-A114	1250	V
Machine Model (MM)	ESD_HAND_MM	Machine Model Contact	50	V
CDM	ESD_HAND_CDM	Charged Device Model Contact Discharge per JEDEC EIA/JESD22-C101	300	V

9.4 Recommended Operating Conditions and DC Characteristics

Functional operation is not guaranteed outside the limits shown in Table 15, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 15. Recommended Operating Conditions and DC Characteristics

Element	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.0[a]	–	4.8[b]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
SDIO Interface I/O Pins					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	–	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.25 × VDDIO	V
Output high voltage @ 2 mA	VOH	0.75 × VDDIO	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					

Table 15. Recommended Operating Conditions and DC Characteristics (Cont.)

Element	Symbol	Value			Unit
		Minimum	Typical	Maximum	
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low Voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[c]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

[a] The CYW43364 is functional across this range of voltages. However, optimal RF performance specified in the data sheet is guaranteed only for 3.2V < VBAT < 4.8V.

[b] The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration over the lifetime of the device are allowed.

[c] Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

10. WLAN RF Specifications

The CYW43364 includes an integrated direct conversion radio that supports the 2.4 GHz band. This section describes the RF characteristics of the 2.4 GHz radio.

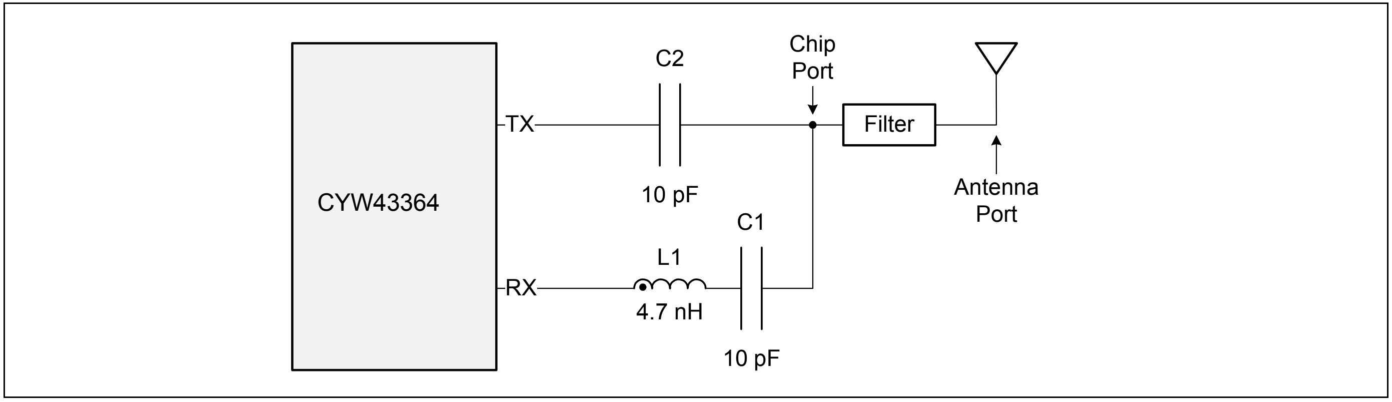
Note: Values in this data sheet are design goals and may change based on device characterization results.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 13 on page 33 and Table 15 on page 34. Functional operation outside these limits is not guaranteed.

Typical values apply for the following conditions:

- VBAT = 3.6V.
- Ambient temperature +25°C.

Figure 16. RF Port Location



Note: All specifications apply at the chip port unless otherwise specified.

10.1 2.4 GHz Band General RF Specifications

Table 16. 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs

10.2 WLAN 2.4 GHz Receiver Performance Specifications

Note: Unless otherwise specified, the specifications in Table 17 are measured at the chip port (for the location of the chip port, see Figure 16 on page 36).

Table 17. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
RX sensitivity (8% PER for 1024 octet PSDU) [a]	1 Mbps DSSS	–97.5	–99.5	–	dBm
	2 Mbps DSSS	–93.5	–95.5	–	dBm
	5.5 Mbps DSSS	–91.5	–93.5	–	dBm
	11 Mbps DSSS	–88.5	–90.5	–	dBm
RX sensitivity (10% PER for 1000 octet PSDU) at WLAN RF port [a]	6 Mbps OFDM	–91.5	–93.5	–	dBm
	9 Mbps OFDM	–90.5	–92.5	–	dBm
	12 Mbps OFDM	–87.5	–89.5	–	dBm
	18 Mbps OFDM	–85.5	–87.5	–	dBm
	24 Mbps OFDM	–82.5	–84.5	–	dBm
	36 Mbps OFDM	–80.5	–82.5	–	dBm
	48 Mbps OFDM	–76.5	–78.5	–	dBm
	54 Mbps OFDM	–75.5	–77.5	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU). Defined for default parameters: GF, 800 ns GI.	20 MHz channel spacing for all MCS rates (Mixed mode)				
	256-QAM, R = 5/6	–67.5	–69.5	–	dBm
	256-QAM, R = 3/4	–69.5	–71.5	–	dBm
	MCS7	–71.5	–73.5	–	dBm
	MCS6	–73.5	–75.5	–	dBm
	MCS5	–74.5	–76.5	–	dBm
	MCS4	–79.5	–81.5	–	dBm
	MCS3	–82.5	–84.5	–	dBm
	MCS2	–84.5	–86.5	–	dBm
	MCS1	–86.5	–88.5	–	dBm
	MCS0	–90.5	–92.5	–	dBm

Table 17. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Blocking level for 3 dB Rx sensitivity degradation (without external filtering)	704–716	LTE	–	–13	–	dBm
	777–787	LTE	–	–13	–	dBm
	776–794 MHz	CDMA2000	–	–13.5	–	dBm
	815–830	LTE	–	–12.5	–	dBm
	816–824	CDMA2000	–	–13.5	–	dBm
	816–849	LTE	–	–11.5	–	dBm
	824–849	WCDMA	–	–11.5	–	dBm
	824–849	CDMA2000	–	–12.5	–	dBm
	824–849	LTE	–	–11.5	–	dBm
	824–849	GSM850	–	–8	–	dBm
	830–845	LTE	–	–11.5	–	dBm
	832–862	LTE	–	–11.5	–	dBm
	880–915	WCDMA	–	–10	–	dBm
	880–915	LTE	–	–12	–	dBm
	880–915	E-GSM	–	–9	–	dBm
	1710–1755	WCDMA	–	–13	–	dBm
	1710–1755	LTE	–	–14.5	–	dBm
	1710–1755	CDMA2000	–	–14.5	–	dBm
	1710–1785	WCDMA	–	–13	–	dBm
	1710–1785	LTE	–	–14.5	–	dBm
	1710–1785	GSM1800	–	–12.5	–	dBm
	1850–1910	GSM1900	–	–11.5	–	dBm
	1850–1910	CDMA2000	–	–16	–	dBm
	1850–1910	WCDMA	–	–13.5	–	dBm
	1850–1910	LTE	–	–16	–	dBm
	1850–1915	LTE	–	–17	–	dBm
	1920–1980	WCDMA	–	–17.5	–	dBm
Blocking level for 3 dB Rx sensitivity degradation (without external filtering) (cont.)	1920–1980	CDMA2000	–	–19.5	–	dBm
	1920–1980	LTE	–	–19.5	–	dBm
	2300–2400	LTE	–	–44	–	dBm
	2500–2570	LTE	–	–43	–	dBm
	2570–2620	LTE	–	–34	–	dBm
	5G (WLAN)	WLAN	–	>–4	–	dBm
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–6	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–12	–	–	dBm
	@ 6–54 Mbps (10% PER, 1000 octets)		–15.5	–	–	dBm

Table 17. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection-DSSS. (Difference between interfering and desired signal [25 MHz apart] at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes.)	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM. (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1000[b] octet PSDU with desired signal level as specified in Condition/ Notes.)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
RCPI accuracy[c]	Range –98 dBm to –75 dBm		–3	–	3	dB
	Range above –75 dBm		–5	–	5	dB
Return loss	Zo = 50Ω across the dynamic range.		10	–	–	dB

[a] Optimal RF performance, as specified in this data sheet, is guaranteed only for temperatures between –10°C and 55°C.
[b] For 65 Mbps, the size is 4096.
[c] The minimum and maximum values shown have a 95% confidence level.

10.3 WLAN 2.4 GHz Transmitter Performance Specifications

Note: Unless otherwise specified, the specifications in Table 17 are measured at the chip port (for the location of the chip port, see Figure 16 on page 36).

Table 18. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and WLAN 5G band (at 21 dBm, 90% duty cycle, 1 Mbps CCK).	776–794 MHz	CDMA2000	–	–167.5	–	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	–	–163.5	–	dBm/Hz
	1450–1495	DAB	–	–154.5	–	dBm/Hz
	1570–1580 MHz	GPS	–	–152.5	–	dBm/Hz
	1592–1610 MHz	GLONASS	–	–149.5	–	dBm/Hz
	1710–1800	DSC-1800-Uplink	–	–145.5	–	dBm/Hz
	1805–1880 MHz	GSM 1800	–	–143.5	–	dBm/Hz
	1850–1910 MHz	GSM 1900	–	–140.5	–	dBm/Hz
	1910–1930 MHz	TDSCDMA,LTE	–	–138.5	–	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne, WCDMA	–	–139	–	dBm/Hz
	2010–2075 MHz	TDSCDMA	–	–127.5	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–124.5	–	dBm/Hz
	2305–2370	LTE Band 40	–	–104.5	–	dBm/Hz
	2370–2400	LTE Band 40	–	–81.5	–	dBm/Hz
	2496–2530	LTE Band 41	–	–94.5	–	dBm/Hz
	2530–2560	LTE Band 41	–	–120.5	–	dBm/Hz
	2570–2690	LTE Band 41	–	–121.5	–	dBm/Hz
	5000–5900	WLAN 5G	–	–109.5	–	dBm/Hz
Harmonic level (at 21 dBm with 90% duty cycle, 1 Mbps CCK)	4.8-5.0 GHz	2nd Harmonic	–	–26.5	–	dBm/MHz
	7.2-7.5 GHz	3rd Harmonic	–	–23.5	–	dBm/MHz
	9.6-10 GHz	4th Harmonic	–	–32.5	–	dBm/MHz
TX power at the chip port for the highest power level setting at 25°C, VBA = 3.6V, and spectral mask and EVM compliance[a, b]	EVM Does Not Exceed					
	IEEE 802.11b (DSSS/CCK)	–9 dB	21	–	–	dBm
	OFDM, BPSK	–8 dB	20.5	–	–	dBm
	OFDM, QPSK	–13 dB	20.5	–	–	dBm
	OFDM, 16-QAM	–19 dB	20.5	–	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	18	–	–	dBm
	OFDM, 64-QAM (R = 5/6)	–27 dB	17.5	–	–	dBm
	OFDM, 256-QAM (R = 5/6)	–32 dB	15	–	–	dBm

Table 18. WLAN 2.4 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
TX power control dynamic range	–		9	–	–	dB
Closed loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies across 5 to 21 dBm output power range.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Zo = 50		4	6	–	dB
Load pull variation for output power, EVM, and Adjacent Channel Power Ratio (ACPR)	VSWR = 2:1.	EVM degradation	–	3.5	–	dB
		Output power variation	–	±2	–	dB
		ACPR-compliant power level	–	15	–	dBm
	VSWR = 3:1.	EVM degradation	–	4	–	dB
		Output power variation	–	±3	–	dB
		ACPR-compliant power level	–	15	–	dBm

a. TX power for channel 1 and channel 11 is specified separately by nonvolatile memory parameters to ensure band-edge compliance.
b. Optimal RF performance, as specified in this data sheet, is guaranteed only for temperatures between –10°C and 55°C.

10.4 General Spurious Emissions Specifications

Table 19. General Spurious Emissions Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
TX emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–99	–96	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–44	–41	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–68	–65	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–88	–85	dBm
RX/standby emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–99	–96	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–54	–51	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–88	–85	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–88	–85	dBm

Note: The specifications in this table apply at the chip port.

11. Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on device characterization results.

Functional operation is not guaranteed outside of the specification limits provided in this section.

11.1 Core Buck Switching Regulator

Table 20. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	2.4	3.6	4.8[a]	V
PWM mode switching frequency	CCM, load > 100 mA VBAT = 3.6V.	–	4	–	MHz
PWM output current	–	–	–	370	mA
Output current limit	–	–	1400	–	mA
Output voltage range	Programmable, 30 mV steps. Default = 1.35V.	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode.	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static load, max. ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap + Board total-ESR < 20 mΩ, C_{out} > 1.9 µF, ESL<200 pH	–	7	20	mVpp
PWM mode peak efficiency	Peak efficiency at 200 mA load, inductor DCR = 200 mΩ, VBAT = 3.6V, VOUT = 1.35V	–	85	–	%
PFM mode efficiency	10 mA load current, inductor DCR = 200 mΩ, VBAT = 3.6V, VOUT = 1.35V	–	77	–	%
Start-up time from power down	VDDIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	400	500	µs
External inductor	0603 size, 2.2 µH ±20%, DCR = 0.2Ω ± 25%	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, 4.7 µF ±20%, 10V	2.0[b]	4.7	10[c]	µF
External input capacitor	For SR_VDDBATP5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ±4.7 µF ±20%, 10V	0.67[b]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

[a] The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.

[b] Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

[c] Total capacitance includes those connected at the far end of the active load.

11.2 3.3V LDO (LDO3P3)

Table 21. LDO3P3 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = V_o + 0.2V = 3.5V dropout voltage requirement must be met under maximum load for performance specifications.	3.1	3.6	4.8[a]	V
Output current	–	0.001	–	450	mA
Nominal output voltage, V_o	Default = 3.3V.	–	3.3	–	V
Dropout voltage	At max. load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load	–	66	85	µA
Line regulation	V_{in} from (V_o + 0.2V) to 4.8V, max. load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o + 0.2V$, V_o = 3.3V, C_o = 4.7 µF, Max. load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	160	250	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V	1.0[b]	4.7	5.64	µF
External input capacitor	For SR_VDDBATA5V pin (shared with band gap) Ceramic, X5R, 0402, (ESR: 30m-200 mΩ), ± 10%, 10V. Not needed if sharing VBAT capacitor 4.7 µF with SR_VDDBATP5V.	–	4.7	–	µF

[a] The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.

[b] Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

11.3 CLDO

Table 22. CLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = 1.2 + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	7	0.2	–	200	mA
Output voltage, V_o	Programmable in 10 mV steps. Default = 1.2.V	0.95	1.2	1.26	V
Dropout voltage	At max. load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	13	–	µA
	200 mA load	–	1.24	–	mA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load regulation	Load from 1 mA to 300 mA	–	0.02	0.05	mV/mA
Leakage current	Power down	–	5	20	µA
	Bypass mode	–	1	3	µA
PSRR	@1 kHz, Vin ≥ 1.35V, C_o = 4.7 µF	20	–	–	dB
Start-up time of PMU	VDDIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	µs
LDO turn-on time	LDO turn-on time when rest of the chip is up.	–	140	180	µs
External output capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	1.1[a]	2.2	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

[a] Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

11.4 LNLDO

Table 23. LNLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. $V_{IN} = V_O + 0.15V = 1.35V$ (where $V_O = 1.2V$) dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	10	12	µA
	Max. load	–	970	990	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, 200 mA load	–	–	5	mV/V
Load regulation	Load from 1 mA to 200 mA: $V_{in} \geq (V_o + 0.12V)$	–	0.025	0.045	mV/mA
Leakage current	Power-down, junction temp. = 85°C	–	5	20	µA
Output noise	@30 kHz, 60–150 mA load C_o = 2.2 µF @100 kHz, 60–150 mA load C_o = 2.2 µF	–	–	60 35	–nV/$\sqrt{Hz}$
PSRR	@1 kHz, $V_{in} \geq (V_o + 0.15V)$, C_o = 4.7 µF	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	140	180	µs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[a]	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1	2.2	µF

[a] Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

12. System Power Consumption

Note:

The values in this data sheet are design goals and are subject to change based on device characterization.Unless otherwise stated, these values apply for the conditions specified in Table 15 on page 34.

12.1 WLAN Current Consumption

Table 24 shows typical currents consumed by the CYW43364's WLAN section.

12.1.1 2.4 GHz Mode

Table 24. 2.4 GHz Mode WLAN Power Consumption

Mode	Rate	VBAT = 3.6V, VDDIO = 1.8V, TA 25°C	
		VBAT (mA)	Vio (µA)
Sleep Modes			
Leakage (OFF)	N/A	0.0035	0.08
Sleep (idle, unassociated) [a]	N/A	0.0058	80
Sleep (idle, associated, inter-beacons) [b]	Rate 1	0.0058	80
IEEE Power Save PM1 DTIM1 (Avg.) [c]	Rate 1	1.05	74
IEEE Power Save PM1 DTIM3 (Avg.) [d]	Rate 1	0.35	86
IEEE Power Save PM2 DTIM1 (Avg.) [c]	Rate 1	1.05	74
IEEE Power Save PM2 DTIM3 (Avg.) [d]	Rate 1	0.35	86
Active Modes			
Rx Listen Mode [e]	N/A	37	12
Rx Active (at –50dBm RSSI) [f]	Rate 1	39	12
	Rate 11	40	12
	Rate 54	40	12
	Rate MCS7	41	12
Tx [f]	Rate 1 @ 20 dBm	320	15
	Rate 11 @ 18 dBm	290	15
	Rate 54 @ 15 dBm	260	15
	Rate C7 @ 15 dBm	260	15

[a] Device is initialized in Sleep mode, but not associated.

[b] Device is associated, and then enters Power Save mode (idle between beacons).

[c] Beacon interval = 100 ms; beacon duration = 1 ms @ 1 Mbps (Integrated Sleep + wakeup + beacon).

[d] Beacon interval = 300 ms; beacon duration = 1 ms @ 1 Mbps (Integrated Sleep + wakeup + beacon).

[e] Carrier sense (CCA) when no carrier present.

[f] Tx output power is measured on the chip-out side; duty cycle =100%. Tx Active mode is measured in Packet Engine mode (pseudo-random data)

13. Interface Timing and AC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 13 on page 33 and Table 15 on page 34. Functional operation outside of these limits is not guaranteed.

13.1 SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 17 and Table 25 on page 48.

Figure 17. SDIO Bus Timing (Default Mode)

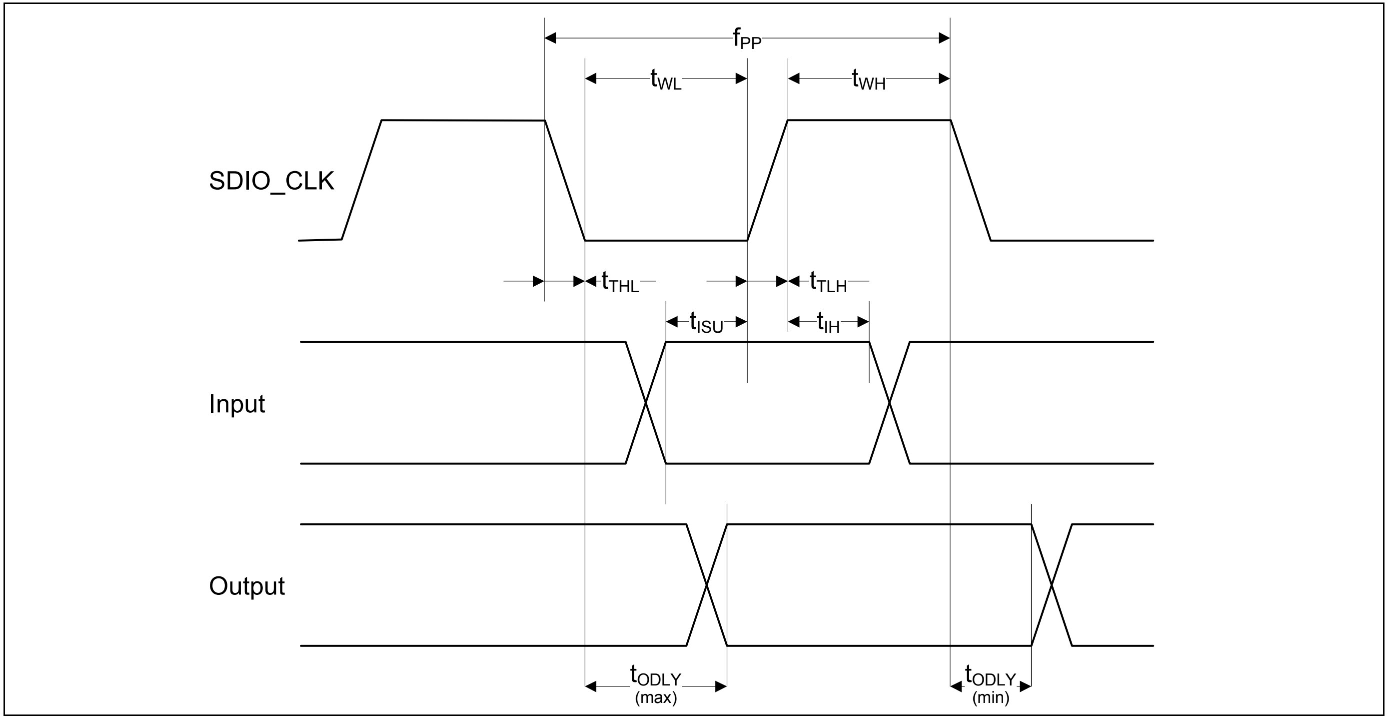


Table 25. SDIO Bus Timing [a] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency—Data Transfer mode	fPP	0	–	25	MHz
Frequency—Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock fall time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time—Data Transfer mode	tODLY	0	–	14	ns
Output delay time—Identification mode	tODLY	0	–	50	ns

[a] Timing is based on CL ≤ 40 pF load on command and data.
[b] Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

13.2 SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 18 and Table 26.

Figure 18. SDIO Bus Timing (High-Speed Mode)

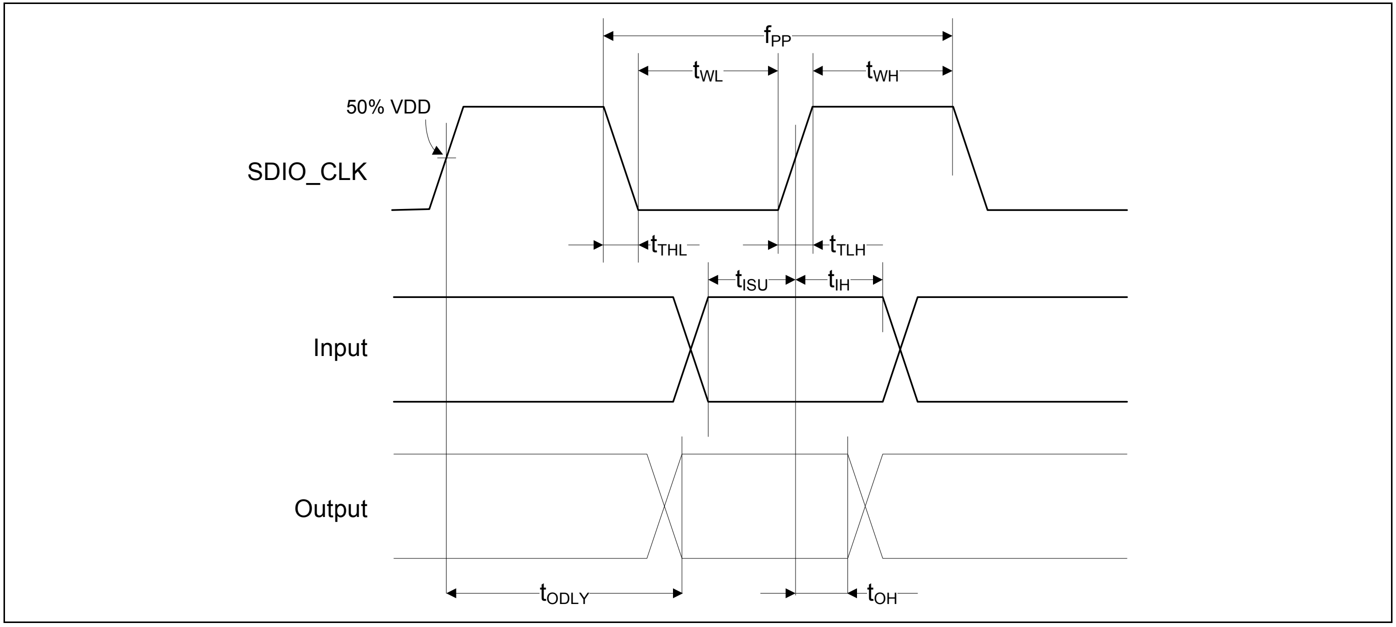


Table 26. SDIO Bus Timing [a] Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock fall time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	–	–	ns
Input hold time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

[a] Timing is based on CL ≤ 40 pF load on command and data.

[b] Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

13.3 JTAG Timing

Table 27. JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

14. Power-Up Sequence and Timing

14.1 Sequencing of Reset and Regulator Control Signals

The CYW43364 WL_REG_ON signal allows the host to control power consumption by enabling or disabling the WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 19 and Figure 20). The timing values indicated are minimum required values; longer delays are also acceptable.

Note:

- The CYW43364 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold (see Table 15 on page 34). Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.
- VBAT and VDDIO should not rise faster than 40 µs. VBAT should be up before or at the same time as VDDIO. VDDIO should not be present first or be held high before VBAT is high.

14.1.1 Control Signal Timing Diagrams

Figure 19. WLAN = ON

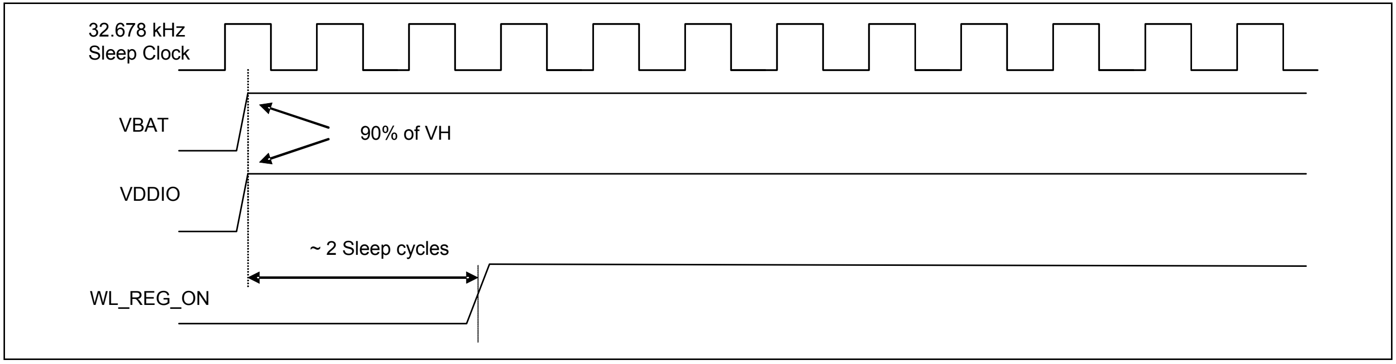
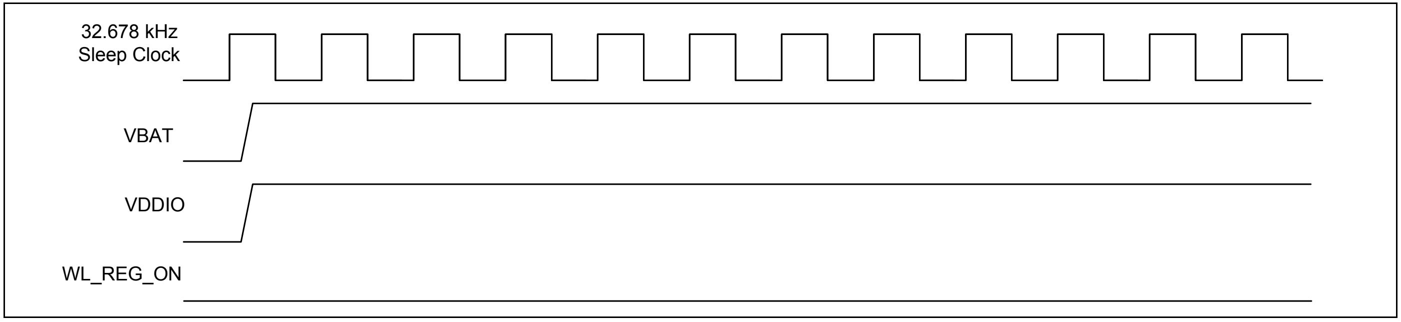


Figure 20. WLAN = OFF



15. Package Information

15.1 Package Thermal Characteristics

Table 28. Package Thermal Characteristics[a]

Characteristic	Value in Still Air
θ_{JA} (°C/W)	53.11
θ_{JB} (°C/W)	13.14
θ_{JC} (°C/W)	6.36
Ψ_{JT} (°C/W)	0.04
Ψ_{JB} (°C/W)	14.21
Maximum Junction Temperature T_j (°C)[b]	125
Maximum Power Dissipation (W)	1.2

[a] No heat sink, TA = 70°C. This is an estimate based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm x 114.3 mm x 1.6 mm) and P = 1.2W continuous dissipation.

[b] Absolute junction temperature limits maintained through active thermal monitoring and dynamic TX duty cycle limiting.

15.1.1 Junction Temperature Estimation and PSI Versus Theta$_{jc}$

Package thermal characterization parameter PSI-JT (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is as follows:

$$T_J = T_T + P \times \Psi_{JT}$$

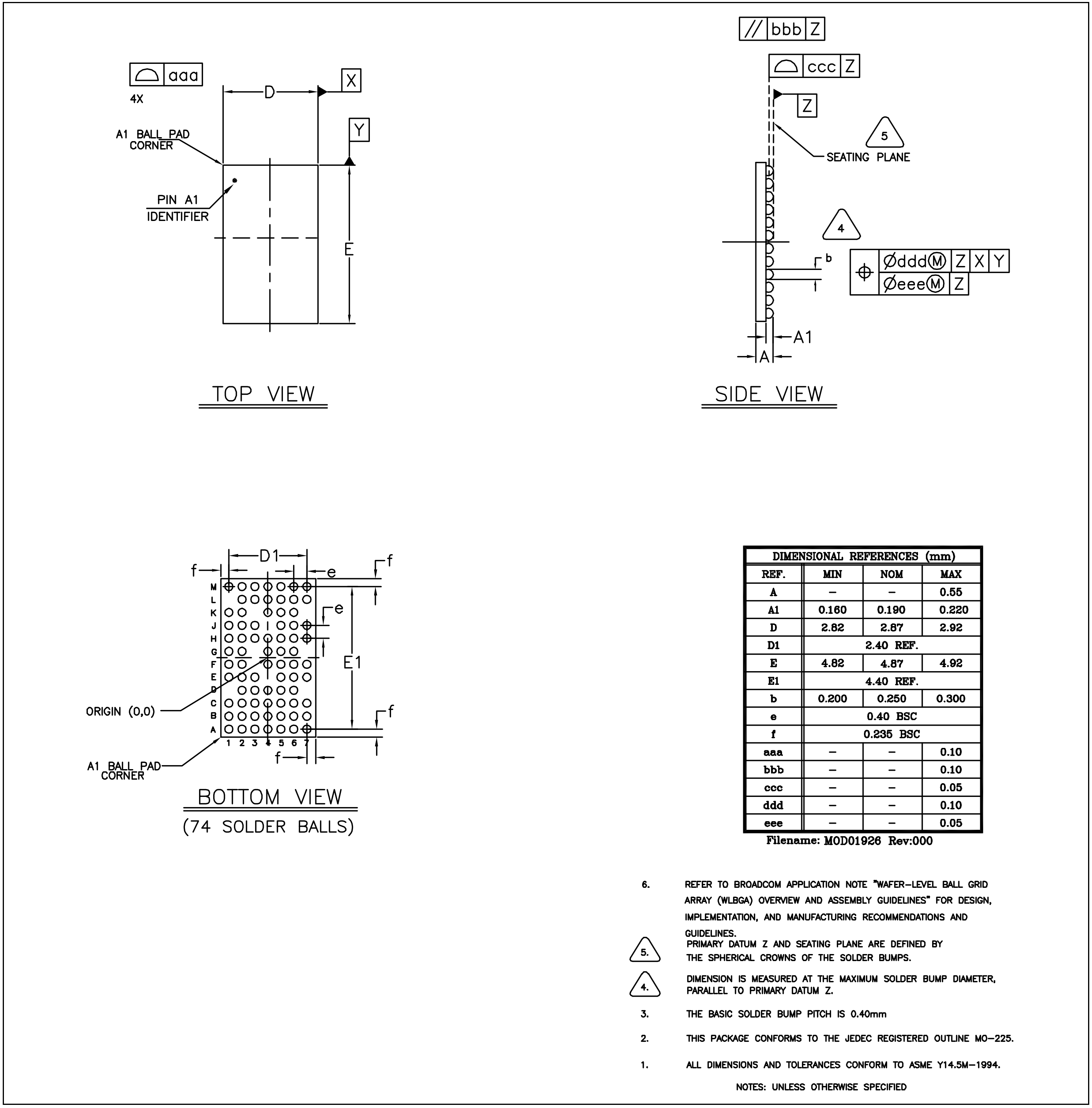
Where:

- T_J = junction temperature at steady-state condition, °C
- T_T = package case top center temperature at steady-state condition, °C
- P = device power dissipation, Watts
- Ψ_{JT} = package thermal characteristics (no airflow), °C/W

16. Mechanical Information

Figure 21 shows the mechanical drawing for the CYW43364 WLBGA package.

Figure 21. 74-Ball WLBGA Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.55
A1	0.160	0.190	0.220
D	2.82	2.87	2.92
D1	2.40 REF.		
E	4.82	4.87	4.92
E1	4.40 REF.		
b	0.200	0.250	0.300
e	0.40 BSC		
f	0.235 BSC		
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD01926 Rev:000

6. REFER TO BROADCOM APPLICATION NOTE "WAFER–LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

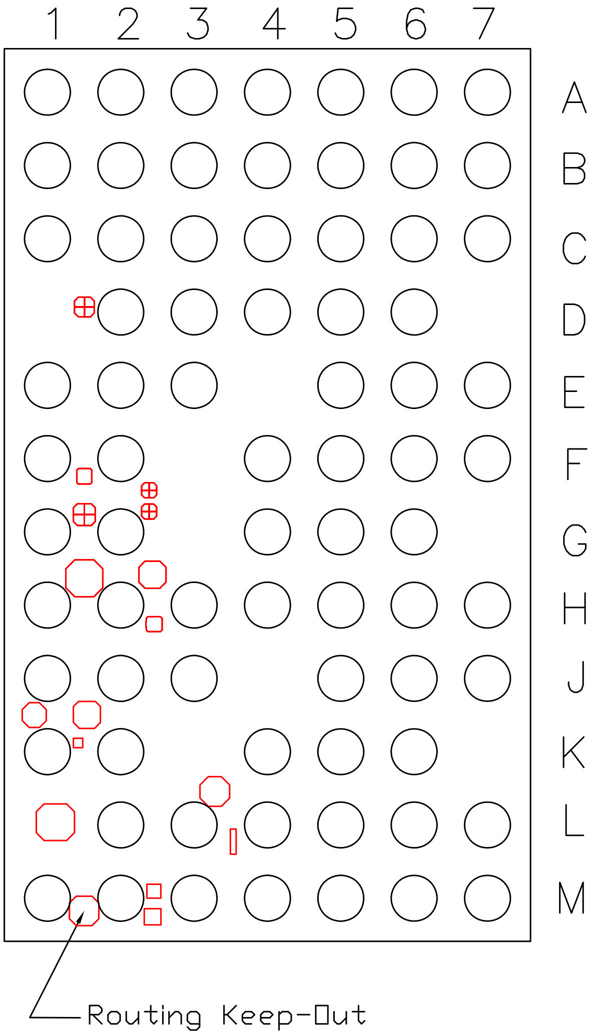
3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 22. WLBGA Package Keep-Out Areas—Top View with the Bumps Facing Down



17. Ordering Information

Part Number [a]	Package	Description	Operating Ambient Temperature
CYW43364KUBG	74-ball WLBGA halogen-free package (4.87 mm x 2.87 mm, 0.40 pitch)	2.4 GHz single-band WLAN IEEE 802.11n	–30°C to +70°C

[a] Add a “T” to the end of the part number to specify “Tape and Reel.”

18. Additional information

18.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

18.2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (https://community.cypress.com/).

Document History

Document Title: CYW43364 Single-Chip IEEE 802.11 b/g/n MAC/Baseband/Radio Document Number: 002-14781				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	12/08/2014	43364-DS100-R Initial release
*A	–	–	08/06/2015	43364-DS101-R **Updated:** ■ Figure 3: “Typical Power Topology (1 of 2),” on page 14. ■ Figure 4: “Typical Power Topology (2 of 2),” on page 15. ■ Figure 22: “74-Ball WLBGA Ball Map (Bottom View),” on page 44. ■ Table 7: “BCM43364 WLBGA Ball List — Ordered By Ball Number,” on page 45. ■ Table 8: “BCM43364 WLBGA Ball List — Ordered By Ball Name,” on page 48. ■ Table 9: “WLBGA Signal Descriptions,” on page 49. ■ Table 12: “I/O States,” on page 53. ■ Table 18: “WLAN 2.4 GHz Receiver Performance Specifications,” on page 59. ■ Table 19: “WLAN 2.4 GHz Transmitter Performance Specifications,” on page 62. ■ Table 25: “2.4 GHz Mode WLAN Power Consumption,” on page 70.
*B	–	–	10/05/2015	43364-DS102-R **Updated:** ■ Table 8, “WLBGA Signal Descriptions,” on page 28 ■ Table 11, “I/O States,” on page 31
*C	5525641	UTSV	11/18/2016	Added Cypress Part numbering Scheme. Updated to Cypress format
*D	5600251	SGUP	03/28/2017	Figure 3: “Typical Power Topology (1 of 2),” on page 7. Removed gSPI condition from the Features. Removed gSPI Mode from Table 5. Removed “4.2 Generic SPI Mode”, “4.2.1 SPI Protocol” and “13.3 gSPI Signal Timing”

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