AN203898

Getting Started with Traveo™ Family S6J3300 Series MCUs

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Associated Part Family: S6J3300 Series

Related Documents: For a complete list, click here.

AN203898 provides an overview of the development environment and tools for Traveo family S6J3300 series MCUs to help you get started with designing with the device family.

1 Introduction

AN203898 provides a summary of development environment and tools for the Traveo family S6J3300 series MCUs.

S6J3300 has an ARM® Cortex®-R5 CPU core with Secure Hardware Extension (SHE), CAN FD, memory, and analog and digital peripheral functions on a single chip. The product lineup of the S6J3300 series includes 208-pin, 176-pin, and 144-pin packages with different memory sizes. See the Technical Reference Manuals and Datasheet for details.

2 Development Environment and Tools

2.1 Evaluation Board

Cypress provides several evaluation boards to help you start using S6J3300 series MCUs. Two types of evaluation boards are available: 208-pin Evaluation Board and 176-pin Evaluation Board. Table 1 lists the part numbers of these evaluation boards.

Table 1. Traveo Family, S6J3300 Series MCU Evaluation Boards

Parts Number	Description
S6T3J200311A208A2	S6J3310 Series, 208-pin, Evaluation Board with secure hardware extension enabled (SHE=ON)
S6T3J200311A176A2	S6J3310 Series, 176-pin, Starter Kit with secure hardware extension enabled (SHE=ON)

2.2 Debugging Tools

Cypress recommends the third-party debugging tools listed in Table 2. For these tools, Cypress provides sample software (template project and sample driver). The template project includes I/O header files, startup settings, and several sample source files. The sample driver software includes source files for the peripheral features of the Traveo family S6J3300 series. Contact Cypress to obtain the sample software.

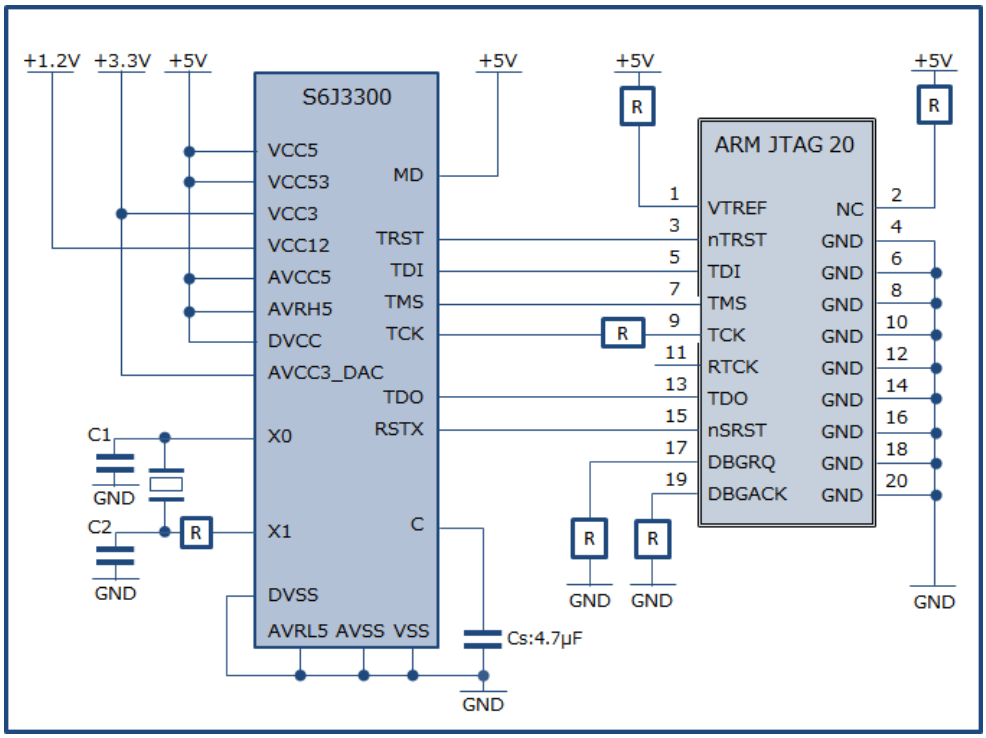
Table 2. Traveo Family, S6J3300 Series Debugging Tools

Vendor	Software (IDE)	Hardware (Debugging Tools)
Green Hills Software	MULTI (Ver. 6.1.4 or later version)	Green Hills Probe
IAR Systems	IAR Embedded Workbench (Ver. 7.30.4 or later version)	I-jet™

3 Basic Connection Diagram and Operation Mode

The Traveo family S6J3300 series MCUs have JTAG ports to connect with a debugging tool. Note that the JTAG nSRST port is not supported in this product series; therefore, you should connect the nSRST port to the RSTX port of this product if needed. In addition, TRST port should not be pulled up. For details, refer to KBA219205. Figure 1 shows the basic connection diagram for S6J3300.

Figure 1. S6J3300 Basic Connection Diagram with ARM JTAG 20



These devices have user mode and serial write modes. Figure 1 shows the user-mode connection. Serial write modes use P1_05 and P1_03 with the MD port. Table 3 lists the operation modes. This shows operation mode combination with MD port, P1_05, port and P1_03 port.

The Serial Write mode (Sync, Async) supports writing a user program to a flash memory in the MCU through a UART connection. The PC and the target MCU are connected via a serial cable. Cypress provides a PC software for programming the flash. Contact Cypress to use the flash program software.

In addition, the flash memory programmer provided by DTS INSIGHT (formerly known as YDC) supports S6J3300 series for writing a user program to the flash memory through a serial port.

Table 3. Operation Mode

Operation Mode	MD	P1_05	P1_03
User mode	1	--	--
Serial Write Mode (Sync)	0	1	0
Serial Write Mode (Async)	0	1	1

4 Related Documents

- Technical Reference Manuals
  - S6J3300 Series 32-bit Microcontroller Traveo™ Family Hardware Manual (Doc.No.002-10185)
  - Traveo Family Hardware Manual Platform Part (Doc.No.002-07884)
- Datasheet
  - S6J3310/S6J3320/S6J3330/S6J3340 Series 32-bit Microcontroller Traveo Family (Doc.No.002-10635)
- KBA
  - JTAG nTRST Pin Termination in Traveo™ S6J3110/3120/3200/3300/3350/3400 Series - KBA219205

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4983047	HIAR	10/23/2015	New application note.
*A	5717963	AESATP12	04/28/2017	Updated logo and copyright.
*B	5798291	HIAR	07/20/2017	Corrected the content of "2.1 Evaluation Board" Corrected the content of "4 Related Documents" Added a new content to "3 Basic Connection Diagram and Operation Mode"

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