Cypress Roadmap: Flash Memory

Q4 2015
### NOR Flash Memory Family Decoder

#### Technology:
- **J** = 110 nm Floating Gate
- **K** = 90 nm Floating Gate
- **L** = 65 nm Floating Gate
- **M** = 45 nm Floating Gate
- **N** = 110 nm MirrorBit
- **P** = 90 nm MirrorBit
- **R, S** = 65 nm MirrorBit
- **T** = 45 nm MirrorBit

#### Density:
- **001** = 1Mb
- **002** = 2Mb
- **004** = 4Mb
- **008** = 8Mb
- **016** = 16Mb
- **032** = 32Mb
- **064** = 64Mb
- **0128** = 128Mb
- **0256** = 256Mb
- **0512** = 512Mb
- **01024** = 1024Mb
- **004G** = 4Gb
- **008G** = 8Gb
- **0016G** = 16Gb
- **0032G** = 32Gb
- **0064G** = 64Gb
- **0128G** = 128Gb
- **0256G** = 256Gb
- **0512G** = 512Gb

#### Voltage:
- **D** = 2.5V
- **L** = 3.0V
- **S** = 1.8V

#### Family:
- **A** = Standard ADP (Address-Data Parallel)
- **C** = Burst Mode ADP (Address-Data Parallel)
- **F** = Quad SPI
- **G** = Page Mode
- **J** = Simultaneous Read/Write ADP (Address-Data Parallel)
- **K** = HyperBus
- **N** = Burst Mode Simultaneous Read/Write ADM (Address-Data Multiplexed)
- **P** = Page Mode Simultaneous Read/Write ADP (Address-Data Parallel)
- **V** = Burst Mode Simultaneous Read/Write ADM (Address-Data Multiplexed)
- **W** = Burst Mode Simultaneous Read/Write ADP (Address-Data Parallel)
- **X** = Burst Mode Simultaneous Read/Write AADM (Address-Address-Data Multiplexed)

#### Series:
- **25** = SPI
- **26** = HyperFlash
- **27** = HyperRAM
- **29** = NOR
- **70** = Stacked Die
- **79** = Dual Quad SPI

#### Prefix:
- **S**
## Parallel NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>Density</th>
<th>Initial / Page Access</th>
<th>* Temp Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>S29AS-J</td>
<td>110 nm, 1.8 V</td>
<td></td>
</tr>
<tr>
<td>S29AL-J</td>
<td>110 nm, 3.0 V</td>
<td></td>
</tr>
<tr>
<td>S29JL-J¹</td>
<td>110 nm, 3.0 V</td>
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</tr>
<tr>
<td>S29PL-J¹,²</td>
<td>110 nm, 3.0 V</td>
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</tr>
<tr>
<td>S29GL-N²</td>
<td>90 nm, 3.0 V</td>
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</tr>
<tr>
<td>S29GL-P²</td>
<td>65 nm, 3.0 V</td>
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</tr>
<tr>
<td>S29GL-S²</td>
<td>45 nm, 3.0 V</td>
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</tr>
</tbody>
</table>

### > 256 Mb

- **2Gb³**: 110 ns / 25 ns  
  - * I, A, V, B

- **1Gb**: 110 ns / 25 ns  
  - * I

- **512Mb**: 100 ns / 25 ns  
  - * I

- **256Mb**: 90 ns / 25 ns  
  - * I

### 64-128 Mb

- **128Mb**: 60 ns / 20 ns  
  - * I, A

- **64Mb**: 55 ns / 20 ns  
  - * I, A

- **64Mb**: 90 ns / 25 ns  
  - * I, A

- **64Mb**: 55 ns / --  
  - * I, A, N, M

- **32Mb**: 60 ns / --  
  - * I, A

- **32Mb**: 55 ns / 20 ns  
  - * I, A

- **32Mb**: 90 ns / 25 ns  
  - * I, A

### ≤ 32 Mb

- **16Mb**: 70 ns / --  
  - * I, A

- **16Mb**: 55 ns / --  
  - * I, A, N, M

- **8Mb**: 70 ns / --  
  - * I, A

- **8Mb**: 55 ns / --  
  - * I, A, N, M

### Status

- **Production**: QQYY
- **Sampling**: QQYY
- **Development**: QQYY
- **Concept**: QQYY

### Availability

- **EOL (Last-Time-Ship)**:

### Flash Memory Roadmap

- **Q116**
- **Q216**

### Notes

- **N** = Extended: -40°C to +125°C
- **M** = Extended, AEC-Q100: -40°C to +125°C
- **V** = Industrial-plus: -40°C to +105°C
- **B** = Industrial-plus, AEC-Q100: -40°C to +105°C
- **I** = Industrial: -40°C to +85°C
- **A** = Industrial, AEC-Q100: -40°C to +85°C
- **1** = Supports Simultaneous Read/Write Operation
- **2** = Supports Page Mode
- **3** = S70 series (stacked die)
### Burst NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th></th>
<th>S29WS-P&lt;sup&gt;1&lt;/sup&gt; 90 nm, 1.8 V</th>
<th>S29NS-P&lt;sup&gt;2&lt;/sup&gt; 90 nm, 1.8 V</th>
<th>S29VS-R&lt;sup&gt;2&lt;/sup&gt; 65 nm, 1.8 V</th>
<th>S29XS-R&lt;sup&gt;3&lt;/sup&gt; 65 nm, 1.8 V</th>
<th>S29CD-J&lt;sup&gt;1&lt;/sup&gt; 110 nm, 2.5 V</th>
<th>S29CL-J&lt;sup&gt;1&lt;/sup&gt; 110 nm, 3.0 V</th>
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</thead>
<tbody>
<tr>
<td><strong>Density</strong></td>
<td></td>
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</tr>
<tr>
<td>* W = Wireless: -25ºC to +85ºC</td>
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</tr>
<tr>
<td>I = Industrial: -40ºC to +85ºC</td>
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</tr>
<tr>
<td>A = Industrial, AEC-Q100: -40ºC to +85ºC</td>
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<tr>
<td>N = Extended: -40ºC to +125ºC</td>
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<tr>
<td>M = Extended, AEC-Q100: -40ºC to +125ºC</td>
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</tr>
<tr>
<td><strong>Initial Access / SDR Clock</strong></td>
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<tr>
<td>* Temp Range</td>
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<tr>
<td>512Mb 80 ns / 104 MHz</td>
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<tr>
<td>256Mb 80 ns / 104 MHz</td>
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<td>64Mb 80 ns / 108 MHz</td>
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<tr>
<td>32Mb 54 ns / 75 MHz</td>
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<tr>
<td>16Mb 54 ns / 66 MHz</td>
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</table>

**Status**
- Production: QQQY
- Sampling: QQQY
- Development: 
- Concept: 

**Availability**
- EOL (Last-Time-Ship): QQQY

**Temperature Ranges**
- H = Hot: -40ºC to +145ºC
- T = Hot, AEC-Q100: -40ºC to +145ºC
- ADP (Address Data Parallel) Burst
- ADM (Address Data Multiplex) Burst
- AADM (Address high, Address low, Data Multiplex) Burst
### SPI NOR Flash Memory Portfolio

<table>
<thead>
<tr>
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<td>65 nm, 3.0 V</td>
<td>90 nm, 3.0 V</td>
<td>65 nm, 3.0 V</td>
<td>65 nm, 3.0 V</td>
<td>65 nm, 1.8 V</td>
</tr>
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<td>4KB²</td>
<td>4KB²</td>
<td>&gt;4KB²</td>
<td>&gt;4KB²</td>
<td>&gt;4KB²</td>
<td>&gt;4KB²</td>
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</table>

#### Density
- SDR Clock / DDR Clock
- * Temp Range

<table>
<thead>
<tr>
<th>256Mb</th>
<th>512Mb</th>
<th>1Gb³</th>
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</table>

<table>
<thead>
<tr>
<th>128Mb⁴</th>
<th>256Mb⁵</th>
<th>512Mb⁶</th>
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</table>

<table>
<thead>
<tr>
<th>64Mb⁷</th>
<th>128Mb⁸</th>
<th>256Mb⁹</th>
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</thead>
</table>

<table>
<thead>
<tr>
<th>16Mb</th>
<th>32Mb</th>
<th>64Mb</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>8Mb</th>
<th>16Mb</th>
<th>32Mb</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>4Mb</th>
<th>8Mb</th>
<th>16Mb</th>
</tr>
</thead>
</table>

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1. S25FL2-K Dual SPI
2. Logical sector size
3. S79 series, Dual Quad SPI (stacked die)
4. Contact Sales
5. S70 series (stacked die)
6. S25FL129P Quad SPI
7. S25FL128P Dual SPI
8. S25FL128S 133-MHz SDR / 80-MHz DDR
9. S25FL127S 108-MHz SDR

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*I = Industrial: -40°C to +85°C
A = Industrial, AEC-Q100: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
B = Industrial-plus, AEC-Q100: -40°C to +105°C
N = Extended: -40°C to +125°C
M = Extended, AEC-Q100: -40°C to +125°C

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Flash Memory Roadmap
# HyperFlash and HyperRAM Portfolio

<table>
<thead>
<tr>
<th>HyperFlash</th>
<th>HyperFlash</th>
<th>HyperRAM</th>
<th>HyperRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S26KS-S</strong>&lt;sup&gt;1&lt;/sup&gt;</td>
<td><strong>S26KL-S</strong>&lt;sup&gt;1&lt;/sup&gt;</td>
<td><strong>S27KS-1</strong>&lt;sup&gt;2&lt;/sup&gt;</td>
<td><strong>S27KL-1</strong>&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>65 nm, 1.8 V</td>
<td>65 nm, 3.0 V</td>
<td>63 nm, 1.8 V</td>
<td>63 nm, 3.0 V</td>
</tr>
</tbody>
</table>

## Density
- Initial Access / DDR Clock
- *Temp Range

### 256Mb
- **1Gb**<sup>3</sup>
  - 96 ns / 166 MHz
  - *I, A, V, B, N, M

### 64-128Mb
- **128Mb**
  - 96 ns / 166 MHz
  - *I, A, V, B, N<sup>4</sup>, M<sup>4</sup>

### ≥256Mb
- **512Mb**
  - 96 ns / 166 MHz
  - *I, A, V, B, N<sup>4</sup>, M<sup>4</sup>

### 64Mb
- **64Mb**
  - 36 ns / 166 MHz
  - *I, A, V, B

## Status
- **EOL (Last-Time-Shirt)**
- **Production**
- **Sampling**
- **Development**
- **Concept**

### Availability
- **QQYY**

## Notes
- **C** = Commercial: -0°C to +70°C
- **I** = Industrial: -40°C to +85°C
- **A** = Industrial, AEC-Q100: -40°C to +85°C
- **V** = Industrial-plus: -40°C to +105°C
- **B** = Industrial-plus, AEC-Q100: -40°C to +105°C
- **N** = Extended: -40°C to +125°C
- **M** = Extended, AEC-Q100: -40°C to +125°C

1 S26 = HyperFlash
2 S27 = HyperRAM
3 S70 series (stacked die)
4 Contact sales
NAND and e.MMC Family Decoder

**NAND**

- **Technology:** 1 = 4x nm, 2 = 32 nm
- **Density:** 01G = 1Gb, 02G = 2Gb, 04G = 4Gb, 08G = 8Gb, 0AG = 16Gb, 0BG = 32Gb
- **Voltage:** L = 3.0V, S = 1.8V
- **Family:** M = NAND (Address-Data Multiplexed)
- **Series:** 34 = NAND
- **Prefix:** S

**e.MMC**

- **Controller:** B1 = e.MMC 4.51, B2 = e.MMC 5.1
- **Revision:** 1 = NAND MLC\(^1\) 1x nm, 2 = NAND MLC\(^1\) 1y nm
- **Density:** 004 = 4GB, 008 = 8GB, 016 = 16GB, 032 = 32GB, 064 = 64GB, 128 = 128GB
- **Controller Architecture:** 41 = e.MMC
- **Series:** 40 = Managed Memory
- **Prefix:** S

\(^1\) Multi-level cell
# SLC NAND and e.MMC Portfolio

<table>
<thead>
<tr>
<th>Density; Bus Width</th>
<th>Interface Bandwidth</th>
<th>* Temp Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>8Gb-16Gb</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8Gb; x8</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>4Gb; x8/16</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>2Gb; x8/16</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>1Gb; x8</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>16Gb; x8</td>
<td>40 MBps</td>
<td>* I</td>
</tr>
<tr>
<td>8Gb; x8</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>4Gb; x8</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>2Gb; x8/16</td>
<td>40 MBps</td>
<td>* I</td>
</tr>
<tr>
<td>1Gb; x8/16</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>8Gb; x8</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>4Gb; x8/16</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>2Gb; x8</td>
<td>40 MBps</td>
<td>* I</td>
</tr>
<tr>
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<td>8Gb; x8</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
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<tr>
<td>4Gb; x8/16</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
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<tr>
<td>2Gb; x8</td>
<td>40 MBps</td>
<td>* I</td>
</tr>
<tr>
<td>1Gb; x8/16</td>
<td>40 MBps</td>
<td>* I, A, V, B</td>
</tr>
</tbody>
</table>

- W = Embedded: -25°C to +85°C
- I = Industrial: -40°C to +85°C
- A = Industrial, AEC-Q100: -40°C to +105°C
- V = Industrial-plus: -40°C to +105°C
- B = Industrial-plus, AEC-Q100: -40°C to +105°C

- 1-bit ECC
- 2-bit ECC
- Secure NAND
- ONFI = Open NAND Flash Interface
- e.MMC = Embedded Multi Media Card
- Contact sales

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**Flash Memory Roadmap**

<table>
<thead>
<tr>
<th>S4041-1B1</th>
<th>S4041-2B2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1x nm, 3.0 V</td>
<td>1y nm, 3.0 V</td>
</tr>
<tr>
<td>MLC, e.MMC 4.5</td>
<td>MLC, e.MMC 5.1</td>
</tr>
</tbody>
</table>

**Availability**
- Production
- Sampling
- Development
- Concept

**EOL (Last-Time-Ship)**

- 64GB; x8
  - 400 MBps
  - * W, I, A
- 32GB; x8
  - 400 MBps
  - * W, I, A
- 16GB; x8
  - 200 MBps
  - * W, I
- 8GB; x8
  - 400 MBps
  - * W, I, A
- 8Gb; x8
  - 400 MBps
  - * W, I, A
- 16Gb; x8
  - 200 MBps
  - * W, I
- 8Gb; x8
  - 400 MBps
  - * W, I, A
- 16Gb; x8
  - 200 MBps
  - * W, I
## Parallel NOR Flash Memory Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>Device</th>
<th>48-ball FBGA (0.8-mm pitch)</th>
<th>48-ball FBGA (0.5-mm pitch)</th>
<th>56-ball BGA (0.8-mm pitch)</th>
<th>64-ball BGA (0.8-mm pitch)</th>
<th>64-ball Fortified BGA (1.0-mm pitch)</th>
<th>48-pin TSOP</th>
<th>56-pin TSOP</th>
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**CF** = Contact Factory  
**UD** = Under Development
# HyperFlash and HyperRAM Packages

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*CF = Contact Factory*
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Cypress 3-V 64Mb (S29GL064S) Parallel Page Mode NOR Flash Memory

**Applications**
- Advanced driver assistance system (ADAS)
- Automotive instrument cluster
- Automotive infotainment
- Communication equipment
- Industrial automation

**Features**
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- Initial access time: 70 ns
- Page access time: 15 ns
- Program\(^1\) time (256B): 0.4 ms (typical)
- Sector Erase\(^2\) time (64KB): 300 ms (typical)
- Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
- Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
- Extended temp range (AEC-Q100 opt.): -40°C to +125°C
- Packages: 48-pin TSOP 12 mm x 20 mm, 56-pin TSOP 14 mm x 20 mm, 64-ball Fortified\(^4\) BGA 9 mm x 9 mm, 64-ball Fortified\(^4\) BGA 13 mm x 11 mm, 48-ball BGA\(^5\) 8.15 mm x 6.15 mm

**Collateral**
- Datasheet: S29GL064S

**Availability**
- Sampling: Now
- Production: Now

---

1. The operation required to change a value “1” to a value “0” in NOR Flash Memory
2. The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming data such as boot code or parametric data
3. The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4. Fortified BGA supports a 1-mm ball pitch
5. BGA supports a 0.8-mm ball pitch
6. Write Protect input
7. Ready/Busy output
8. An input that selects the data bus width of either 8 bits or 16 bits
Cypress 3-V 128Mb (S29GL128S) Parallel Page Mode NOR Flash Memory

Applications
Advanced driver assistance system (ADAS)
Automotive instrument cluster
Automotive infotainment
Communication equipment
Industrial automation

Features
Operating voltage range: 2.7 V to 3.6 V
100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles
20-year data retention at +55°C
Initial access time: 90 ns
Page access time: 15 ns
Program\(^1\) time (512B): 0.34 ms (typical)
Sector Erase\(^2\) time (128KB): 275 ms (typical)
Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
Packages: 56-pin TSOP 14 mm x 20 mm, 64-ball Fortified\(^4\)
BGA 9 mm x 9 mm, 64-ball Fortified\(^4\) BGA 13 mm x 11 mm,
56-ball BGA\(^5\) 9 mm x 7 mm

Collateral
Datasheet: S29GL128S

Availability
Sampling: Now
Production: Now

---

1. The operation required to change a value “1” to a value “0” in NOR Flash Memory
2. The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming data such as boot code or parametric data
3. The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4. Fortified BGA supports a 1-mm ball pitch
5. BGA supports a 0.8-mm ball pitch
6. Write Protect input
7. Ready/Busy output
Cypress 3-V 256Mb (S29GL256S) Parallel Page Mode NOR Flash Memory

Applications
- Advanced driver assistance system (ADAS)
- Automotive instrument cluster
- Automotive infotainment
- Communication equipment
- Industrial automation

Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- Initial access time: 90 ns
- Page access time: 15 ns
- Program\(^1\) time (512B): 0.34 ms (typical)
- Sector Erase\(^2\) time (128KB): 275 ms (typical)
- Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
- Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
- Packages: 56-pin TSOP 14 mm x 20 mm, 64-ball Fortified\(^4\)
- BGA 9 mm x 9 mm, 64-ball Fortified\(^4\)
- BGA 13 mm x 11 mm, 56-ball BGA\(^5\) 9 mm x 7 mm

Collateral
- Datasheet: S29GL256S

Availability
- Sampling: Now
- Production: Now

1 The operation required to change a value “1” to a value “0” in NOR Flash Memory
2 The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming data such as boot code or parametric data
3 The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4 Fortified BGA supports a 1-mm ball pitch
5 BGA supports a 0.8-mm ball pitch
6 Write Protect input
7 Ready/Busy output
Cypress 3-V 512Mb (S29GL512S) Parallel Page Mode NOR Flash Memory

**Applications**
Advanced driver assistance system (ADAS)
Automotive instrument cluster
Automotive infotainment
Communication equipment
Industrial automation

**Features**
Operating voltage range: 2.7 V to 3.6 V
100,000 Program¹/Sector Erase² endurance cycles³
20-year data retention at +55°C
Initial access time: 100 ns
Page access time: 15 ns
Program¹ time (512B): 0.34 ms (typical)
Sector Erase² time (128KB): 275 ms (typical)
Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
Packages: 56-pin TSOP 14 mm x 20 mm, 64-ball Fortified⁴
BGA 9 mm x 9 mm, 64-ball Fortified⁴ BGA 13 mm x 11 mm,
56-ball BGA⁵ 9 mm x 7 mm

**Collateral**
Datasheet: S29GL512S

**Availability**
Sampling: Now
Production: Now

---
¹ The operation required to change a value “1” to a value “0” in NOR Flash Memory
² The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming data such as boot code or parametric data
³ The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
⁴ Fortified BGA supports a 1-mm ball pitch
⁵ BGA supports a 0.8-mm ball pitch
⁶ Write Protect input
⁷ Ready/Busy output
Cypress 3-V 1Gb (S29GL01GS) Parallel Page Mode NOR Flash Memory

Applications
Advanced driver assistance system (ADAS)
Automotive instrument cluster
Automotive infotainment
Communication equipment
Industrial automation

Features
Operating voltage range: 2.7 V to 3.6 V
100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
20-year data retention at +55°C
Initial access time: 100 ns
Page access time: 15 ns
Program\(^1\) time (512B): 0.34 ms (typical)
Sector Erase\(^2\) time (128KB): 275 ms (typical)
Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
Packages: TSOP 14 mm x 20 mm, 64-ball Fortified\(^4\) BGA
9 mm x 9 mm, 64-ball Fortified\(^4\) BGA 13 mm x 11 mm

Collateral
Datasheet: S29GL01GS

Availability
Sampling: Now
Production: Now

1 The operation required to change a value “1” to a value “0” in NOR Flash Memory
2 The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming data such as boot code or parametric data
3 The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4 Fortified BGA supports a 1-mm ball pitch
5 Write Protect input
6 Ready/Busy output
Cypress 3-V 2Gb (S70GL02GS) Parallel Page Mode NOR Flash Memory

Applications
- Advanced driver assistance system (ADAS)
- Automotive instrument cluster
- Automotive infotainment
- Communication equipment
- Industrial automation

Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- Initial access time: 100 ns
- Page access time: 15 ns
- Program\(^1\) time (512B): 0.34 ms (typical)
- Sector Erase\(^2\) time (128KB): 275 ms (typical)
- Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
- Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
- Packages: 64-ball Fortified\(^4\) BGA 13 mm x 11 mm

Collateral
Datasheet: S70GL02GS

Availability
- Sampling: Now
- Production: Now

1 The operation required to change a value “1” to a value “0” in NOR Flash Memory
2 The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming data such as boot code or parametric data
3 The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4 Fortified BGA supports a 1-mm ball pitch
5 Write Protect input
6 Ready/Busy output
Cypress 3-V 128Mb (S25FL127S) Quad SPI NOR Flash Memory

Applications
Printers
Networking devices
Set-top boxes

Features
Operating voltage range: 2.7 V to 3.6 V
100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
20-year data retention at +55°C
SDR\(^4\) clock rate: 108-MHz QIO\(^5\)
Program\(^1\) time (256B): 0.395 ms (typical)
Sector Erase\(^2\) time (64KB): 130 ms (typical)
Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
Packages: 8-SOIC 208 mil, 16-SOIC 300 mil, 8-WSON\(^6\)
6 mm x 5 mm, 24-ball BGA 6 mm x 8 mm

Collateral
Datasheet: S25FL127S
Download App Note: Cypress FL-S SPI NOR Flash Memory

Availability
Sampling: Now
Production: Now

---

1 The operation required to change a value “1” to a value “0” in NOR Flash Memory
2 The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
3 The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4 Single data rate: A mode of data transfer in which data is transferred once per clock cycle
5 Quad input/output (QIO): An interface that transfers addresses or data on four I/O’s simultaneously
6 Very, Very Thin, Small-Outline, No-Lead semiconductor package
7 Signals used for standard Quad (x4) SPI interface. Refer to the S25FL127S datasheet for signal definitions in the x1 and x2 mode.
8 RESET# is an optional signal available on 16-SOIC and BGA packages.
9 Read data buffer
Cypress 3-V 128Mb (S25FL128S) Quad SPI NOR Flash Memory

Applications
- Advanced driver assistance systems (ADAS)
- Automotive instrument clusters
- Automotive infotainment systems
- White goods
- Set-top boxes

Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- SDR\(^4\) clock rate: 104-MHz QIO\(^5\)
- DDR\(^6\) clock rate: 80-MHz QIO\(^5\)
- Program\(^1\) time (256B): 0.250 ms (typical)
- Sector Erase\(^2\) time (64KB): 130 ms (typical)
- Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
- Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
- Extended temp range (AEC-Q100 opt.): -40°C to +125°C
- Packages: 16-SOIC 300 mil, 8-WSON\(^7\) 6 mm x 8 mm, 24-ball BGA 6 mm x 8 mm

Collateral
- Datasheet: S25FL128S
- Download App Note: Cypress FL-S SPI NOR Flash Memory

Availability
- Sampling: Now
- Production: Now

Notes:
1. The operation required to change a value “1” to a value “0” in NOR Flash Memory
2. The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
3. The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4. Single data rate: A mode of data transfer in which data is transferred once per clock cycle
5. Quad input/output (QIO): An interface that transfers addresses or data on four I/O’s simultaneously
6. Double data rate: A mode of data transfer in which data is transferred twice per clock cycle
7. A thin, small-outline, no-lead semiconductor package
8. Signals used for standard Quad (x4) SPI interface. Refer to the S25FL128S datasheet for signal definitions in the x1 and x2 mode.
9. RESET# is an optional signal available on 16-SOIC and BGA packages.
10. Read data buffer
**Cypress 3-V 256Mb (S25FL256S) Quad SPI NOR Flash Memory**

### Applications
- Advanced driver assistance systems (ADAS)
- Automotive instrument clusters
- Automotive infotainment systems
- Networking devices
- Set-top boxes

### Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- SDR\(^4\) clock rate: 104-MHz QIO\(^5\)
- DDR\(^6\) clock rate: 80-MHz QIO\(^5\)
- Program\(^1\) time (256B): 0.25 ms (typical)
- Sector Erase\(^2\) time (64KB): 130 ms (typical)
- Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
- Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
- Extended temp range (AEC-Q100 opt.): -40°C to +125°C
- Packages: 16-SOIC 300 mil, 8-WSON\(^7\) 6 mm x 8 mm, 24-ball BGA 6 mm x 8 mm

### Collateral
- Datasheet: [S25FL256S](#)
- Download App Note: [Cypress FL-S SPI NOR Flash Memory](#)

### Availability
- Sampling: Now
- Production: Now

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\(^1\) The operation required to change a value “1” to a value “0” in NOR Flash Memory
\(^2\) The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
\(^3\) The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
\(^4\) Single data rate: A mode of data transfer in which data is transferred once per clock cycle
\(^5\) Quad input/output (QIO): An interface that transfers addresses or data on four I/Os simultaneously
\(^6\) Double data rate: A mode of data transfer in which data is transferred twice per clock cycle
\(^7\) Very, Very Thin, Small-Outline, No-Lead semiconductor package
\(^8\) Signals used for standard Quad (x4) SPI interface; refer to the [S25FL256S](#) datasheet for signal definitions in the x1 and x2 mode
\(^9\) RESET# is an optional signal available on 16-SOIC and BGA packages
\(^10\) Read data buffer
Cypress 3-V 512Mb (S25FL512S) Quad SPI NOR Flash Memory

Applications

Advanced driver assistance systems (ADAS)
Automotive instrument clusters
Automotive infotainment systems
Base stations
Set-top boxes

Features

Operating voltage range: 2.7 V to 3.6 V
100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
20-year data retention at +55°C
SDR\(^4\) clock rate: 104-MHz QIO\(^5\)
DDR\(^6\) clock rate: 80-MHz QIO\(^5\)
Program\(^1\) time (512B): 0.340 ms (typical)
Sector Erase\(^2\) time (256KB): 520 ms (typical)
Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
Packages: 16-SOIC 300 mil, 24-ball BGA 6 mm x 8 mm

Collateral

Datasheet: S25FL512S
Download App Note: Cypress FL-S SPI NOR Flash Memory

Availability

Sampling: Now
Production: Now

1 The operation required to change a value “1” to a value “0” in NOR Flash Memory
2 The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
3 The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4 Single data rate: A mode of data transfer in which data is transferred once per clock cycle
5 Quad input/output (QIO): An interface that transfers addresses or data on four I/O’s simultaneously
6 Double data rate: A mode of data transfer in which data is transferred twice per clock cycle
7 Signals used for standard Quad (x4) SPI interface. Refer to the S25FL512S datasheet for signal definitions in the x1 and x2 mode.
8 RESET# is an optional signal available on 16-SOIC and BGA packages.
9 Read data buffer
Cypress 3-V 1Gb (S70FL01GS) Quad SPI NOR Flash Memory

Applications
- Advanced driver assistance systems (ADAS)
- Automotive instrument clusters
- Automotive infotainment systems
- Base stations
- Industrial controllers

Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- SDR\(^4\) clock rate: 104-MHz QIO\(^5\)
- DDR\(^6\) clock rate: 80-MHz QIO\(^5\)
- Program\(^1\) time (512B): 0.340 ms (typical)
- Sector Erase\(^2\) time (256KB): 520 ms (typical)
- Industrial temp range (AEC-Q100 opt.): -40°C to +85°C
- Industrial plus temp range (AEC-Q100 opt.): -40°C to +105°C
- Packages: 16-SOIC 300 mil, 24-ball BGA 6 mm x 8 mm

Datasheet: S70FL01GS
Download App Note: Cypress FL-S SPI NOR Flash Memory

Collateral

Availability
- Sampling: Now
- Production: Now

1 The operation required to change a value “1” to a value “0” in NOR Flash Memory
2 The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
3 The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4 Single data rate: A mode of data transfer in which data is transferred once per clock cycle
5 Quad input/output (QIO): An interface that transfers addresses or data on four I/O’s simultaneously
6 Double data rate: A mode of data transfer in which data is transferred twice per clock cycle
7 Signals used for standard Quad (x4) SPI interface. Refer to the S70FL01GS datasheet for signal definitions in the x1 and x2 mode.
8 RESET# is an optional signal available on 16-SOIC and BGA packages.
9 Read data buffer
Cypress 1.8-V 128Mb (S25FS128S) Quad SPI NOR Flash Memory

**Applications**
- Automotive instrument clusters
- Wearable electronics
- Industrial controls
- Home automation
- Digital single-lens reflex (DSLR) cameras

**Features**
- Operating voltage range: 1.7 V to 2.0 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- SDR\(^4\) clock rate: 133-MHz QIO\(^5\)
- DDR\(^6\) clock rate: 80-MHz QIO\(^5\)
- Program\(^1\) time (256B): 0.36 ms (typical)
- Sector Erase\(^2\) time (64KB): 240 ms (typical)
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Packages: 8-SOIC 208 mil, 8-WSON\(^7\) 5 mm x 6 mm, 24-ball BGA 6 mm x 8 mm

**Availability**
- Sampling: Now
- Production: Now

**Datasheet**
- S25FS128S

**App Notes**
- Cypress FS-S SPI NOR Flash Memory

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1 The operation required to change a value “1” to a value “0” in NOR Flash Memory
2 The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
3 The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4 Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
5 Quad input/output: An interface that transfers addresses or data on four I/Os simultaneously
6 Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
7 Very, Very Thin, Small-Outline, No-Lead semiconductor package
8 Signals used for standard Quad (x4) SPI interface. Refer to the S25FS128S datasheet for signal definitions in the x1 and x2 mode.
9 Read data buffer
Cypress 1.8-V 256Mb (S25FS256S) Quad SPI NOR Flash Memory

Applications
- Wearable electronics
- Advanced driver assistance systems (ADAS)
- Portable communications, Wireless LAN
- Blade server
- Road tolling system

Features
- Operating voltage range: 1.7 V to 2.0 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- SDR\(^4\) clock rate: 133-MHz QIO\(^5\)
- DDR\(^6\) clock rate: 80-MHz QIO\(^5\)
- Program\(^1\) time (256B): 0.360 ms (typical)
- Sector Erase\(^2\) time (64KB): 240 ms (typical)
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Packages: 16-SOIC 300 mil, 8-WSON\(^7\) 6 mm x 8 mm, 24-ball BGA 6 mm x 8 mm

Datasheet: S25FS256S
App Notes: Cypress FS-S SPI NOR Flash Memory

Availability
- Sampling: Now
- Production: Now

Notes:
1. The operation required to change a value “1” to a value “0” in NOR Flash Memory
2. The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
3. The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4. Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
5. Quad input/output: An interface that transfers addresses or data on four I/Os simultaneously
6. Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
7. Very, Very Thin, Small-Outline, No-Lead semiconductor package
8. Signals used for standard Quad (x4) SPI interface; refer to the S25FS256S datasheet for signal definitions in the x1 and x2 mode
9. Read data buffer
Cypress 1.8-V 512Mb (S25FS512S) Quad SPI NOR Flash Memory

### Applications
- Wearable electronics
- Automotive telematics/infotainment
- Advanced driver assistance systems (ADAS)
- Networking/communications, e.g., base station, WiFi, LTE (Long Term Evolution)

### Features
- Operating voltage range: 1.7 V to 2.0 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- SDR\(^4\) clock rate: 133-MHz QIO\(^5\)
- DDR\(^6\) clock rate: 80-MHz QIO\(^5\)
- Program\(^1\) time (512B): 0.360 ms (typical)
- Sector Erase\(^2\) time (256KB): 930 ms (typical)
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Packages: 16-SOIC 300 mil, 8-WSON\(^7\) 6 mm x 8 mm, 24-ball BGA 6 mm x 8 mm

### Collateral
- Datasheet: [S25FS512S](#)
- App Notes: [Cypress FS-S SPI NOR Flash Memory](#)

### Availability
- Sampling: Now
- Production: Now

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1. The operation required to change a value "1" to a value "0" in NOR Flash Memory
2. The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value "1"
3. The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4. Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
5. Quad input/output: An interface that transfers addresses or data on four I/Os simultaneously
6. Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
7. Very, Very Thin, Small-Outline, No-Lead semiconductor package
8. Signals used for standard Quad (x4) SPI interface. Refer to the [S25FS512S](#) datasheet for signal definitions in the x1 and x2 mode.
9. Read data buffer
Cypress 1.8-V 1Gb (S70FS01GS) Quad SPI NOR Flash Memory

Applications
- Base stations
- Home gateways
- Automotive telematics
- Wireless LAN

Features
- Operating voltage range: 1.7 V to 2.0 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- SDR\(^4\) clock rate: 133-MHz QIO\(^5\)
- DDR\(^6\) clock rate: 80-MHz QIO\(^5\)
- Program\(^1\) time (512B): 0.340 ms (typical)
- Sector Erase\(^2\) time (256KB): 520 ms (typical)
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Packages: 16-SOIC 300 mil, 24-ball BGA 6 mm × 8 mm

Collateral
- Datasheet: [Contact Sales](#)
- App Notes: [Cypress FS-S SPI NOR Flash Memory](#)

Availability
- Sampling: Now
- Production: Q4 2015

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\(^1\) The operation required to change a value “1” to a value “0” in NOR Flash Memory
\(^2\) The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
\(^3\) The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
\(^4\) Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
\(^5\) Quad input/output: An interface that transfers addresses or data on four I/Os simultaneously
\(^6\) Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
\(^7\) Signals used for standard Quad (x4) SPI interface
\(^8\) Read data buffer
Cypress 3-V 64Mb (S25FL064L) Quad SPI NOR Flash Memory

Applications
Set-top boxes
Printers
White goods
Smart meters
Automotive instrument clusters and infotainment systems

Features
Operating voltage range: 2.7 V to 3.6 V
100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
20-year data retention at +55°C
SDR\(^4\) clock rate: 108-MHz QIO\(^5\)
DDR\(^6\) clock rate: N/A
Program\(^1\) time (256B): 0.70 ms (typical)
Sector Erase\(^2\) time (64KB): 400 ms (typical)
Industrial temp range (AEC-Q100 optional): -40°C to +85°C
Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
Extended temp range (AEC-Q100 optional): -40°C to +125°C
Packages: 8-SOIC 208 mil, 8-WSON\(^7\) 4 mm x 4 mm or 5 mm x 6 mm, 24-ball BGA 6 mm x 8 mm

Collateral
Datasheet: S25FL064L
App Notes: Cypress FL-L SPI NOR Flash Memory

Availability
Sampling: Q3 2016
Production: Q1 2017

1 The operation required to change a value “1” to a value “0” in NOR Flash memory
2 The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
3 The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4 Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
5 Quad input/output (QIO): An interface that transfers addresses or data on four I/O’s simultaneously
6 Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
7 Very, Very Thin, Small-Outline, No-Lead semiconductor package
8 Signals used for standard Quad (x4) SPI interface.
9 RESET# is an optional signal available on 16-SOIC and BGA packages.
10 Read data buffer
Cypress 3-V 128Mb (S25FL128L) Quad SPI NOR Flash Memory

### Applications
- Video game consoles
- Advanced driver assistance systems (ADAS)
- Automotive instrument clusters and infotainment systems
- White goods
- Set-top boxes

### Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\)
- 20-year data retention at +55°C
- SDR\(^4\) clock rate: 133-MHz QIO\(^5\)
- DDR\(^6\) clock rate: 66-MHz QIO\(^5\)
- Program\(^1\) time (256B): 0.30 ms (typical)
- Sector Erase\(^2\) time (64KB): 270 ms (typical)
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Extended temp range (AEC-Q100 optional): -40°C to +125°C
- Packages: 16-SOIC 300 mil, 8-WSON\(^7\) 5 mm x 6 mm, 24-ball BGA 6 mm x 8 mm

### Collateral
- Datasheet: [S25FL128L](#)
- App Notes: Cypress FL-L SPI NOR Flash Memory

### Availability
- Sampling: Q1 2016
- Production: Q2 2016

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1. The operation required to change a value “1” to a value “0” in NOR Flash memory
2. The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
3. The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4. Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
5. Quad input/output (QIO): An interface that transfers addresses or data on four I/O’s simultaneously
6. Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
7. Very, Very Thin, Small-Outline, No-Lead semiconductor package
8. Signals used for standard Quad (x4) SPI interface. Refer to the [S25FL128L](#) datasheet for signal definitions in the x1 and x2 mode.
9. RESET# is an optional signal available on 16-SOIC and BGA packages.
10. Read data buffer
Cypress 3-V 256Mb (S25FL256L) Quad SPI NOR Flash Memory

Applications
- Video game consoles
- Advanced driver assistance systems (ADAS)
- Automotive instrument clusters and infotainment systems
- Networking devices
- Set-top boxes

Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program1/Sector Erase2 endurance cycles3
- 20-year data retention at +55°C (typical)
- SDR4 clock rate: 133-MHz QIO5
- DDR6 clock rate: 66-MHz QIO5
- Program1 time (256B): 0.30 ms (typical)
- Sector Erase2 time (64KB): 270 ms (typical)
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Extended temp range (AEC-Q100 optional): -40°C to +125°C
- Packages: 16-SOIC 300 mil, 8-WSON7 6 mm x 8 mm, 24-ball BGA 6 mm x 8 mm

Collateral
- Datasheet: S25FL256L
- App Notes: Cypress FL-L SPI NOR Flash Memory

Availability
- Sampling: Q1 2016
- Production: Q1 2016

1 The operation required to change a value “1” to a value “0” in NOR Flash memory
2 The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value “1”
3 The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
4 Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
5 Quad input/output (QIO): An interface that transfers addresses or data on four I/Os simultaneously
6 Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
7 Very, Very Thin, Small-Outline, No-Lead semiconductor package
8 Signals used for standard Quad (x4) SPI interface; refer to the S25FL256L datasheet for signal definitions in the x1 and x2 mode
9 RESET# is an optional signal available on 16-SOIC and BGA packages
10 Read data buffer
Cypress 1.8-V 128Mb (S26KS128S) HyperFlash Memory

**Applications**
- Automotive instrument cluster
- Automotive infotainment
- Communication equipment
- Highest-performance consumer products

**Features**
- Operating voltage range: 1.70 V to 1.95 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\) (min)
- 20-year data retention at +55°C (typical)
- Initial access time: 96 ns\(^4\)
- Clock rate: 166 MHz with 333 MBps Read Bandwidth
- Program\(^1\) time (512B): 475 μs (typical)
- Sector Erase\(^2\) time (256KB): 930 ms (typical)
- On-Chip ECC: Single-bit Soft Error\(^5\) correction
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Extended temp range\(^6\) (AEC-Q100 optional): -40°C to +125°C
- Package: 24-ball BGA\(^7\) 6 mm x 8 mm

**Collateral**
- Datasheet: [S26KS128S](#)

**Availability**
- Sampling: Now
- Production: Now

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1. The operation required to change a value "1" to a value "0" in NOR Flash Memory
2. The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming
3. The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4. Following the initial read access time, a byte of data is transferred on each clock edge. At 166 MHz, the continuous data rate is 333 MBps
5. A data error caused by background radiation
6. Endurance for devices supporting extended temperature range is 10,000 cycles min
7. Ball Grid Array (BGA) supports a 1-mm ball pitch
8. Read Write Data Strobe I/O
9. Hardware reset; not a mandatory signal for data transaction
10. Interrupt output; not a mandatory signal for data transaction
11. Reset output; not a mandatory signal for data transaction
Cypress 1.8-V 256Mb (S26KS256S) HyperFlash Memory

### Applications
- Automotive instrument cluster
- Automotive infotainment
- Communication equipment
- Highest-performance consumer products

### Features
- Operating voltage range: 1.70 V to 1.95 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\) (min)
- 20-year data retention at +55°C (typical)
- Initial access time: 96 ns\(^4\)
- Clock rate: 166 MHz with 333 MBps Read Bandwidth
- Program\(^1\) time (512B): 475 µs (typical)
- Sector Erase\(^2\) time (256KB): 930 ms (typical)
- On-Chip ECC: Single-bit Soft Error\(^5\) correction
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Extended temp range\(^6\) (AEC-Q100 optional): -40°C to +125°C
- Package: 24-ball BGA\(^7\) 6 mm x 8 mm

### Collateral
- Datasheet: [S26KS256S](#)

### Availability
- Sampling: Now
- Production: Now

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1. The operation required to change a value “1” to a value “0” in NOR Flash Memory
2. The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming
3. The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4. Following the initial read access time, a byte of data is transferred on each clock edge. At 166 MHz, the continuous data rate is 333 MBps
5. A data error caused by background radiation
6. Endurance for devices supporting extended temperature range is 10,000 cycles min
7. Ball Grid Array (BGA) supports a 1-mm ball pitch
8. Read Write Data Strobe I/O
9. Hardware reset; not a mandatory signal for data transaction
10. Interrupt output; not a mandatory signal for data transaction
11. Reset output; not a mandatory signal for data transaction
Cypress 1.8-V 512Mb (S26KS512S) HyperFlash Memory

Applications
Automotive instrument cluster
Automotive infotainment
Communication equipment
Highest-performance consumer products

Features
Operating voltage range: 1.70 V to 1.95 V
100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\) (min)
20-year data retention at +55°C (typical)
Initial access time: 96 ns\(^4\)
Clock rate: 166 MHz with 333 MBps Read Bandwidth
Program\(^1\) time (512B): 475 µs (typical)
Sector Erase\(^2\) time (256KB): 930 ms (typical)
On-Chip ECC: Single-bit Soft Error\(^5\) correction
Industrial temp range (AEC-Q100 optional): -40°C to +85°C
Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
Extended temp range\(^6\) (AEC-Q100 optional): -40°C to +125°C
Package: 24-ball BGA\(^7\) 6 mm x 8 mm

Collateral
Datasheet: S26KS512S

Availability
Sampling: Now
Production: Now

1 The operation required to change a value "1" to a value "0" in NOR Flash Memory
2 The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming
3 The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4 Following the initial read access time, a byte of data is transferred on each clock edge. At 166 MHz, the continuous data rate is 333 MBps
5 A data error caused by background radiation
6 Endurance for devices supporting extended temperature range is 10,000 cycles min
7 Ball Grid Array (BGA) supports a 1-mm ball pitch
8 Read Write Data Strobe I/O
9 Hardware reset; not a mandatory signal for data transaction
10 Interrupt output; not a mandatory signal for data transaction
11 Reset output; not a mandatory signal for data transaction
Cypress 3-V 128Mb (S26KL128S) HyperFlash Memory

Applications
Automotive instrument cluster
Automotive infotainment
Communication equipment
Highest-performance consumer products

Features
Operating voltage range: 2.7 V to 3.6 V
100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\) (min)
20-year data retention at +55\(^\circ\)C (typical)
Initial access time: 96 ns\(^4\)
Clock rate: 100 MHz with 200 MBps Read Bandwidth
Program\(^1\) time (512B): 475 µs (typical)
Sector Erase\(^2\) time (256KB): 930 ms (typical)
On-Chip ECC: Single-bit Soft Error\(^5\) correction
Industrial temp range (AEC-Q100 optional): -40\(^\circ\)C to +85\(^\circ\)C
Industrial-plus temp range (AEC-Q100 optional): -40\(^\circ\)C to +105\(^\circ\)C
Extended temp range\(^6\) (AEC-Q100 optional): -40\(^\circ\)C to +125\(^\circ\)C
Package: 24-ball BGA\(^7\) 6 mm x 8 mm

Collateral
Datasheet: S26KL128S

Availability
Sampling: Now
Production: Now


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1 The operation required to change a value “1” to a value “0” in NOR Flash Memory
2 The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming
3 The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4 Following the initial read access time, a byte of data is transferred on each clock edge. At 100 MHz, the continuous data rate is 200 MBps
5 A data error caused by background radiation
6 Endurance for devices supporting extended temperature range is 10,000 cycles min
7 Ball Grid Array (BGA) supports a 1-mm ball pitch
8 Read Write Data Strobe I/O
9 Hardware reset; not a mandatory signal for data transaction
10 Interrupt output; not a mandatory signal for data transaction
11 Reset output; not a mandatory signal for data transaction
Cypress 3-V 256Mb (S26KL256S) HyperFlash Memory

Applications
- Automotive instrument cluster
- Automotive infotainment
- Communication equipment
- Highest-performance consumer products

Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\) (min)
- 20-year data retention at +55°C (typical)
- Initial access time: 96 ns\(^4\)
- Clock rate: 100 MHz with 200 MBps Read Bandwidth
- Program\(^1\) time (512B): 475 µs (typical)
- Sector Erase\(^2\) time (256KB): 930 ms (typical)
- On-Chip ECC: Single-bit Soft Error\(^5\) correction
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Extended temp range\(^6\) (AEC-Q100 optional): -40°C to +125°C
- Package: 24-ball BGA\(^7\) 6 mm x 8 mm

Collateral
- Datasheet: S26KL256S

Availability
- Sampling: Now
- Production: Now

1 The operation required to change a value "1" to a value "0" in NOR Flash Memory
2 The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming
3 The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4 Following the initial read access time, a byte of data is transferred on each clock edge. At 100 MHz, the continuous data rate is 200 MBps
5 A data error caused by background radiation
6 Endurance for devices supporting extended temperature range is 10,000 cycles min
7 Ball Grid Array (BGA) supports a 1-mm ball pitch
8 Read Write Data Strobe I/O
9 Hardware reset; not a mandatory signal for data transaction
10 Interrupt output; not a mandatory signal for data transaction
11 Reset output; not a mandatory signal for data transaction
## Applications

- Automotive instrument cluster
- Automotive infotainment
- Communication equipment
- Highest-performance consumer products

## Features

- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program\(^1\)/Sector Erase\(^2\) endurance cycles\(^3\) (min)
- 20-year data retention at +55°C (typical)
- Initial access time: 96 ns\(^4\)
- Clock rate: 100 MHz with 200 MBps Read Bandwidth
- Program\(^1\) time (512B): 475 µs (typical)
- Sector Erase\(^2\) time (256KB): 930 ms (typical)
- On-Chip ECC: Single-bit Soft Error\(^5\) correction
- Industrial temp range (AEC-Q100 optional): -40°C to +85°C
- Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
- Extended temp range\(^6\) (AEC-Q100 optional): -40°C to +125°C
- Package: 24-ball BGA\(^7\) 6 mm x 8 mm

## Collateral

**Datasheet:** S26KL512S

1. The operation required to change a value “1” to a value “0” in NOR Flash Memory
2. The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming
3. The number of times a NOR Flash Memory Sector can be Programmed or Erased before it wears out
4. Following the initial read access time, a byte of data is transferred on each clock edge. At 100 MHz, the continuous data rate is 200 MBps

## Availability

- **Sampling:** Now
- **Production:** Now

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**Explanation of Abbreviations:**

- **HyperFlash Memory**
- **Flash Memory Roadmap**
- **Sampling:** Now
- **Production:** Now

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**Note:**

5. A data error caused by background radiation
6. Endurance for devices supporting extended temperature range is 10,000 cycles min
7. Ball Grid Array (BGA) supports a 1-mm ball pitch
8. Read Write Data Strobe I/O
9. Hardware reset; not a mandatory signal for data transaction
10. Interrupt output; not a mandatory signal for data transaction
11. Reset output; not a mandatory signal for data transaction

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**Product Overview**

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**Flash Memory Roadmap**
### Cypress 3-V 1Gb (S34SL01G2) SecureNAND™ Flash Memory

#### Applications
- Set-top boxes
- Point-of-sale systems
- Wearables

#### Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program/Block Erase endurance cycles\(^1\) (typical)
- 10-year data retention at +55°C (typical)
- Error-Correcting Code (ECC)\(^2\) requirement: 4-bit ECC\(^3\)
- Volatile and Nonvolatile Block Protection\(^4\)
- Random read\(^5\) access time: 30 µs (maximum)
- Program time: 700 µs (maximum)
- Block Erase time: 10 ms (maximum)
- Industrial temp range: -40°C to +85°C
- Package: 63-ball BGA 9 mm x 11 mm

#### Collateral
- Datasheet: [Contact Sales](#)

#### Availability
- Sampling: Now
- Production: December 2015

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1. The number of times a Flash Memory Block can be Programmed/Erased before it wears out
2. Data encoded with extra parity bits to detect and correct bit errors
3. The maximum number of bit errors that need to be corrected per 528 bytes
4. Security features that provide protection from Program/Erase operations in which settings are reset or maintained on power loss
5. Read operation that accesses data using random addressing
6. Signals used for the standard Open NAND Flash Interface (ONFI) 1.0 specification
7. VPE is a signal used for Volatile Block Protection
8. WPN# is an internal signal used to prevent Program/Erase operations on the SLC NAND Flash Memory
Cypress 3-V 2Gb (S34SL02G2) SecureNAND™ Flash Memory

### Applications
- Set-top boxes
- Point-of-sale systems
- Wearables

### Features
- Operating voltage range: 2.7 V to 3.6 V
- 100,000 Program/Block Erase endurance cycles (typical)
- 10-year data retention at +55°C (typical)
- Error-Correcting Code (ECC) requirement: 4-bit ECC
- Volatile and Nonvolatile Block Protection
- Random read access time: 30 µs (maximum)
- Program time: 700 µs (maximum)
- Block Erase time: 10 ms (maximum)
- Industrial temp range: -40°C to +85°C
- Package: 63-ball BGA 9 mm x 11 mm

### Collateral
- Datasheet: [Contact Sales](#)

### Availability
- Sampling: Now
- Production: December 2015

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1 The number of times a Flash Memory Block can be Programmed/Erased before it wears out
2 Data encoded with extra parity bits to detect and correct bit errors
3 The maximum number of bit errors that need to be corrected per 544 bytes
4 Security features that provide protection from Program/Erase operations in which settings are reset or maintained on power loss
5 Read operation that accesses data using random addressing
6 Signals used for the standard Open NAND Flash Interface (ONFI) 1.0 specification
7 VPE is a signal used for Volatile Block Protection
8 WPN# is an internal signal used to prevent Program/Erase operations on the SLC NAND Flash Memory
Cypress 3-V 4Gb (S34SL04G2) SecureNAND™ Flash Memory

Applications
Set-top boxes
Point-of-sale systems
Wearables

Features
Operating voltage range: 2.7 V to 3.6 V
100,000 Program/Block Erase endurance cycles\(^1\) (typical)
10-year data retention at +55°C (typical)
Error-Correcting Code (ECC)\(^2\) requirement: 4-bit ECC\(^3\)
Volatile and Nonvolatile Block Protection\(^4\)
Random read\(^5\) access time: 30 μs (maximum)
Program time: 700 μs (maximum)
Block Erase time: 10 ms (maximum)
Industrial temp range: -40°C to +85°C
Package: 63-ball BGA 9 mm x 11 mm

Collateral
Datasheet: Contact Sales

Availability
Sampling: Now
Production: December 2015

---

\(^1\) The number of times a Flash Memory Block can be Programmed/Erased before it wears out
\(^2\) Data encoded with extra parity bits to detect and correct bit errors
\(^3\) The maximum number of bit errors that need to be corrected per 544 bytes
\(^4\) Security features that provide protection from Program/Erase operations in which settings are reset or maintained on power loss
\(^5\) Read operation that accesses data using random addressing
\(^6\) Signals used for the standard Open NAND Flash Interface (ONFI) 1.0 specification
\(^7\) VPE is a signal used for Volatile Block Protection
\(^8\) WPN# is an internal signal used to prevent Program/Erase operations on the SLC NAND Flash Memory