Cypress Roadmap: USB
Q1 2018
# USB Portfolio

## USB 3.1
- **Device**: CYUSB301x FX3
  - 32-Bit Bus to USB 3.1 Gen 1 ARM9, 512K RAM
- **Hub**: CYUSB33xx
  - HX3
  - USB 3.1 Gen 1, Shared Link™ BC 1.2, Ghost Charge™
- **Bridge**: CYUSB306x
  - GX3
  - USB 3.1 Gen 1 to GigE Energy Efficient Ethernet
- **Host**: CYUSB303x
  - FX3
  - 16-Bit Bus to USB 3.1 Gen 1 RAID®, Dual SDXC/eMMC®
- **Storage**: CYUSB302x
  - SD3
  - USB 3.1 Gen 1 SD Reader SDXC/eMMC®, RAID®
- **Type-C**: CYPD1xxx
  - CCG1
  - USB Type-C Port Controller 1 PD Port, 5 Profiles, 100 W
- **Type-C**: CYPD2xxx
  - CCG2
  - USB Type-C Cable Controller 1 PD Port, Termination, ESD
- **Type-C**: CYPD3xxx
  - CCG3
  - USB Type-C Port Controller 20-V, Crypto, Billboard
- **Type-C**: CYPD4xxx
  - CCG4/CCG4M
  - USB Type-C Port Controller 2 PD Ports, 128KB Flash, Mux
- **Type-C**: CYPD5xxx
  - CCG5
  - USB Type-C Port Controller 2 PD Ports, 25V CC/SBU
- **Type-C**: CYPD270x
  - CMG1
  - USB Type-C EMCA Controller 1 PD Port, Short Protection

## USB 2.0
- **Device**: CYCB201x
  - FX2G2
  - 32-Bit Bus to USB 2.0 ARM9 512KB RAM
- **Hub**: CYCB203x
  - HX3
  - USB 3.1 Gen 2 Type-C Hub with PD Contact Sales
- **Bridge**: CYCB205x
  - HX3C
  - 4 Ports: 1 Type-C, 3 Type-A USB PD, Billboard, BC1.2
- **Host**: CYCB207x
  - HX3P
  - USB 3.1 Gen 2 Type-C Hub with PD Contact Sales
- **Storage**: CYCB209x
  - TX2UL
  - ULPI 16-Bit Bus to USB 2.0 8051, 16KB RAM
- **Type-C**: CYPD2xxx
  - CCG2
  - USB Type-C Port Controller 1 PD Port, Termination, ESD
- **Type-C**: CYPD3xxx
  - CCG3
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1. Simultaneous USB 2.0 and SuperSpeed traffic on the same port
2. Battery Charging specification v1.2
3. Enables USB charging without host connection
4. Redundant array of independent disks
5. SD extended capacity
6. Embedded Multimedia Card
7. Display Serial Interface
8. UMTI low-pin interface

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Cypress Confidential Roadmap: USB (NDA)
## EZ-PD CCG2

**USB Type-C and PD Port Controller**

### Applications

- USB Type-C Electronically Marked Cabled Assembly (EMCA) and powered accessories

### Features

- **32-bit MCU Subsystem**
  - 48-MHz ARM® Cortex®-M0 CPU with 32KB Flash and 4KB SRAM
- **Integrated Digital Blocks**
  - Integrated timer/counter/pulse-width modulators (TCPWMs)
  - Two SCBs¹ configurable to I2C, SPI or UART modes
- **Type-C Support**
  - Integrated transceiver, supporting one Type-C port
  - Integrated termination resistors (R_P, R_D, R_A)²
- **Power Delivery (PD) Support**
  - Standard power profiles
- **Low-Power Operation**
  - Two independent V_CONN rails with integrated isolation
  - Independent supply voltage pin for GPIO
  - 2.7–5.5-V operation: Sleep: 2.0 mA; Deep Sleep: 2.5 µA
- **System-Level ESD on CC and VDD Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 20-ball CSP (3.3 mm²) with 0.4-mm ball pitch, 14-pin DFN (2.5 x 3.5 mm) with 0.6-mm pin pitch and 24-pin QFN (4 mm²) with 0.55-mm pin pitch

### Collateral

<table>
<thead>
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<th>Datasheet:</th>
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<tr>
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<td>CCG2 RDK</td>
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<td>Evaluation Kit:</td>
<td>CCG3 EVK</td>
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</tbody>
</table>

### Availability

- **Production:** Now

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¹ Serial communication block configurable as UART, SPI or I2C

² Termination resistors: R_P read as a DFP, R_D as a UFP, R_A as an EMCA
**EZ-PD CCG3**

**USB Type-C and PD Port Controller**

### Applications
- Accessories and power adapters

### Features
- One Type-C Port with Integrated Transceiver
  - Alternate Modes\(^1\), Crypto Engine\(^2\) for USB Authentication\(^3\)
- Power Delivery (PD) Support for Standard Power Profiles
- Integrated Digital Blocks for \(V_{BUS}\) Power and MUX Interface
  - 4 timers/counters/pulse-width modulators (TCPWM), 24x GPIOs
  - 4 serial communication blocks (SCBs) configurable as master/slave \(^1\)I\(^2\)C, SPI or UART
  - USB Billboard Controller\(^4\) with Billboard Device Class\(^5\) support
- Integrated Analog Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)
  - 21.5-V OVP and OCP; 2:2 cross-bar switch
- 32-bit ARM\(^\circledR\) Cortex\(^\circledR\)-M0 CPU with MCU Subsystem
  - 2x64KB Flash for fail-safe updates over CC, \(^1\)I\(^2\)C or USB interfaces
- Low-Power Operation
  - 2x \(V_{BUS}\) Gate Drivers\(^6\) for consumer and provider power paths
  - 2x high-voltage (5–21.5 V, 25 V, maximum) \(V_{BUS}\) voltage inputs
  - Sleep: 2.0 mA; Deep Sleep: 2.5 \(\mu\)A with wake-on-\(^1\)I\(^2\)C or wake-on-CC
- System-Level ESD on CC/\(V_{CONN}\), \(V_{BUS}\), and SBU Pins
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- Packages
  - 42-ball (8.38 mm\(^2\)) CSP, 40-pin (36 mm\(^2\)) QFN and 32-pin (25 mm\(^2\)) QFN

### Collateral
- **Datasheet:** [CCG3 Datasheet](#)

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1. Mode of operation in which the data lines are repurposed to transmit non-USB data
2. The encryption hardware and software required to implement USB Authentication
3. A USB-ID specification that defines the authentication protocol for Type-C accessories
4. A USB Device controller that informs the USB Host of the supported Alternate Modes
5. A specification that defines the method for a USB Device to communicate the supported Alternate Modes
6. Circuits to control the gates of external power Field-Effect Transistors (FETs) on \(V_{BUS}\) (5-20 V)
7. Termination resistors: \(R_p\) as a DFP, \(R_d\) as a UFP, \(R_a\) as an EMCA
EZ-PD CCG4/4M
Dual-Port USB Type-C and PD Port Controller

Features
- Integrated USB Type-C Transceivers Support Two Type-C Ports
  - Integrated 2x 1-W \( V_{CONN} \) FETs and 2x FET control signals, per port programmable \( R_P \) \(^1\) and removable \( R_P \) and \( R_D \) \(^2\) terminations
  - Supports dead battery mode operation
  - Integrated SuperSpeed USB/DisplayPort (DP) Mux (CCG4M)
- Increased Flash Enables Fail-Safe Bootup
  - Integrates 128KB Flash to store dual FW images for fail-safe boot
- Integrated Digital Blocks for Inter-Chip Communications
  - Four serial communication blocks (SCBs) master or slave configurable to \( I^2C \), SPI or UART
  - SCBs interconnect CCG4 with embedded controller, two alternate muxes and Thunderbolt controller (optional)
- Integrated Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)
  - Four 8-bit SAR ADCs configurable for OVP and OCP
- Low-Power Operation
  - 2.7–V to 5.5-V operation and independent supply voltage for GPIO; Sleep: 2.0 mA; Deep Sleep: 2.5 \( \mu \)A with wake-on-\( I^2C \) or wake-on-configuration channel (CC)
- System-Level ESD on CC Pins
  - \( \pm 8-kV \) Contact, \( \pm 15-kV \) Air Gap IEC61000-4-2 Level 4C
- 32-bit ARM\(^\circledR\) Cortex\(^\circledR\)-M0 CPU with MCU Subsystem
  - 128KB Flash, upgradable over CC lines or \( I^2C \) interface
- Packages
  - 40-pin QFN, 96-ball BGA (CCG4M)

Availability
- Production: Now

Collateral
- Datasheet: CCG4 Datasheet

1 Termination resistor read as a DFP
2 Termination resistor read as a UFP
EZ-PD CCG3PA
USB Type-C and PD Port Controller

**Applications**
Power adapters, chargers, power banks

**Features**

- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO to power CCG3PA
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI, or UART

- **Integrated Analog**
  - Configurable \( V_{BUS} \) overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier\(^1\) with analog out for \( V_{BUS} \) control
  - Low side current sense\(^2\) capable of detecting 100mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC\(^3\))

- **32-bit ARM\(^{®}\) Cortex\(^{®}\)-M0 CPU with 64KB Flash**

- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) \( V_{BUS} \) voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 \( \mu \)A with wake-on-I²C or CC

- **System-Level ESD on CC / \( V_{CONN} \) \( V_{BUS} \), and SBU Pins**
  - \( \pm 8-kV \) Contact, \( \pm 15-kV \) Air Gap IEC61000-4-2 Level 4C

- **Packages**
  - 24-QFN (16 mm\(^2\)), 16-SOIC (60 mm\(^2\))

**Collateral**

- Datasheet: [CCG3PA Datasheet](#)

**Availability**

- Production: Now

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\(^1\) Analog feedback voltage control circuit to control \( V_{BUS} \)
\(^2\) Circuit to measure the current flowing on the \( V_{BUS} \)
\(^3\) Adaptive Fast Charging
\(^4\) Termination resistors: \( R_p \) read as a DFP, \( R_d \) as a UFP, \( R_a \) as an EMCA
EZ-PD CCG5
Dual-Port USB Type-C and PD Port Controller

Applications
Notebooks, docks, Thunderbolt devices

Features
- Integrated Type-C Transceiver for Two Type-C USB PD 3.0-Compliant Ports
  - Support for Thunderbolt, DisplayPort (DP), HDMI Alt Mode and USB platforms
  - USCI1-compliant Interface with WHQL2-certified driver
  - Support for UEFI3 driver with Microsoft capsule firmware download
- Integrated Analog
  - Integrated high-voltage LDO and 4x VCONN FETs supporting up to 500 mA
  - Integrated 2x2 USB analog switch; integrated SBU analog pass with high-voltage tolerance
  - Integrated 2x USB Charger Detect (BC 1.2, Apple Charging, QC 4.0 and Samsung AFC4)
  - Integrated Type-C termination resistors (RP, RC, RDB)5
  - 25-V tolerance on CC1/2 and SBU pins
- ARM® Cortex®-M0 CPU with 128KB Flash and 12KB SRAM
  - 4x serial communication blocks (SCB) - I²C, SPI or UART
  - Firmware upgradable over SWD/I²C interfaces
  - Supports Dead Battery mode operation
  - Overvoltage protection (OVP) with 2µs response time; integrated VBUS/VCONN overcurrent protection (OCP)
- System-Level ESD on CC/VCONN, VBUS, and SBU Pins
  - ±8-kV Contact, ±15-kV Air Discharge IEC61000-4-2 Level 4C
- Packages
  - 2-Port in 96-BGA (6 mm²), 1-Port in 40-QFN (6 mm²)

Collateral
Datasheet: CCG5 Datasheet

CCG5: USB Type-C Port Controller

MCU Subsystem
- ARM Cortex-M0 48 MHz
- Flash (128KB)
- SRAM (12KB)

Integrated Digital Blocks
- 2x TCPWM
- SCB (I²C, SPI, UART)
- SCB (I²C, SPI, UART)
- SCB (I²C, SPI, UART)

I/O Subsystem
- Programmable I/O Matrix
- 4x GPIO Port

USB PD Subsystem x2
- Baseband MAC
- Baseband PHY
- Hi-Voltage LDO (21.5V)
- 4x 8-bit SAR ADC
- 2x VFETs Gate Driver

System Resources
- 2x VCONN FETs
- 2x VBUS / VCONN OCP
- HV Protection On CC, SBU
- UVP/OVP
- 2x VFETs Gate Driver

Availability
Production: Now

1 USB Type-C Connector System Software Interface
2 Unified Extensible Firmware Interface
3 Termination resistors: RP, read as a DFP, RC as a UFP, RDB as UFP in Dead-Battery scenario
4 Windows Hardware Quality Labs
5 Adaptive Fast Charging
EZ-PD CMG1
USB Type-C Passive EMCA Controller

Applications
USB-C EMCA

Features
- USB-C PD Controller, PD 3.0 Transceiver
- $V_{BUS}$-to-CC Short Protection
- $V_{BUS}$-to-$V_{CONN}$ Short Protection
- Power from $V_{CONN}$ Range 3.0–5.5-V
- Termination Resistor $R_A$
- Supports $R_A$ Weakening to Reduce Power Consumption
- Configurable 40-byte Storage for Configuration Over Type-C Interface
- Integrated Oscillator Eliminating the Need for External Clock
- Power Operation
  - 2.7–5.5-V operation ($V_{CONN}$ pin)
  - Active: 7.5 mA
  - Sleep: 1 mA
- System-Level ESD on CC, $V_{CONN}$ Pins
  - ±8-kV contact, ±15-kV Air Gap IEC61000-4-2 level 4C
- Packages
  - 9-ball WLCSP (1.95 mm$^2$)
  - Supports industrial temperature range (-40°C to +85°C)

Collateral
Preliminary Datasheet: CMG1 Datasheet

CMG1: Passive EMCA Controller

<table>
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<th>USB PD Subsystem</th>
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<tbody>
<tr>
<td>$V_{BUS}$-to-CC Short Protection</td>
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<tr>
<td>$V_{BUS}$-to-$V_{CONN}$ Short Protection, $R_A$</td>
</tr>
<tr>
<td>$V_{BUS}$-to-$V_{CONN}$ Short Protection, $R_A$</td>
</tr>
<tr>
<td>EMCA Protocol Engine</td>
</tr>
<tr>
<td>USB Type-C Physical Layer</td>
</tr>
</tbody>
</table>

Storage
40-Byte Storage for Configuration

System Resources
Oscillator
Reset
VREF
IREF

Availability
Samples: Now  Production: Q2 2018
EZ-USB FX3
USB 3.1 Gen 1 Peripheral Controller

**Applications**
- Industrial cameras, medical and machine vision cameras, 3-D and 1080p full HD and 4K Ultra HD (UHD) cameras, document and fingerprint scanners, videoconferencing and data acquisition systems, video capture cards and HDMI converters, protocol and logic analyzers, USB test tools and software-designed radios (SDRs)

**Features**
- USB 3.1 Gen 1-Compliant Peripheral Controller
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- Fully Accessible 32-bit, 200-MHz ARM® 926EJ Core
  - 512KB of embedded SRAM for code space and buffers
- 32-bit, 100-MHz, flexible GPIF II Interface
  - Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- Flexible Clock Options
- Packages
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)

**Collateral**
- Datasheet: [FX3 Datasheet](#)
- Development Kit: [FX3 SuperSpeed Explorer Kit](#)
- Software Development Kit: [EZ-USB FX3 SDK](#)

**Availability**
- Production: Now
EZ-USB FX3S
USB 3.1 Gen 1 RAID1-on-Chip

Applications
Servers, routers, mobile storage, USB Flash drives, POS terminals, automatic teller machines (ATM), SDIO expanders and data logging devices

Features
- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz ARM® 926EJ Core**
  - 512KB of embedded SRAM for code space and buffers
- **32-bit, 100-MHz, Flexible GPIF II Interface**
  - Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
- **Two SDXC2, eMMC3 4,4, or SDIO 3.0 Interfaces**
  - Support RAID0 or RAID1 configurations
- **Flexible Clock Options**
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- **Packages**
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)

Collateral
Datasheet: [FX3S Datasheet](#)
Kit: [FX3S RAID1-on-Chip Boot Disk Kit](#)
Software Development Kit: [EZ-USB FX3 SDK](#)

Availability
Production: Now

FX3S: RAID1-on-Chip

1 Redundant array of independent disks
2 SD extended capacity
3 Embedded Multimedia Card
**Applications**

Industrial, medical and machine vision cameras, 1080p full HD and 4K Ultra HD (UHD) cameras, document scanners, fingerprint scanners, game consoles, videoconferencing systems, notebook PCs, tablets and image acquisition systems

**Features**

- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz ARM® 926EJ core**
  - 512KB of embedded SRAM for code space and buffers
- **Four-Lane MIPI^1 Camera Serial Interface v2.0 (CSI-2) Input**
  - Camera Control Interface (CCI) for image sensor configuration
  - Other peripheral interfaces such as I²C, UART, SPI and 12 GPIOs
- **Supports Industry-Standard Video Data Formats**
  - RAW8/10/12/14^2, YUV422/444^3, RGB888/666/565^4
- **Supports Uncompressed Streaming Video**
  - 4K UHD at 15 fps, 1080p at 30 fps, 720p at 60 fps
- **Packages**
  - 121-ball BGA (10 x 10 x 1.7 mm)

**Collateral**

- **Datasheet:** [CX3 Datasheet](#)
- **Reference Design Kit:** [CX3 Reference Design Kit](#)
- **Software Development Kit:** [EZ-USB FX3 SDK](#)

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1. Mobile Industry Processor Interface
2. Video format for raw video data
3. Video format for luminance and chrominance components
4. Video format for red, green and blue pixel components

**Availability**

**Production:** Now
EZ-USB GX3
USB 3.1 Gen 1 to GigE¹ Bridge

Applications
USB dongles, docking stations and port replicators, network printers and security cameras, ultrabooks and home gateways, game consoles and portable media players, DVRs, IP set-top boxes and IP TVs and other embedded systems

Features
- One-Chip USB 3.1 Gen 1 to 10/100/1000M GigE Bridge
  - Integrates USB 3.1 Gen 1 PHY and GigE PHY
  - Integrates USB 3.1 Gen 1 Controller and GigE MAC²
  - Needs only a 25-MHz crystal to drive both USB and GigE1 PHY
- IEEE 802.3az³ Support for Low-Power Idle State
  - Supports dynamic cable length and power adjustment
  - Offers multiple power management wake-on-LAN⁴ features
- Supports Optional EEPROM to Store USB Descriptors
  - Integrates on-chip power-on-reset (POR) circuitry
- Packages
  - 68-QFN (8 x 8 x 0.85 mm)

Collateral
Datasheet: GX3 Datasheet
Reference Design Kit: GX3 Reference Design Kit
Software & Drivers: GX3 Drivers

Availability
Production: Now

¹ Gigabit Ethernet
² Media access controller that provides the address to an Ethernet node
³ A new-energy efficient Ethernet standard
⁴ An Ethernet standard that allows a computer to be turned on by a network message
EZ-USB HX3
USB 3.1 Gen 1 Hub

Applications
Docking stations for notebook PCs and tablets, PC motherboards, servers, televisions and monitors, retail hub boxes, printers and scanners, set-top boxes, home gateways, routers and game consoles

Features
- USB 3.1 Gen 1-Compliant Four-Port Hub Controller
  - USB-IF certified (Test ID: 330000047)
  - WHQL certified for Windows 7, Window 8, Windows 8.1
- Shared Link™
  - Supports simultaneous USB 2.0 and USB SuperSpeed (SS) devices on the same port
- Ghost Charge™
  - Enables USB charging while the hub is disconnected from a USB Host
- Charging Standard support
  - USB-IF Battery Charging (BC) v1.2, Apple Charging Standard
  - Charging an OTG Host in an ACA-Dock
- Programming of External EEPROM via USB
- Configurable USB SS and USB 2.0 PHY (drives 11” trace)
- Packages
  - 68-QFN (8 x 8 x 1.0 mm), 88-QFN (10 x 10 x 1.0 mm), 100-BGA (6 x 6 x 1.0 mm)

Collateral
Datasheet: HX3 Datasheet
Kit: CY4609, CY4603, CY4613
Configuration Utility: Blaster Plus¹
App Notes: HX3 Hardware Design Guide (AN91378)

Availability
Production: Now

¹ A Cypress GUI-based PC application for setting HX3 configuration parameters
² Transaction translator
EZ-USB HX3C
USB 3.1 Gen 1 Type-C PD Hub

Applications
USB Type-C charging hubs, adapters and accessories, docking stations for notebook PCs and tablets, televisions and monitors, PC motherboards and servers, set-top boxes, home gateways and routers

Features
- USB 3.1 Gen 1-Compliant Hub Controller with Type-C and PD
  - Upstream (US): Type-C, Downstream (DS): 1 Type-C and 2 Type-A ports
- Integrated Type-C Transceivers, Supporting Two Type-C Ports
  - Integrated termination resistors (R_P and R_D)¹
  - Integrated USB Billboard Controller²
- Charging Support
  - USB PD, BC v1.2, Apple Charging Standard
  - PD policy engine configures power profiles dynamically
- Ghost Charge™
  - Charging DS without US connection
- Firmware Upgradable Over USB
- System-Level ESD on Configuration Channel (CC) Pins
  - 8 kV Contact, 15 kV Air
- Configurable USB SS and USB 2.0 PHY (drives 11” trace)
- Packages
  - 121-ball BGA (10 mm x 100 mm, 0.8 mm ball-pitch)

Collateral
Datasheet: HX3C Datasheet
Reference Design: HX3C Type-C Monitor/Dock Reference Design

Availability
Production: Now

¹ Termination resistors: R_P read as a DFP, R_D as a UFP
² A USB Device controller that is used to implement the USB Billboard Device Class
₃ Transaction Translator
Informs the USB Host of the supported Alternate Modes as well as any failures
EZ-USB HX3PD
USB 3.1 Gen 2 Type-C Hub with Power Delivery

Applications
Notebook/tablet docking stations, monitor docks, multi-function USB Type-C peripherals

Features
- USB 3.1 Gen 2-Compliant Hub Controller with Type-C and PD
  - Upstream (US) ports:
    - 10 Gbps; Type-A or Type-C plus PD (UFP)
  - Downstream (DS) ports:
    - 7 ports: 5x 10 Gbps, 2x 480 Mbps
    - 2 Type-C ports: 1 PD port (DFP), 1 Type-C only
- Integrated Type-C Transceivers and Dual-PHY for Type-C plug orientation correction
  - Integrated termination resistors (R_P and R_D)\(^1\)
  - Integrated USB Billboard Controller\(^2\), USB Type-C Bridge Controller
  - Integrated VCONN FETs and ADC for overvoltage and overcurrent protection
- Charging Support
  - USB PD, BC v1.2, Apple Charging Standard, QC 4.0, Samsung AFC
  - USB PD policy engine configures power profiles dynamically
- Ghost Charge\(^TM\): Charging DS without US connection
- Dock Management Controller for secured firmware download
  - Firmware upgradeable over USB
- System-Level ESD on Configuration Channel (CC) Pins: 8 kV Contact, 15 kV Air
- Package: 192-ball BGA (12 mm x 12 mm x 1 mm, 0.8-mm ball-pitch)

Collateral
Datasheet: HX3PD Datasheet
Kit: HX3PD Evaluation Kit

Availability
Samples: Q1 2018 Production: Q3 2018

1 Termination resistors: R_P read as a DFP, R_D as a UFP
2 A USB Device controller that is used to implement the USB Billboard Device Class
  Informs the USB Host of the supported Alternate Modes as well as any failures
3 Transaction Translator