Features

- Detects Rising Edge, Falling Edge, or Either Edge

General Description

The Edge Detector component samples the connected signal and produces a pulse when the selected edge occurs.

When to Use an Edge Detector

Use the Edge Detector when a circuit needs to respond to a state change on a signal.

Input/Output Connections

This section describes the various input and output connections for the Edge Detector.

**d – Input**

The signal connected to the d input is the signal that will be sampled for an edge.

**clock – Input**

The clock input determines how often the d input will be sampled.

**det – Output**

The det output pulses high when an edge is detected on the d input.
Component Parameters

Drag an Edge Detector onto your design and double-click it to open the **Configure** dialog.

The Edge Detector provides the following parameters.

**Edgetype**

This parameter determines what type of edge to detect. The value must be **Rising Edge**, **Falling Edge**, or **Either Edge**. The default is **Rising Edge**.

**Functional Description**

The Edge Detector stores the state of the signal at the last rising clock edge, and compares it to the current value of the signal. If the state change matches the edge type selected in the customizer, the det terminal will go high until the next rising clock edge. This means that the resulting pulse from an edge may be shorter than one clock cycle, but it will never be longer.

*Figure 1. Rising Edge Schematic*
Figure 1 displays a logical representation of the implementation for the **Rising Edge** configuration. Figure 2 provides a sample waveform to illustrate the functionality.

**Figure 2. Rising Edge Waveform**

As seen in Figure 2, the `det` output will go high as soon as a **rising** edge is detected on the `d` input. The `det` output is cleared on the next rising clock edge.

**Figure 3. Falling Edge Schematic**

Figure 3 displays a logical representation of the implementation for the **Falling Edge** configuration. Figure 4 provides a sample waveform to illustrate the functionality.

**Figure 4. Falling Edge Waveform**

As seen in Figure 4, the `det` output will go high as soon as a **falling** edge is detected on the `d` input. The `det` output is cleared on the next rising clock edge.

**Figure 5. Either Edge Schematic**

Figure 5 displays a logical representation of the implementation for the **Falling Edge** configuration. Figure 6 provides a sample waveform to illustrate the functionality.
Figure 6. Either Edge Waveform

As seen in Figure 6, the \textit{det} output will go high as soon as any edge is detected on the \textit{d} input. The \textit{det} output is cleared on the next rising clock edge.

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**MISRA Compliance**

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined: project deviations – deviations that are applicable for all PSoC Creator components and specific deviations – deviations that are applicable only for this component. This section provides information on component specific deviations. The project deviations are described in the MISRA Compliance section of the \textit{System Reference Guide} along with information on the MISRA compliance verification environment.

The Edge Detector component does not have any C source code APIs.

**Component Changes**

Version 1.0 is the first release of the Edge Detector Component.