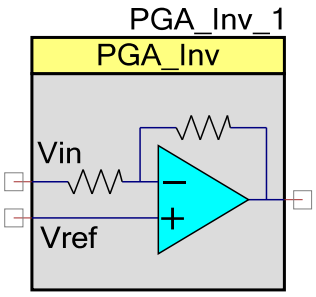
Inverting Programmable Gain Amplifier (PGA_Inv)

1.60

Features

- Gain steps from -1 to -49
- High input impedance
- Adjustable power settings



General Description

The Inverting Programmable Gain Amplifier (PGA_Inv) component implements an opamp-based inverting amplifier with user-programmable gain. It is derived from the SC/CT block.

The inverting gain can be between -1.0 (0 dB) and -49.0 (+33.8 dB). The gain can be selected via configuration or changed at run-time using the provided API. The maximum bandwidth is limited by the gain-bandwidth of the opamp and is reduced as the gain is increased. The input of the PGA_Inv operates from rail to rail, but the maximum input swing (difference between Vin and Vref) is limited to Vdda/Gain. The output of the PGA_Inv is class A, and is rail to rail for sufficiently high load resistance.

The PGA_Inv is used when an input signal has insufficient amplitude and the preferred output polarity is the inverse of the input. A PGA_Inv may be placed in front of a comparator, ADC, or mixer to increase the signal amplitude. A unity gain PGA_Inv may be used following another gain stage or buffer to generate differential outputs.

Input/Output Connections

This section describes the various input and output connections for the PGA_Inv. An asterisk (*) in the list of I/Os indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

Vin – Analog

Vin is the input signal terminal.

Vref – Analog

Vref is the input terminal for a reference signal. The reference input has a high impedance and may be connected to fixed reference (e.g., Vdda/2), VDAC output or routed to a pin.

Vout – Analog

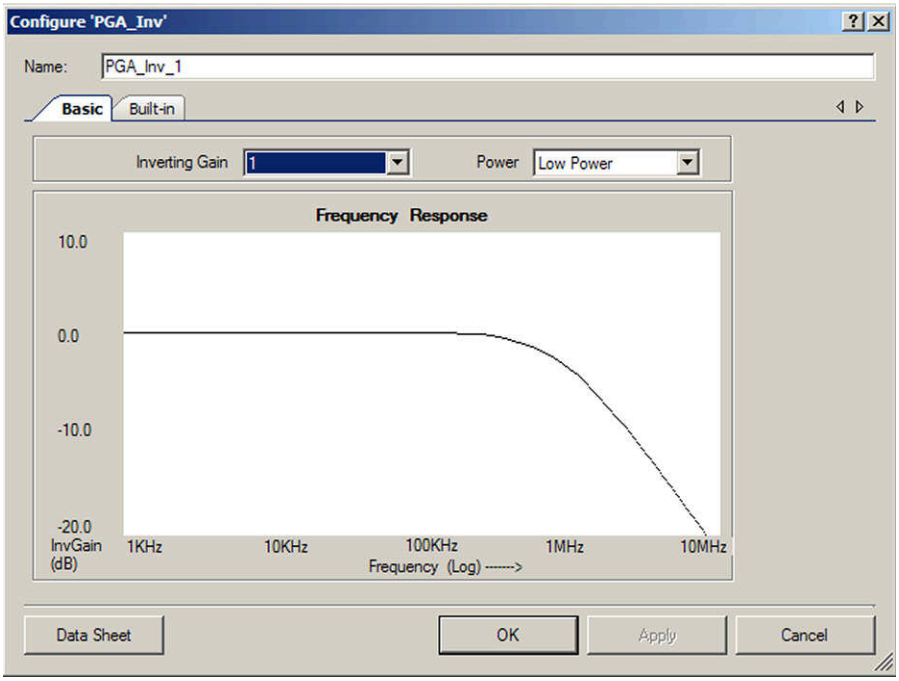
Vout is the output voltage signal terminal. Vout is a function of (Vin - Vref) times the Gain:

*Vout = Vref + (Vin-Vref) * Gain* where Gain is a negative value

Parameters and Setup

Drag a PGA_Inv component onto your design and double-click it to open the Configure dialog.

Figure 1 Configure PGA_Inv Dialog



Inverting_Gain

This parameter is used to set the default gain of the amplifier. The allowable inverting gains provided are: -1 (default), -3, -7, -15, -22, -24, -31, -47, and -49.

Power

This sets the initial drive power of the PGA_Inv. The **Power** setting determines the speed with which the PGA_Inv responds to changes in the input signal. There are four **Power** settings: Minimum, Low, Medium (default), and High. A Low setting results in the slowest response time and a High setting results in the fastest response time. The **Power** setting can be set at runtime using the PGA_Inv_SetPower() API.

Placement

There are no placement specific options.

Resources

The PGA_Inv uses one SC/CT block. Additional details on this block can be found in the applicable device data sheet and the Technical Reference Manual (TRM). These documents are available on the Cypress web site.

	Digital Blocks					API Memory (Bytes)		
Analog Blocks	Datapaths	Macro cells	Status Registers	Control Registers	Counter7	Flash	RAM	Pins (per External I/O)
1 SC/CT Fixed block	N/A	N/A	N/A	N/A	N/A	356	20	3

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. The following table lists and describes the interface to each function. The subsequent sections cover each function in more detail.

By default, PSoC Creator assigns the instance name "PGA_Inv_1" to the first instance of a component in a given design. You can rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is "PGA_Inv".

Function	Description
void PGA_Inv_Start(void)	Start the PGA_Inv.
void PGA_Inv_Stop(void)	Power down the PGA_Inv.
void PGA_Inv_SetGain(uint8 gain)	Set gain to pre-defined constants.
void PGA_Inv_SetPower(uint8 power)	Set drive power to one of four settings.
void PGA_Inv_Sleep(void)	Stops and saves the user configurations.
void PGA_Inv_Wakeup(void)	Restores and enables the user configurations.
void PGA_Inv_SaveConfig(void)	Empty function. Provided for future usage.
void PGA_Inv_RestoreConfig(void)	Empty function. Provided for future usage.

Function	Description
void PGA_Inv_Init(void)	Initializes or restores default PGA_Inv configuration.
void PGA_Inv_Enable(void)	Enables the PGA_Inv.

Global Variables

Variable	Description
PGA_Inv_initVar	Indicates whether the PGA_Inv has been initialized. The variable is initialized to 0 and set to 1 the first time PGA_Inv_Start() is called. This allows the component to restart without reinitialization after the first call to the PGA_Inv_Start() routine. If reinitialization of the component is required, then the PGA_Inv_Init() function can be called before the PGA_Inv_Start() or PGA_Inv_Enable() function.

void PGA_Inv_Inv_Start(void)

Description: Turns on the PGA_Inv and sets the power level.

Parameters: None

Return Value: None

Side Effects: None

void PGA_Inv_Stop(void)

Description: Turns off PGA_Inv and enables its lowest power state.

Note This API is not recommended for use on PSoC 3 ES2 and PSoC 5 ES1 silicon. These devices have a defect that causes connections to several analog resources to be unreliable when not powered. The unreliability manifests itself in silent failures (e.g. unpredictably bad results from analog components) when the component utilizing that resource is stopped. It is recommended that this component be powered up (by calling the PGA_Inv_Start() function at all times. Do not call PGA_Inv_Stop().

Parameters: None

Return Value: None

Side Effects: None. Does not affect power or gain settings.

void PGA_Inv_SetGain(uint8 gain)

Description: Set gain of amplifier between -1 and -49. The table below shows the valid gain settings.

Parameters: Uint8 gain: Set the gain to a specific value. See table below for valid gain settings.

Gain Setting	Notes
PGA_Inv_GAIN_01	Gain = -1
PGA_Inv_GAIN_03	Gain = -3
PGA_Inv_GAIN_07	Gain = -7
PGA_Inv_GAIN_15	Gain = -15
PGA_Inv_GAIN_22	Gain = -22
PGA_Inv_GAIN_24	Gain = -24
PGA_Inv_GAIN_31	Gain = -31
PGA_Inv_GAIN_47	Gain = -47
PGA_Inv_GAIN_49	Gain = -49

Return Value: None

Side Effects: None

void PGA_Inv_SetPower(uint8 power)

Description: Sets the drive power to one of four settings; minimum, low, medium, or high.

Parameters: (uint8) power: Sets the power level to one of three settings, low, medium, or high.

Power Setting	Notes
PGA_Inv_MINPOWER	Minimum active power and slowest reaction time.
PGA_Inv_LOWPOWER	Low power and speed.
PGA_Inv_MEDPOWER	Medium power and speed.
PGA_Inv_HIGHPOWER	Highest active power and fastest reaction time.

Return Value: None

Side Effects: None

void PGA_Inv_Sleep(void)

Description: This is the preferred routine to prepare the component for sleep. The PGA_Inv_Sleep() function saves the current component state. Then it calls the PGA_Inv_Stop() function and calls PGA_Inv_SaveConfig() to save the hardware configuration.

Call the PGA_Inv_Sleep() function before calling the CyPmSleep() or the CyPmHibernate() function. Refer to the PSoC Creator *System Reference Guide* for more information about power management functions.

Parameters: None

Return Value: None

Side Effects: None

void PGA_Inv_Wakeup(void)

Description: This is the preferred routine to restore the component to the state when PGA_Inv_Sleep() was called. The PGA_Inv_Wakeup() function calls the PGA_Inv_RestoreConfig() function to restore the configuration. If the component was enabled before the PGA_Inv_Sleep() function was called, the PGA_Inv _Wakeup() function will also re-enable the component.

Parameters: None

Return Value: None

Side Effects: Calling the PGA_Inv_Wakeup() function without first calling the PGA_Inv_Sleep() or PGA_Inv_SaveConfig() function may produce unexpected behavior.

void PGA_Inv_SaveConfig(void)

Description: Empty function. Provided for future usage.

Parameters: None

Return Value: None

Side Effects: None

void PGA_Inv_RestoreConfig(void)

Description: Empty function. Provided for future usage.

Parameters: None

Return Value: None

Side Effects: None

void PGA_Inv_Init(void)

Description: Initializes or restores the component according to the customizer Configure dialog settings. It is not necessary to call PGA_Inv_Init() because the PGA_Inv_Start() routine calls this function and is the preferred method to begin component operation.

Parameters: None

Return Value: None

Side Effects: All registers will be set to values according to the customizer Configure dialog.

void PGA_Inv_Enable(void)

Description: Activates the hardware and begins component operation. It is not necessary to call PGA_Inv_Enable() because the PGA_Inv_Start() routine calls this function, which is the preferred method to begin component operation.

Parameters: None

Return Value: None

Side Effects: None

Sample Firmware Source Code

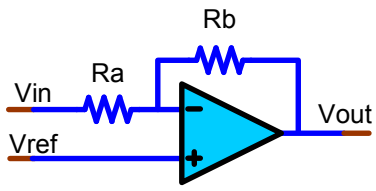
PSoC Creator provides numerous example projects that include schematics and example code in the Find Example Project dialog. For component-specific examples, open the dialog from the Component Catalog or an instance of the component in a schematic. For general examples, open the dialog from the Start Page or **File** menu. As needed, use the **Filter Options** in the dialog to narrow the list of projects available to select.

Refer to the "Find Example Project" topic in the PSoC Creator Help for more information.

Functional Description

The PGA_Inv is constructed from a generic SC/CT block. The gain is selected by adjusting two resistors, Ra and Rb. (See the following figure.). Ra may be set to either 20K or 40K ohms, depending on selected gain. Rb may be set between 20K and 1000K ohms, to generate the possible gain values selectable in either the Configure dialog or the SetGain function.

Figure 2 PGA_Inv Schematic



The block has a programmable capacitor in parallel with the feedback resistor, Rb. The capacitor value is configured for each gain selection to achieve guaranteed stability. Reassigning Rb values without also selecting the appropriate feedback capacitor value may result in PGA_Inv instability. You are strongly advised to use the provided APIs for gain changes.

The input resistance of the PGA_Inv is finite. The gain accuracy is dependent on the routing resistance between the source and the Vin input. The gain specifications accommodate the nominal variation in the routing resistance.

Registers

The PGA_Inv component configuration is implemented in registers SC[0..3]_CR0, SC[0..3]_CR1 and SC[0..3]_CR2. These can be accessed in user code by reference to the instantiated component name, e.g., PGA_Inv_1_CR0_REG. The register contents can be reviewed in the PSoC Creator component debug window. Refer to the applicable TRM, available on the Cypress web site, for a detailed description of each register. The following registers are displayed in the PGA component debug window.

Register: PGA_Inv_1_CR0_REG

Name: Switched Capacitor Control Register 0

Description: Register bits 3:1 configure the switch capacitor block operating mode. This field is set to 110b for the PGA component.

Register: PGA_Inv_1_CR1_REG

Name: Switched Capacitor Control Register 1

Description: Register fields configure drive mode, compensation capacitor values, and gain setting of the switch capacitor block.

Register: PGA_Inv_1_CR2_REG

Name: Switched Capacitor Control Register 2

Description: Register fields configure the input impedance, feedback impedance and the reference ground selection for the switch capacitor block.

Register: PGA_Inv_1_PM_ACT_CFG_REG

Name: Active Power Mode Configuration Register 9

Description: Register bits 3:0 enable power to the four switch capacitor blocks.

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the tables below, all T_A = 25° C, V_{dd} = 5.0 V, Power HIGH, opamp bias LOW, output referenced to Analog Ground = V_{ssa} .

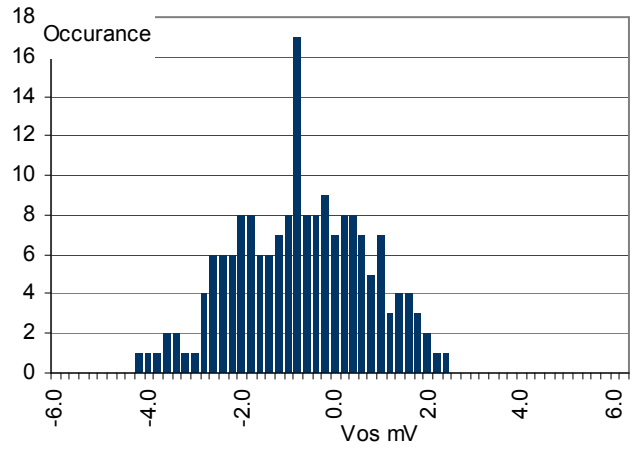
5.0V/3.3V DC Electrical Characteristics

Data collection is currently in progress. This table will be updated in a future release.

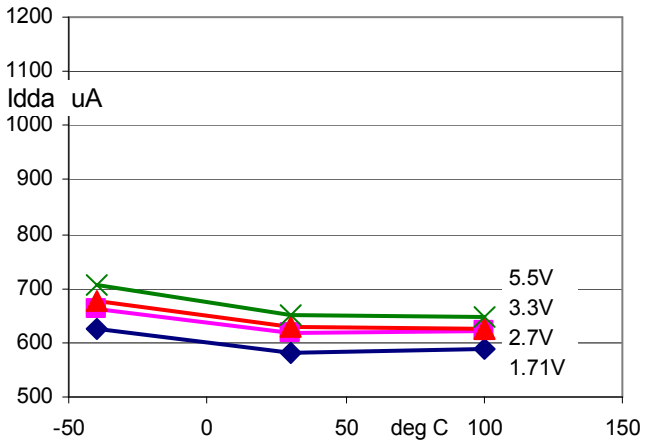
Parameter	Description	Conditions	Min	Typ	Max	Units
Vin	Input voltage range	Power mode = minimum	Vssa	–	Vdda	V
Vos	Input offset voltage	Power mode = high, gain = 1, Vdda = 5 V	–	TBD	10	mV
TCVos	Input offset voltage drift with temperature	Power mode = high, gain = 1, Vdda = 5 V	–	±30	TBD	µV/°C
Ge1	Gain error, gain = 1	Vdda = 5 V	–	±TBD	±0.15	%
Ge16	Gain error, gain = 16	Vdda = 5 V	–	±TBD	±2.5	%
Ge50	Gain error, gain = 50	Vdda = 5 V	–	±TBD	±5	%
Gd1	Gain drift, gain = 1		–	±TBD	±TBD	ppm/°C
Gd16	Gain drift, gain = 16		–	±TBD	±TBD	ppm/°C
Gd50	Gain drift, gain = 50		–	±TBD	±TBD	ppm/°C
VonI	DC output nonlinearity	Gain = 1	–	–	±0.01	% of FSR
Rin	Input resistance		35	–	–	MΩ
Cin	Input capacitance		–	–	TBD	pF
Voh, Vol	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	V_{DDA} – 0.15	TBD	V_{SSA} + 0.15	V
Iout	Output current, source or sink	V_{SSA} + 500 mV = Vout = V_{DDA} – 500 mV	TBD	TBD	–	µA
Idd	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		69	TBD	–	dB

Figures

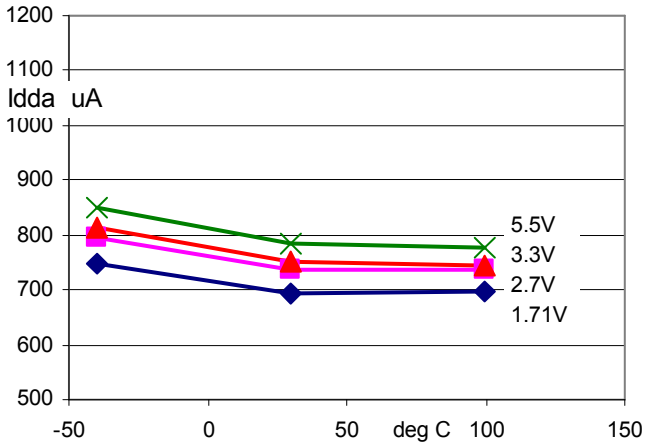
Histogram Input Offset Voltage



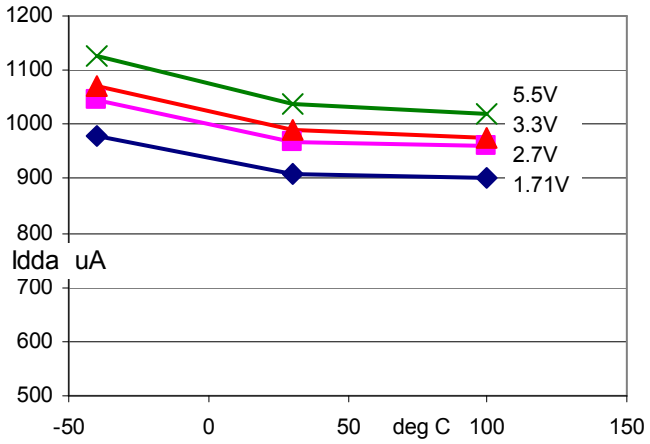
Typical Operating Current vs Temp, Power = Minimum



Typical Operating Current vs Temp, Power = Low



Typical Operating Current vs Temp, Power = High

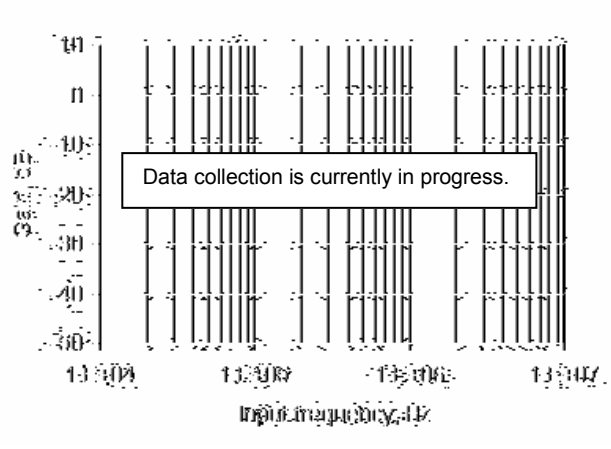


5.0V/3.3V AC Electrical Characteristics

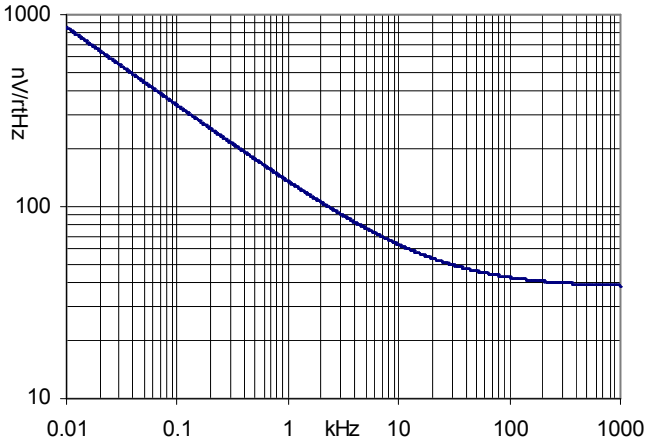
Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1, Vdda = 5V	7	TBD	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	TBD	–	V/µs
e_n	Input noise density	Power mode = high, Vdda = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

Figures

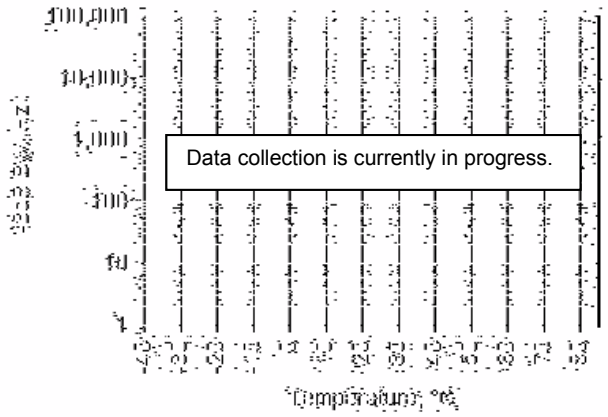
Gain vs. Frequency, at Different Gain Settings, Vdda = 3.3 V, Power Mode = High



Voltage noise, Vdda = 5.0V, Power=High



Bandwidth vs. Temperature, at Different Gain Settings, Power = High



Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
1.60	Removed VDDA parameter from component customizer	VDDA setting in the component is redundant and unnecessary for multiple components. The parameter was removed and the component queries the global setting for minimum VDDA in the DWR and automatically enables the pump when necessary.
	Configuration window created to include Frequency response graphs a better ease of use GUI.	Previous configuration window did not provide enough information for ease of use.

Version	Description of Changes	Reason for Changes / Impact
	SetGain constants corrected in the header file	The constants provided for the SetGain API had incorrect values. These have been corrected.
	Added characterization data to datasheet	
	Minor datasheet edits and updates	
1.50	Added Sleep/Wakeup and Init/Enable APIs.	To support low power modes, as well as to provide common interfaces to separate control of initialization and enabling of most components.
	Removed Gain setting of 23.	The gain of 23 was too close to 22 and 24 and therefore offered no value.
	Updated the symbol and Configure dialog.	These were updated to comply with corporate standards.