ADC Guide, Part 1 – The Ideal ADC

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Analog to Digital Converters (ADCs) are one of the most commonly used blocks in embedded systems. Applications of ADCs include current sensing, motor control, temperature sensing and a myriad of others. As a consequence, understanding the basic specifications of an ADC and selecting an appropriate device for the given application is a must for reliable operation and cost-effective design. This series of articles will begin with the basics of ADCs and then discuss different characteristics of an ADC that are important to design, including the impact of various irregularities, types of ADC available on the market, advantages and disadvantages of each type, and how their selection varies from application to application. This first part of this article series discusses what exactly is an ADC and how an ideal ADC works. In the subsequent articles, we will go to more practical aspects and parameters of an ADC.

What is an ADC?

An ADC is a device that converts an analog signal to an equivalent digital signal. An analog signal is continuous in both time and amplitude whereas a digital signal is discrete in time as well as in amplitude. Logically, an ADC has to covert an analog signal to an equivalent digital one in two steps: converting the analog signal to a discrete in time signal and converting it into a discrete in amplitude signal. The process of converting an analog signal to discrete in time signal is called as 'sampling' and the process of converting it to a discrete in amplitude signal is called 'quantization'. These processes can occur in any order.

Figure 1 shows the sampling and quantization of a simple sine wave signal. Signal A in this figure is an analog signal. Signal B and Signal C show the effect of quantization and sampling separately on this signal. Signal D is the composite digital signal and can be obtained either through quantization of a sampled signal or through sampling of a quantized signal.

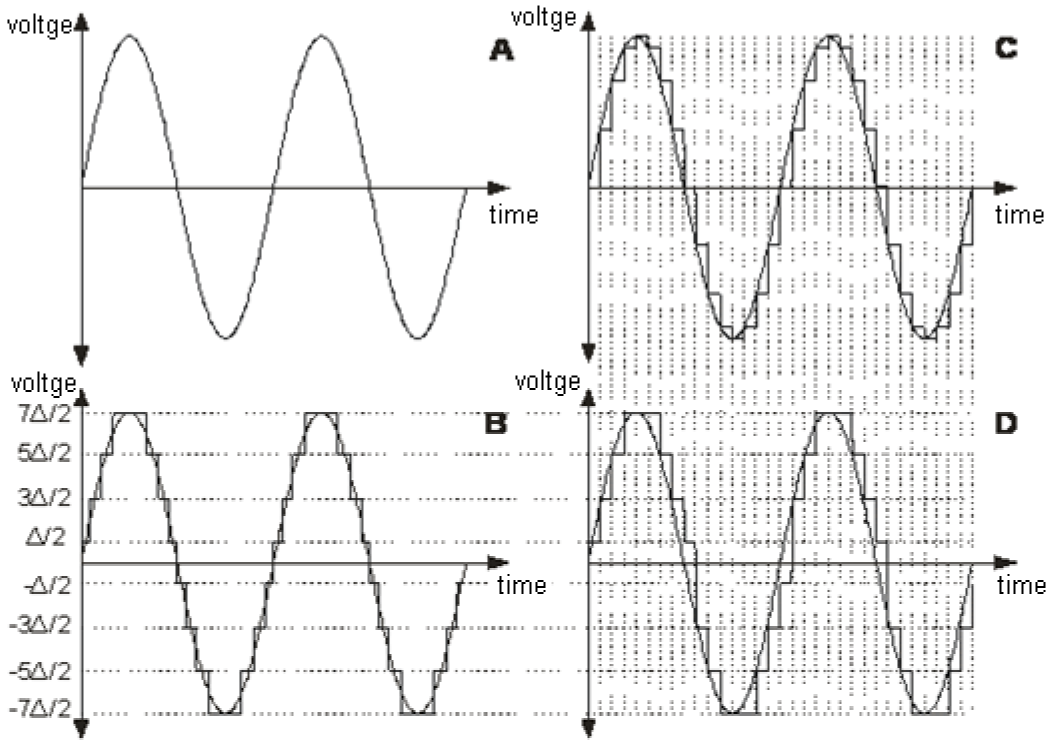

Figure 1. Operation of an ideal ADC.

The example above shows the analog to digital conversion as done by an ideal ADC. An ideal ADC has a linear response throughout the input range of ADC. The input range of an ADC can be considered as the range of analog voltages that ADC is able to convert to an equivalent digital signal. If an ADC is able to convert both positive as well as negative voltage, then its response will be split in the first and third quadrants (Figure 2-A). On the other hand, if the ADC is able to convert only positive voltage, then, its response will be limited to the first quadrant (Figure 2-B). In both the cases, the maximum amplitude of analog voltage that the ADC can convert is called the ‘Full scale input voltage’ of the ADC.

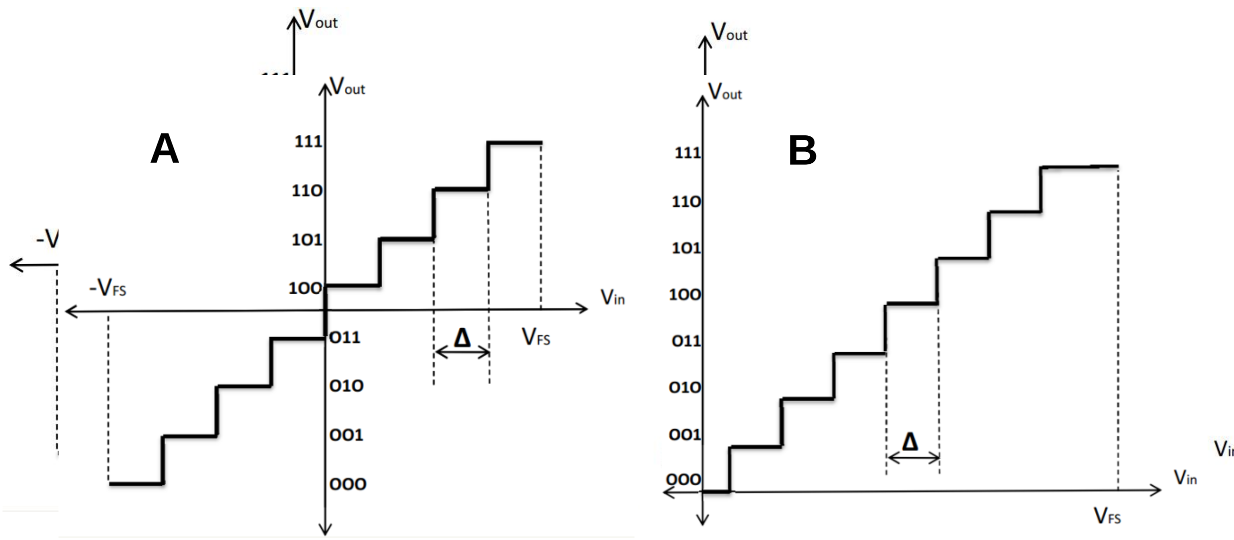

Figure 2. Response of an ideal ADC

As it can be seen in Figure 2, the response of an ideal ADC is perfectly linear. This means that none of the digital codes are missing in the output of the ADC and every successive code occurs at the output exactly after a definite increment in the input voltage. In this diagram, the entire input range of the ADC is divided into 8 equal parts and each of these parts corresponds to a digital output code. This span of analog voltage after which an ADC changes its output is known as one LSB for the ADC based on the fact that this much change in ADC input will change the output of the ADC by one bit. The LSB of an ADC is also known as the ‘Step Size’ of the ADC. The terms are often used interchangeably.

Step size

Step size is the minimum change in input voltage which can be resolved by the ADC. The concept of step size is closely associated with the resolution of ADC.

Resolution

The resolution of an ADC refers to the number of bits in the digital output code of the ADC. Thus, for an ADC with a response as shown in Figure2, the resolution will be 3 bits. The relation between step size, resolution, and input range can be given by:

$$Step\ Size = \frac{Input\ Range}{2^{Resolution}} \qquad \cdots Equation\ (1)$$

$$where\ \ Input\ Range = V_{FS} \qquad ;\ for\ ADC\ oprating\ with\ only\ positive\ input$$

$$= 2 \times V_{FS} \qquad ;\ for\ ADC\ operating\ with\ positive\ and\ negative\ input$$

Noise in an ideal ADC

After the above discussion about an ideal ADC, one may think that there will not be any noise in an ideal ADC. However, this is not the case. As Figure 2 shows, an ideal ADC converts an analog signal to its equivalent digital signal linearly with a constant step size. During the quantization phase, the signal loses its original amplitude and is represented by the closest digital code as compared to its amplitude. This quantization noise is the only source of noise for an ideal ADC, and it varies from $(-\Delta/2)$ to $(\Delta/2)$, where Δ is the step size of the ADC. Figure 3 shows the variation of quantization noise throughout the entire input range of an ideal ADC.

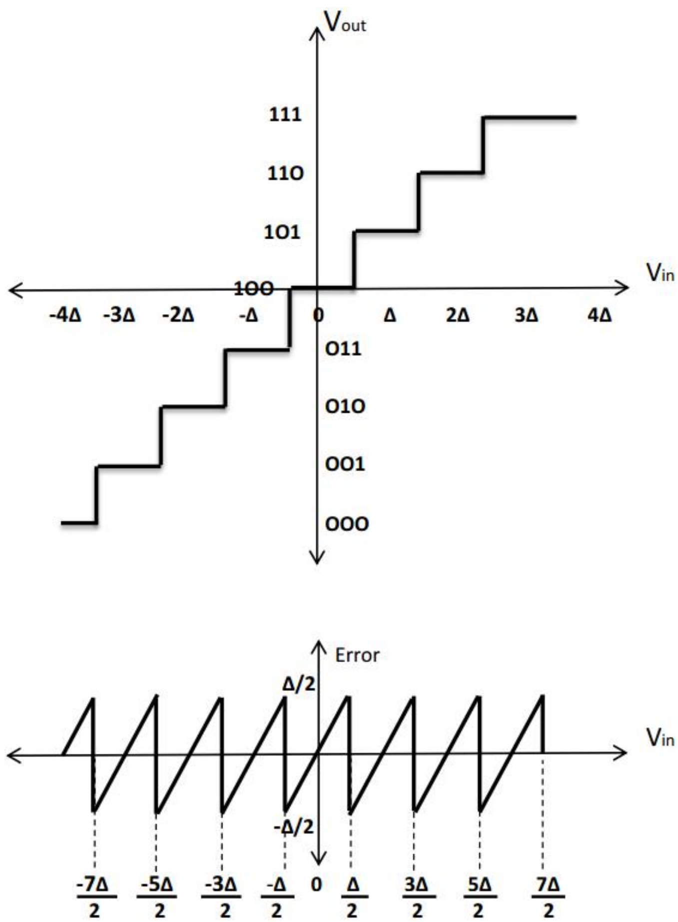

Figure 3. Quantization noise

Signal-to-noise ratio

The integrity of conversion of an ADC is measured in terms of its signal-to-noise ratio (SNR). SNR is defined as the relation of signal amplitude to noise amplitude in the output of an ADC at a given time. SNR is typically measured in terms of decibels and is given by Equation (2):

$$SNR_{dB} = 20 \log_{10} \frac{Signal\ Amplitude}{Noise\ Amplitude} \qquad \cdots Equation\ (2)$$

As stated previously, the only noise source for an ideal ADC is quantization noise. Thus, to find the SNR of an ideal ADC, we replace signal amplitude by the root mean square (RMS) value of a full scale sine wave signal and noise amplitude by the RMS value of quantization noise throughout the input range. Considering these definitions, the SNR of an ideal ADC is:

$$\begin{aligned}
Signal\ Amplitude &= RMS\ of\ full\ scale\ sine\ wave \\
&= \frac{Peak\ to\ Peak\ voltage}{2 \times \sqrt{2}} \\
&= \frac{V_{FS}}{2 \times \sqrt{2}} \\
Signal\ Amplitude &= \frac{\Delta \times 2^N}{2 \times \sqrt{2}} \qquad ; N - Resolution, \Delta - Step\ Size
\end{aligned}$$

Considering the quantization noise only over $(-\Delta/2)$ to $(\Delta/2)$ as it is repetitive,

$$\begin{aligned}
Noise\ Amplitude &= RMS\ quantization\ noise \\
&= \sqrt{\frac{1}{\Delta} \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} v^2 dv} \\
&= \sqrt{\frac{1}{\Delta}\left[\frac{\left(\frac{\Delta}{2}\right)^3}{3} - \frac{\left(-\frac{\Delta}{2}\right)^3}{3}\right]} \\
&= \sqrt{\frac{\Delta^2}{12}} \\
Noise\ Amplitude &= \frac{\Delta}{\sqrt{12}}
\end{aligned}$$

Replacing these values in Equation (2), we get a SNR for an ideal ADC as follows:

$$\begin{aligned}
SNR_{dB} &= 20 \log_{10}\left[\frac{\Delta \times 2^N / 2 \times \sqrt{2}}{\Delta / \sqrt{12}}\right] \\
&= 20 \log_{10}\left[\frac{2^N}{\sqrt{3/2}}\right] \\
&= 20\ N \times \log_{10} 2 + 20 \log_{10} \sqrt{3/2} \\
SNR_{dB} &= 6.02\ N + 1.76 \qquad \cdots Equation\ (3)
\end{aligned}$$

As seen in Equation (3), the SNR of an ideal ADC depends solely on the resolution of the ADC. As we increase the resolution, we keep adding quantization levels exponentially. This reduces the step size and increases the possibility of finding a digital

code nearer to any given analog input voltage within the input range of ADC. This results in a reduction of quantization noise, as well as a corresponding increase in the SNR.

Next time, we will look more into the practical aspects of an ADC. The second part of this series will cover sample rate and the effects of sampling rate on the output of an ADC.

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