

Features

- Temperature ranges
 - Automotive-A: -40 °C to 85 °C
 - Automotive-E: -40 °C to 125 °C
- Pin and function compatible with CY7C1021CV33
- High speed
 - t_{AA} = 10 ns (Automotive-A)
 - t_{AA} = 12 ns (Automotive-E)
- CMOS for optimum speed and power
- Low active power: 325 mW (max)
- Automatic power down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin 400 Mil SOJ, 44-pin TSOP II, and 48-ball FBGA packages

Functional Description

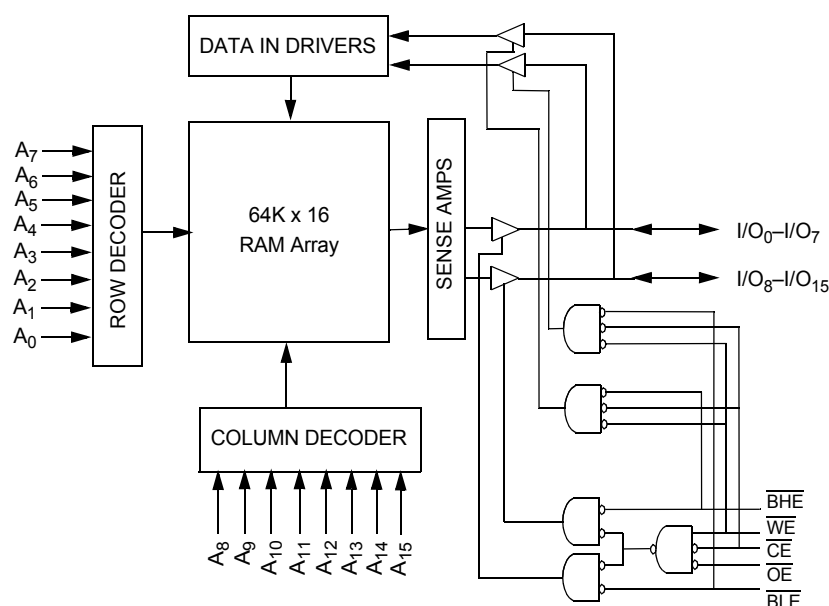
The CY7C1021CV33 is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₁ through I/O₈), is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₉ through I/O₁₆) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O₁ to I/O₈. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₉ to I/O₁₆. For more information, see the [Truth Table on page 10](#) for a complete description of Read and Write modes.

The input and output pins (I/O₁ through I/O₁₆) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (\overline{CE} LOW and WE LOW).

Logic Block Diagram



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Selection Guide

Description		-10	-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Automotive-A	90	–	mA
	Automotive-E	–	90	mA
Maximum CMOS Standby Current	Automotive-A	5	–	mA
	Automotive-E	–	10	mA

Pin Configuration

Figure 1. 44-pin SOJ/TSOP II ^[1]

A ₄	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	OE
A ₀	5	40	BHE
CE	6	39	BLE
I/O ₁	7	38	I/O ₁₆
I/O ₂	8	37	I/O ₁₅
I/O ₃	9	36	I/O ₁₄
I/O ₄	10	35	I/O ₁₃
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₅	13	32	I/O ₁₂
I/O ₆	14	31	I/O ₁₁
I/O ₇	15	30	I/O ₁₀
I/O ₈	16	29	I/O ₉
WE	17	28	NC
A ₁₅	18	27	A ₈
A ₁₄	19	26	A ₉
A ₁₃	20	25	A ₁₀
A ₁₂	21	24	A ₁₁
NC	22	23	NC

Figure 2. 48-ball FBGA Pinout ^[1]

1	2	3	4	5	6	
BLE	OE	A ₀	A ₁	A ₂	NC	A
I/O ₈	BHE	A ₃	A ₄	CE	I/O ₀	B
I/O ₉	I/O ₁₀	A ₅	A ₆	I/O ₂	I/O ₁	C
V _{SS}	I/O ₁₁	NC	A ₇	I/O ₃	V _{CC}	D
V _{CC}	I/O ₁₂	NC	NC	I/O ₄	V _{SS}	E
I/O ₁₄	I/O ₁₃	A ₁₄	A ₁₅	I/O ₅	I/O ₆	F
I/O ₁₅	NC	A ₁₂	A ₁₃	WE	I/O ₇	G
NC	A ₈	A ₉	A ₁₀	A ₁₁	NC	H

Note

1. NC pins are not connected on the die.

Pin Definitions

Pin Name	SOJ, TSOP Pin Number	BGA Pin Number	I/O Type	Description
A ₀ –A ₁₅	1–5, 18–21, 24–27, 42–44	A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4	Input	Address Inputs. Used to select one of the address locations.
I/O ₁ –I/O ₁₆ ^[2]	7–10, 13–16, 29–32, 35–38	B6, C6, C5, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	Input or Output	Bidirectional Data I/O lines. Used as input or output lines depending on operation.
NC	22, 23, 28	A6, D3, E3, E4, G2, H1, H6	No Connect	No Connects. Not connected to the die.
$\overline{\text{WE}}$	17	G5	Input or Control	Write Enable Input, Active LOW. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.
$\overline{\text{CE}}$	6	B5	Input or Control	Chip Enable Input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}, \overline{\text{BLE}}$	40, 39	B2, A1	Input or Control	Byte Write Select Inputs, Active LOW. $\overline{\text{BHE}}$ controls I/O ₁₆ – I/O ₉ , $\overline{\text{BLE}}$ controls I/O ₈ – I/O ₁ .
$\overline{\text{OE}}$	41	A2	Input or Control	Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, the I/O pins are tristated and act as input data pins.
V _{SS}	12, 34	D1, E6	Ground	Ground for the Device. Connected to ground of the system.
V _{CC}	11, 33	D6, E1	Power Supply	Power Supply Inputs to the Device.

Note

2. I/O₁–I/O₁₆ for SOJ/TSOP and I/O₀–I/O₁₅ for BGA packages.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Ambient Temperature with
Power Applied -55 °C to +125 °C

Supply Voltage on
 V_{CC} Relative to GND ^[3] -0.5 V to +4.6 V

DC Voltage Applied to Outputs
in High Z State ^[3] -0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage ^[3] -0.5 V to $V_{CC} + 0.5$ V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage
(MIL-STD-883, Method 3015) > 2001 V

Latch Up Current > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Automotive-A	-40 °C to +85 °C	3.3 V \pm 10%
Automotive-E	-40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		Unit
				Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = −4.0 mA		2.4	–	2.4	–	V
V _{OL}	Output LOW Voltage	V _{CC} = Min, I _{OL} = 8.0 mA		–	0.4	–	0.4	V
V _{IH}	Input HIGH Voltage			2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[3]			−0.3	0.8	−0.3	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	Automotive-A	−1	+1	–	–	μA
			Automotive-E	–	–	−12	+12	
I/O _Z	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output disabled	Automotive-A	−1	+1	–	–	μA
			Automotive-E	–	–	−12	+12	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Automotive-A	–	90	–	–	mA
			Automotive-E	–	–	–	90	
I _{SB1}	Automatic CE Power Down Current — TTL Inputs	Max V _{CC} , CE ≥ V _{IH} V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Automotive-A	–	15	–	–	mA
			Automotive-E	–	–	–	20	
I _{SB2}	Automatic CE Power Down Current — CMOS Inputs	Max V _{CC} , CE ≥ V _{CC} − 0.3 V, V _{IN} ≥ V _{CC} − 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	Automotive-A	–	5	–	–	mA
			Automotive-E	–	–	–	10	

Note

3. $V_{IL}(\text{min}) = -2.0$ V and $V_{IH}(\text{max}) = V_{CC} + 0.5$ V for pulse durations of less than 20 ns.

Capacitance

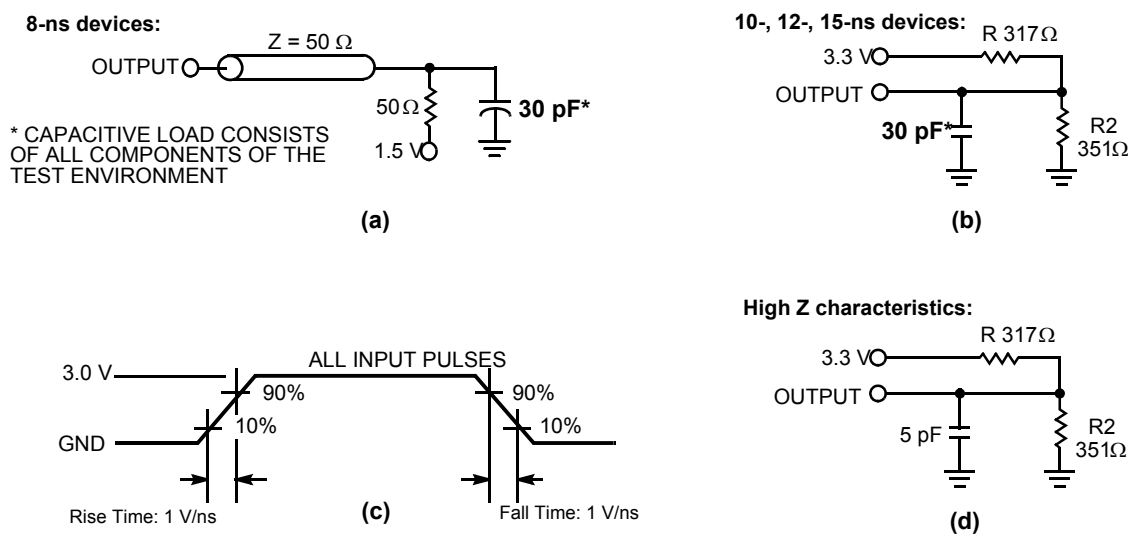
Parameter ^[4]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{ V}$	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter ^[4]	Description	Test Conditions	44-pin SOJ	44-pin TSOP II	48-ball FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	65.06	76.92	95.32	$^\circ\text{C/W}$
Θ_{JC}	Thermal Resistance (Junction to Case)		34.21	15.86	10.68	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[5]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) for all 8-ns parts are tested using the load conditions shown in Figure 3 (a). All other speeds are tested using the Thevenin load shown in Figure 3 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (d).

Switching Characteristics

Over the Operating Range

Parameter ^[6]	Description	-10		-12		Unit
		Min	Max	Min	Max	
Read Cycle						
t _{power} ^[7]	V _{CC} (Typical) to the First Access	100	–	100	–	μs
t _{RC}	Read Cycle Time	10	–	12	–	ns
t _{AA}	Address to Data Valid	–	10	–	12	ns
t _{OHA}	Data Hold from Address Change	3	–	3	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid	–	10	–	12	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid	–	5	–	6	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[8]	0	–	0	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[8, 9]	–	5	–	6	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[8]	3	–	3	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[8, 9]	–	5	–	6	ns
t _{PU} ^[10]	$\overline{\text{CE}}$ LOW to Power Up	0	–	0	–	ns
t _{PD} ^[10]	$\overline{\text{CE}}$ HIGH to Power Down	–	10	–	12	ns
t _{DBE}	Byte Enable to Data Valid	–	5	–	6	ns
t _{LZBE}	Byte Enable to Low Z	0	–	0	–	ns
t _{HZBE}	Byte Disable to High Z	–	5	–	6	ns
Write Cycle ^[11]						
t _{WC}	Write Cycle Time	10	–	12	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	8	–	9	–	ns
t _{AW}	Address Setup to Write End	8	–	9	–	ns
t _{HA}	Address Hold from Write End	0	–	0	–	ns
t _{SA}	Address Setup to Write Start	0	–	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	7	–	8	–	ns
t _{SD}	Data Setup to Write End	5	–	6	–	ns
t _{HD}	Data Hold from Write End	0	–	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[8]	3	–	3	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[8, 9]	–	5	–	6	ns
t _{BW}	Byte Enable to End of Write	7	–	8	–	ns

Notes

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
7. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
8. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of [Figure 3 on page 6](#). Transition is measured ± 500 mV from steady state voltage.
10. This parameter is guaranteed by design and is not tested.
11. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW, $\overline{\text{WE}}$ LOW, and $\overline{\text{BHE/BLE}}$ LOW. $\overline{\text{CE}}$, $\overline{\text{WE}}$, and $\overline{\text{BHE/BLE}}$ is LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled)^[12, 13]

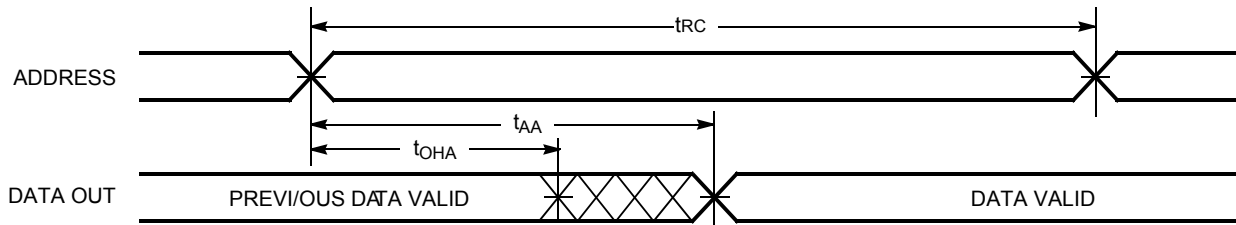
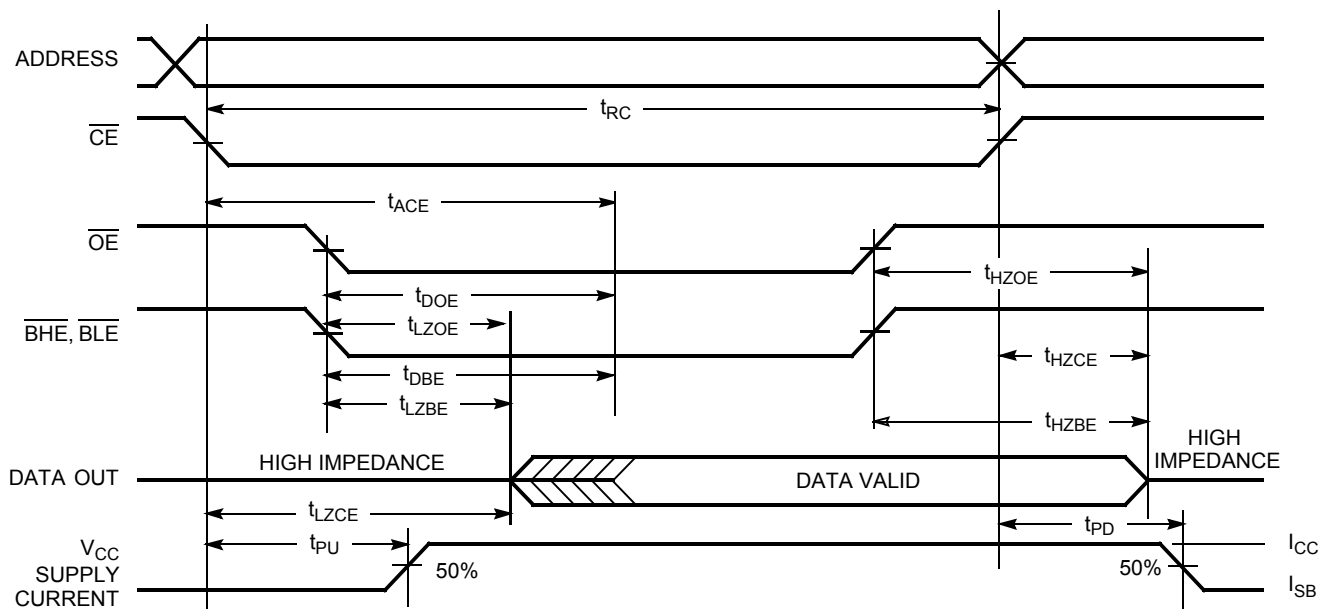


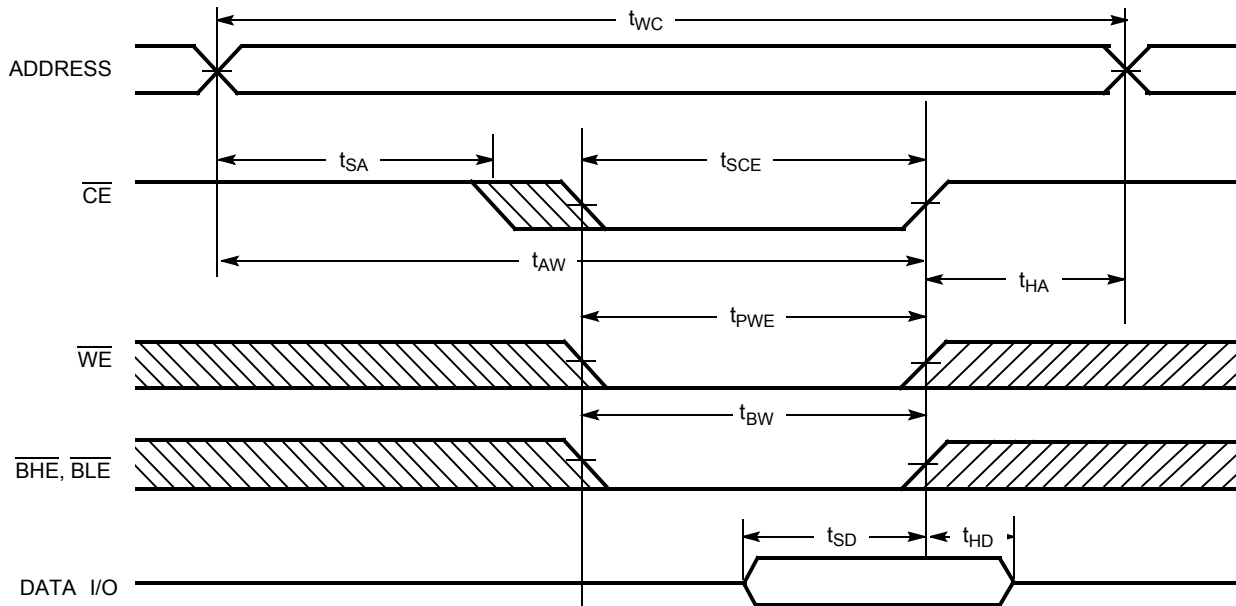
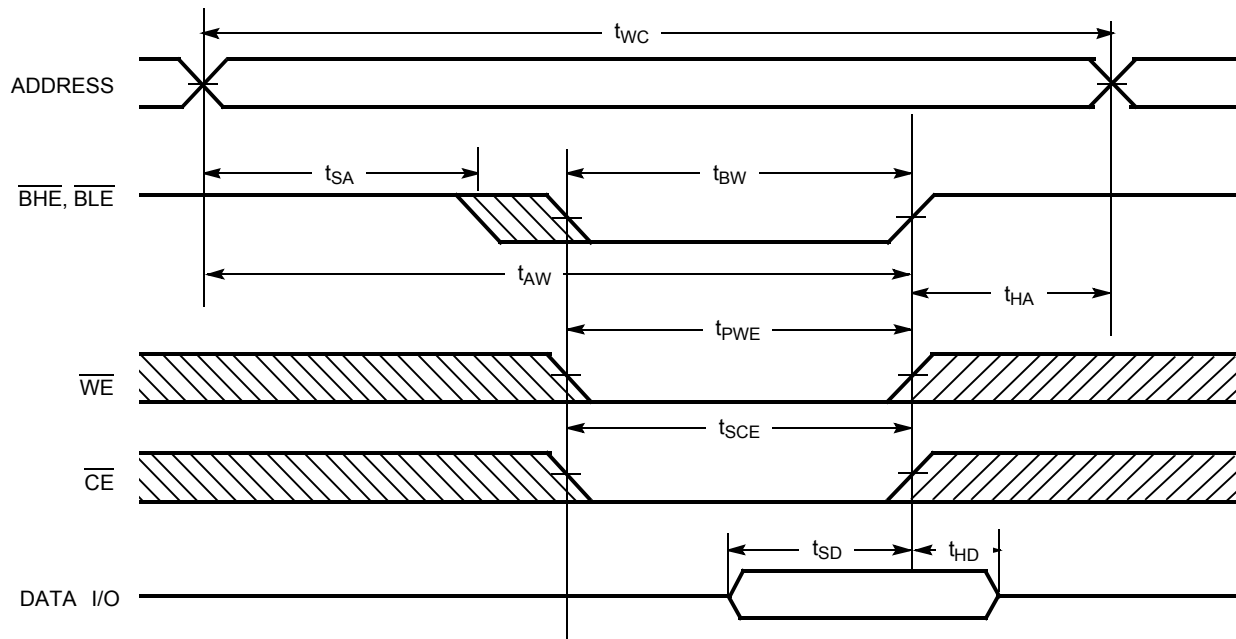
Figure 5. Read Cycle No. 2 (\overline{OE} Controlled)^[13, 14]



Notes

12. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} , and/or \overline{BLE} = V_{IL} .
13. \overline{WE} is HIGH for read cycle.
14. Address valid prior to or coincident with \overline{CE} transition LOW.

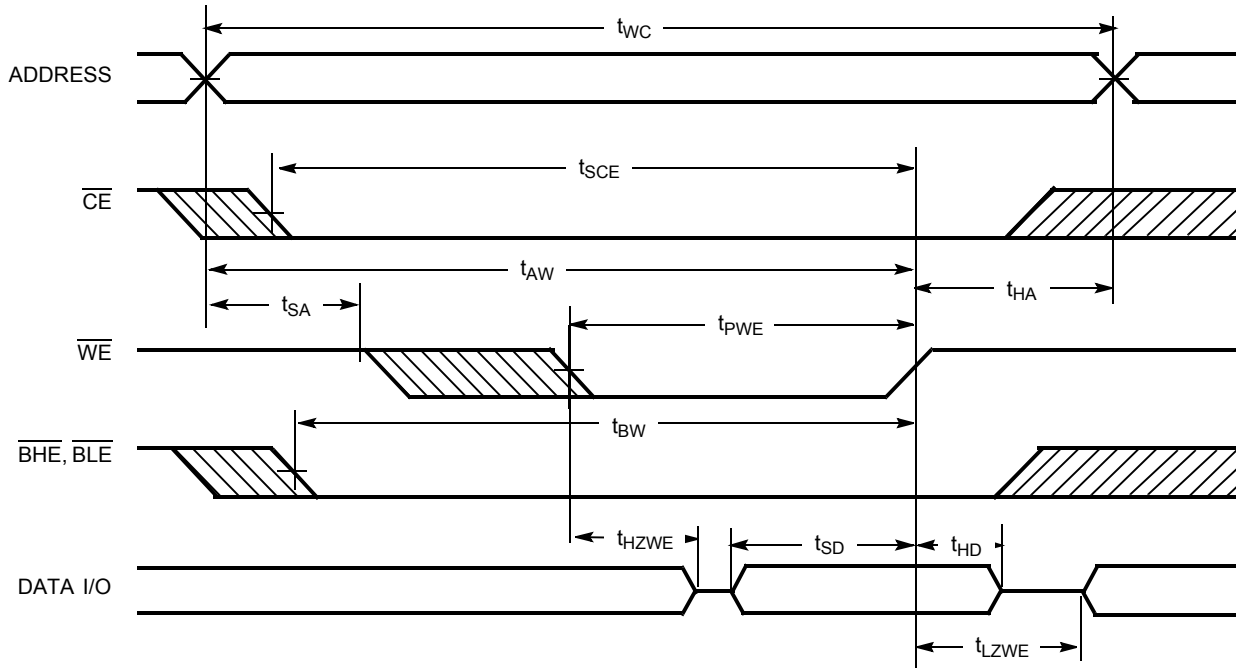
Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[15, 16]

Figure 7. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

Notes

 15. Data I/O is high impedance if $\overline{\text{OE}}$, $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.

 16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, LOW)

Truth Table

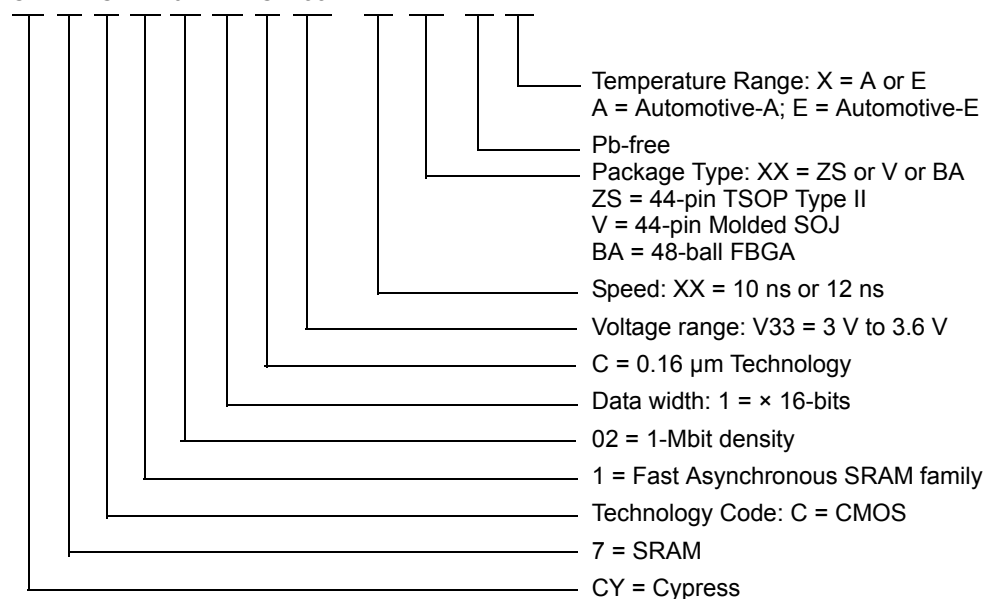
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₁ – I/O ₈	I/O ₉ – I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All Bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All Bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1021CV33-10ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A
12	CY7C1021CV33-12VXE	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Automotive-E
	CY7C1021CV33-12ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021CV33-12BAE	51-85096	48-ball FBGA	

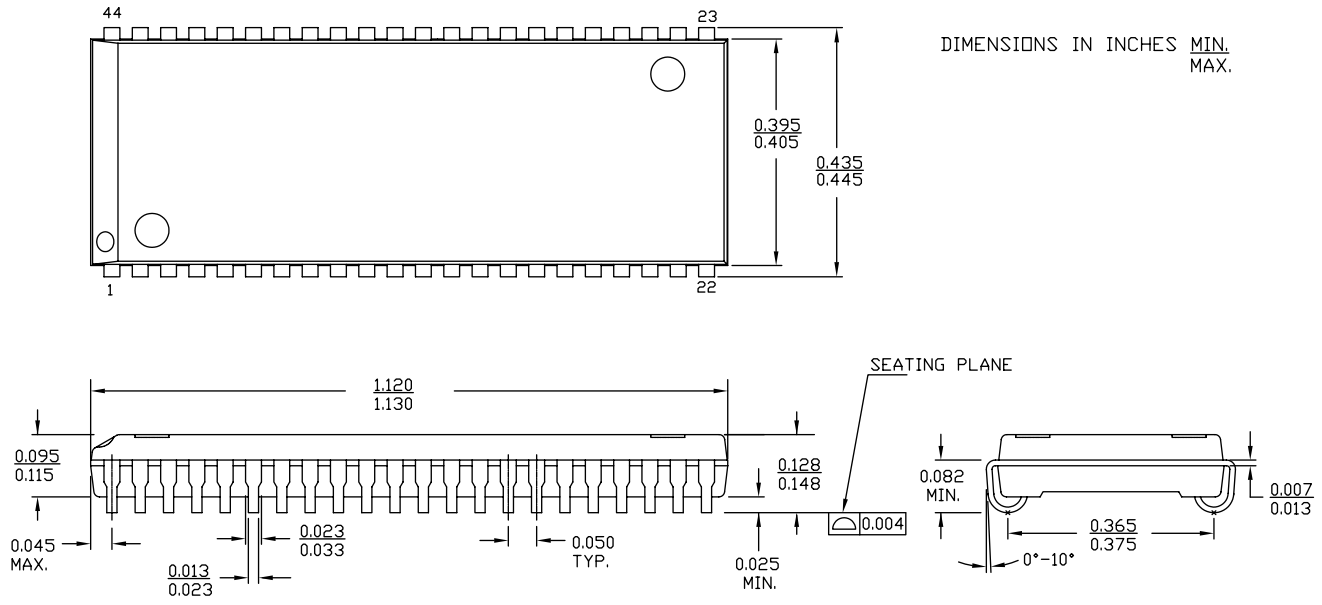
Ordering Code Definitions

CY 7 C 1 02 1 C V33 - XX XX X X



Package Diagrams

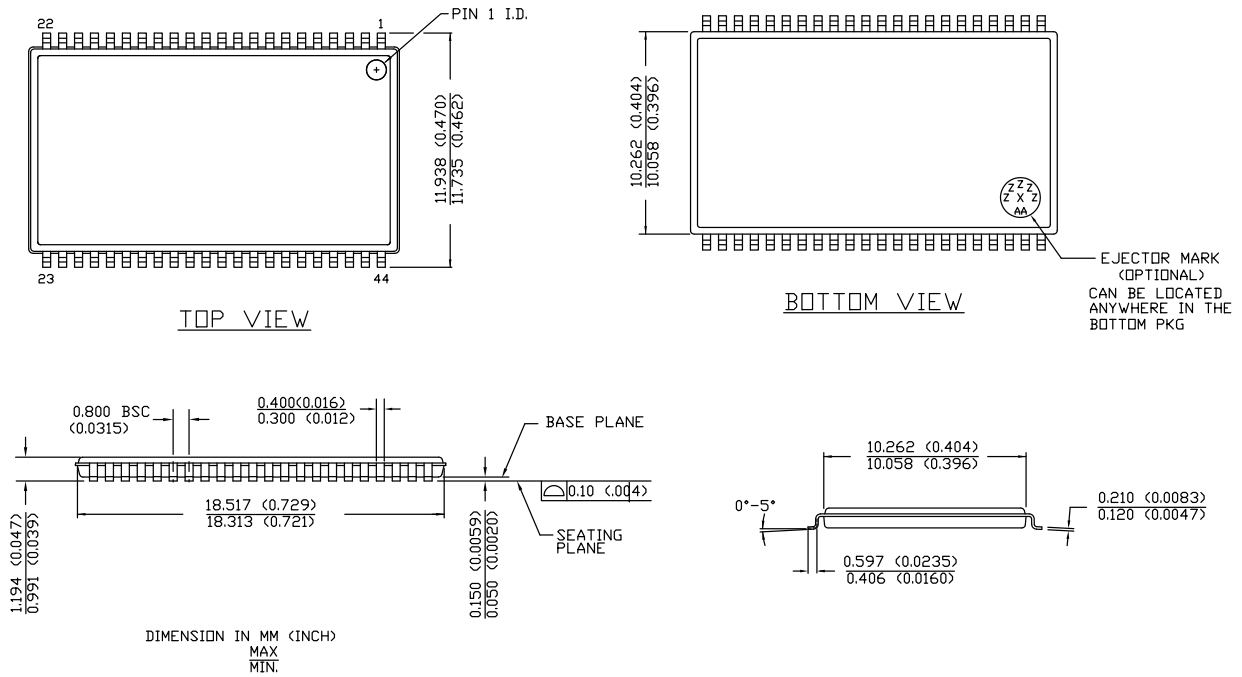
Figure 9. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082



51-85082 *D

Package Diagrams (continued)

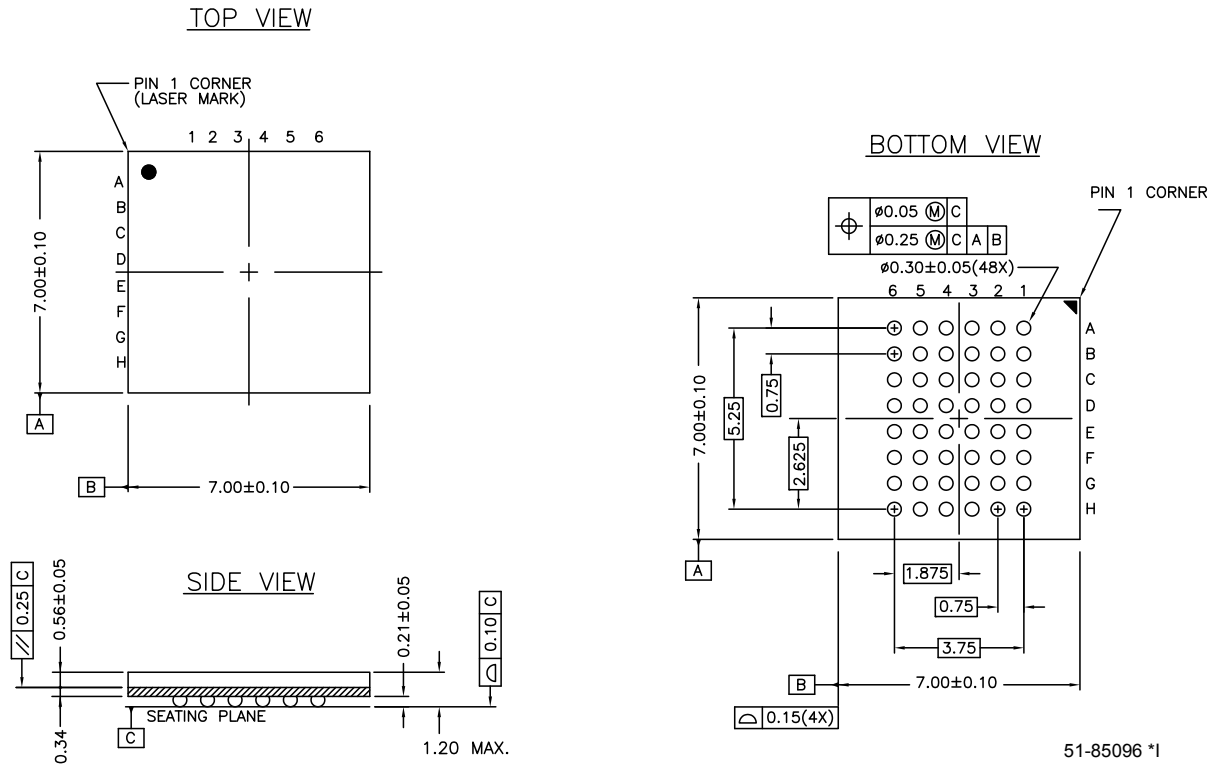
Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *D

Package Diagrams (continued)

Figure 11. 48-ball FBGA (7 × 7 × 1.2 mm) BA48 Package Outline, 51-85096



Acronyms

Acronym	Description
BGA	ball grid array
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
FBGA	fine-pitch ball grid array
I/O	input/output
$\overline{\text{OE}}$	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TQFP	thin quad flat pack
TSOP	thin small-outline package
TTL	transistor-transistor logic
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
mW	milliwatt
MHz	megahertz
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1021CV33, 1-Mbit (64 K × 16) Static RAM Document Number: 38-05132				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	109472	12/06/01	HGK	New data sheet
*A	115044	05/08/02	HGK	Ram7 version C4K x 16 Async Removed "Preliminary"
*B	115808	06/25/02	HGK	I _{SB1} and I _{CC} values changed
*C	120413	10/31/02	DFP	Updated BGA pin E4 to NC
*D	238454	See ECN	RKF	Added Automotive Specifications to datasheet Added Pb-free devices in the Ordering Information
*E	334398	See ECN	SYT	Added Pb-free on page 9 and 10
*F	493565	See ECN	NXR	Added Automotive-A operating range Corrected typo in the Pin Definition table Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I _{OS} parameter from DC Electrical Characteristics table Updated the ordering information table
*G	563963	See ECN	VKN	Added t _{POWER} specification in the AC Switching Characteristics table Added footnote 8
*H	1390863	See ECN	VKN / AESA	Corrected TSOP II package outline
*I	1891366	See ECN	VKN / AESA	Added -10ZSXA part in the Ordering Information table Updated Ordering Information Table
*J	2880096	02/17/2010	VKN / AESA	Added "CY7C1021CV33-10ZXI" part in the Ordering Information table Updated package diagrams.
*K	2897691	03/23/2010	RAME	Updated Ordering Information Updated Package Diagrams
*L	3089939	11/18/2010	PRAS	Removed inactive parts from Ordering Information.
*M	3127893	01/04/2011	HMLA	Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated in new template.
*N	3272897	06/07/2011	HMLA	Updated Features (Removed the information associated with speed bins -8 and also the information associated with Commercial and Industrial parts.) Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.".) Updated Selection Guide (Removed the information associated with Commercial and Industrial parts.) Updated Operating Range (Removed the information associated with Commercial and Industrial parts.) Updated Electrical Characteristics (Removed the information associated with Commercial and Industrial parts.) Updated Package Diagrams .
*O	3400821	10/10/2011	HMLA	Updated Operating Range (Straddled both rows under V _{CC} column so that the same condition is applicable for both Automotive-A and Automotive-E ranges). Updated Ordering Information (Removed the Note "The 44-pin TSOP II package containing the Automotive grade device is designated as "ZS", while the same package containing the Commercial/Industrial grade device is "Z"." below the Ordering Information table since Commercial/Industrial grade devices are not offered in this data sheet). Updated Package Diagrams .

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