

Features

- Temperature Ranges
 - Industrial: -40 °C to 85 °C
 - Automotive-A: -40 °C to 85 °C
- Pin and Function compatible with CY7C1019BV33
- High Speed
 - $t_{AA} = 10 \text{ ns}$
- CMOS for optimum Speed and Power
- Data Retention at 2.0 V
- Center Power/Ground Pinout
- Automatic Power Down when deselected
- Easy Memory Expansion with \overline{CE} and \overline{OE} Options
- Available in Pb-free 32-pin TSOP II package

Functional Description

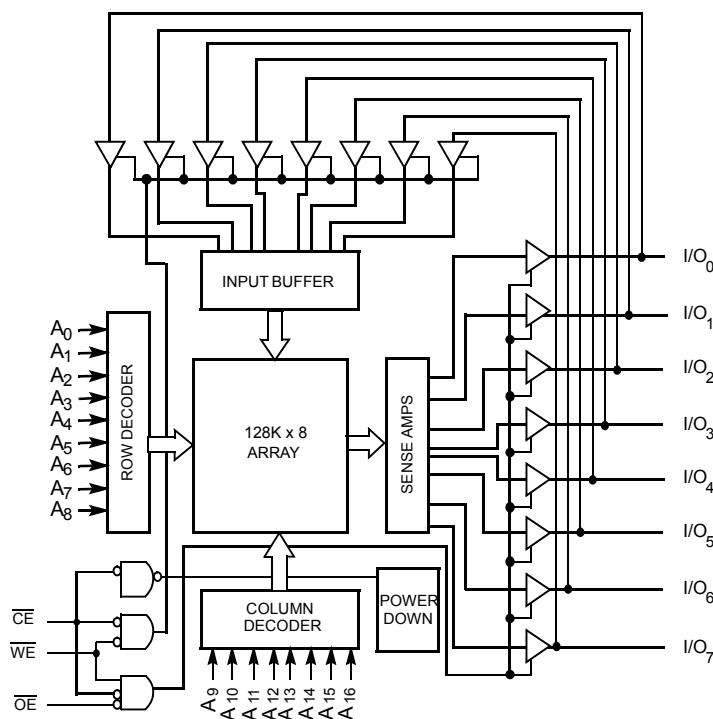
The CY7C1019CV33 is a high performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and tristate drivers. This device has an automatic power down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

Logic Block Diagram



Contents

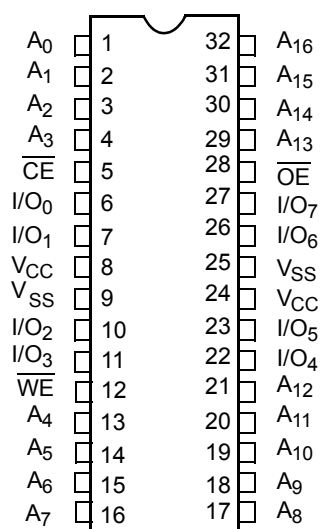
Selection Guide	3	Package Diagram	10
Pin Configuration	3	Acronyms	11
Maximum Ratings	4	Document Conventions	11
Operating Range	4	Units of Measure	11
Electrical Characteristics	4	Document History Page	12
Capacitance	4	Sales, Solutions, and Legal Information	13
AC Test Loads and Waveforms	5	Worldwide Sales and Design Support	13
Switching Characteristics	6	Products	13
Switching Waveforms	7	PSoC Solutions	13
Truth Table	9		
Ordering Information	9		
Ordering Code Definitions	9		

Selection Guide

Description	-10 (Industrial/ Auto-A)	Unit
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum Standby Current	5	mA

Pin Configuration

Figure 1. 32-pin TSOP II (Top View) ^[1]



Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Ambient Temperature with
Power Applied -55 °C to +125 °C

Supply Voltage on
 V_{CC} to Relative GND^[2] -0.5 V to +4.6 V

DC Voltage Applied to Outputs
in High Z State^[2] -0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage^[2] -0.5 V to $V_{CC} + 0.5$ V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 10%
Industrial	-40 °C to +85 °C	3.3 V ± 10%
Automotive-A	-40 °C to +85 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10 (Industrial/Auto-A)		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[2]		-0.3	0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	—	80	mA
I_{SB1}	Automatic CE Power down Current — TTL Inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	—	15	mA
I_{SB2}	Automatic CE Power down Current — CMOS Inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$, or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$	—	5	mA

Capacitance

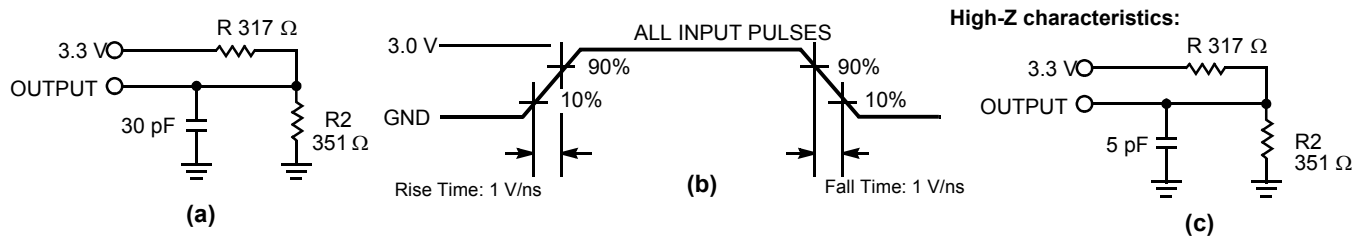
Parameter ^[3]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 5.0 \text{ V}$	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes

- $V_{IL} (\text{min.}) = -2.0 \text{ V}$ for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[4]



Note

4. AC characteristics (except High Z) for all speeds are tested using the Thevenin load shown in section (a) in Figure 2. High Z characteristics are tested for all speeds using the test load shown in section (c) in Figure 2.

Switching Characteristics

Over the Operating Range

Parameter ^[5]	Description	-10 (Industrial/ Auto-A)		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read Cycle Time	10	–	ns
t _{AA}	Address to Data Valid	–	10	ns
t _{OHA}	Data Hold from Address Change	3	–	ns
t _{ACE}	\overline{CE} LOW to Data Valid	–	10	ns
t _{DOE}	\overline{OE} LOW to Data Valid	–	5	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0	–	ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]	–	5	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	3	–	ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]	–	5	ns
t _{PU} ^[8]	\overline{CE} LOW to Power Up	0	–	ns
t _{PD} ^[8]	\overline{CE} HIGH to Power Down	–	10	ns
Write Cycle ^[9, 10]				
t _{WC}	Write Cycle Time	10	–	ns
t _{SCE}	\overline{CE} LOW to Write End	8	–	ns
t _{AW}	Address Setup to Write End	8	–	ns
t _{HA}	Address Hold from Write End	0	–	ns
t _{SA}	Address Setup to Write Start	0	–	ns
t _{PWE}	\overline{WE} Pulse Width	7	–	ns
t _{SD}	Data Setup to Write End	5	–	ns
t _{HD}	Data Hold from Write End	0	–	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3	–	ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6, 7]	–	5	ns

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of [Figure 2 on page 5](#). Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 3. Read Cycle No. 1 [11, 12]

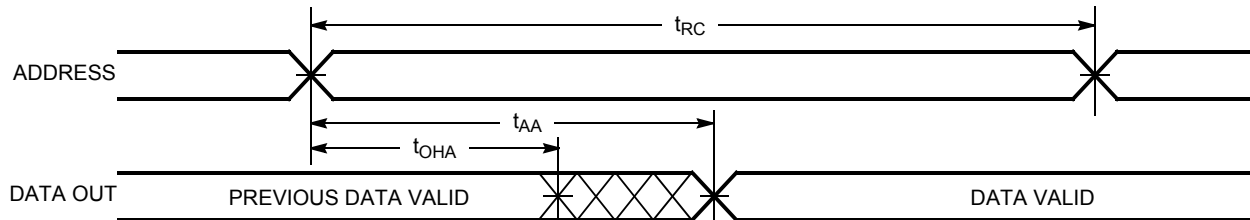


Figure 4. Read Cycle No. 2 (\overline{OE} Controlled) [12, 13]

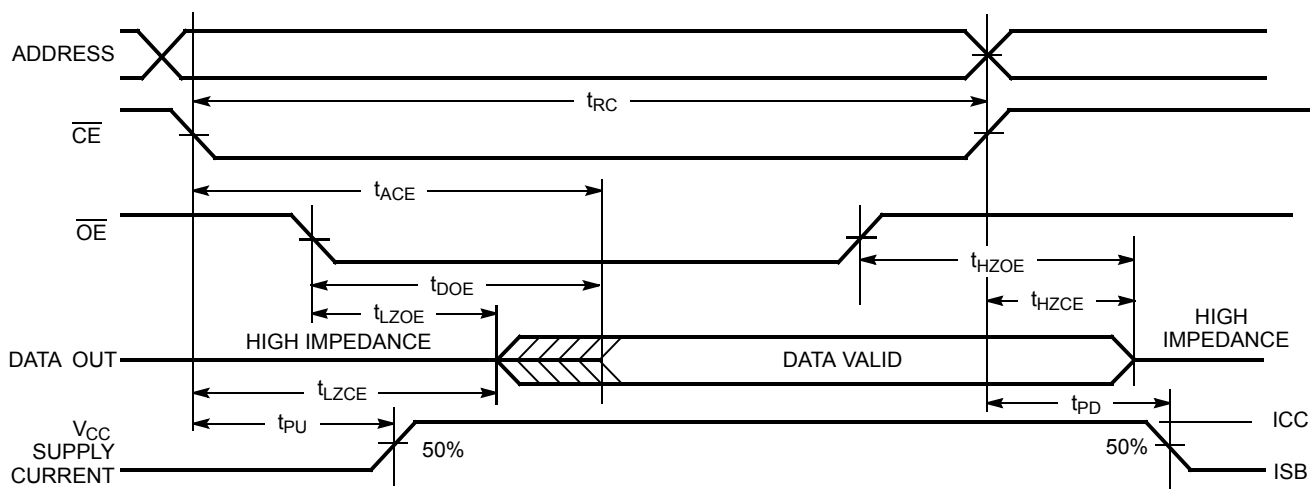
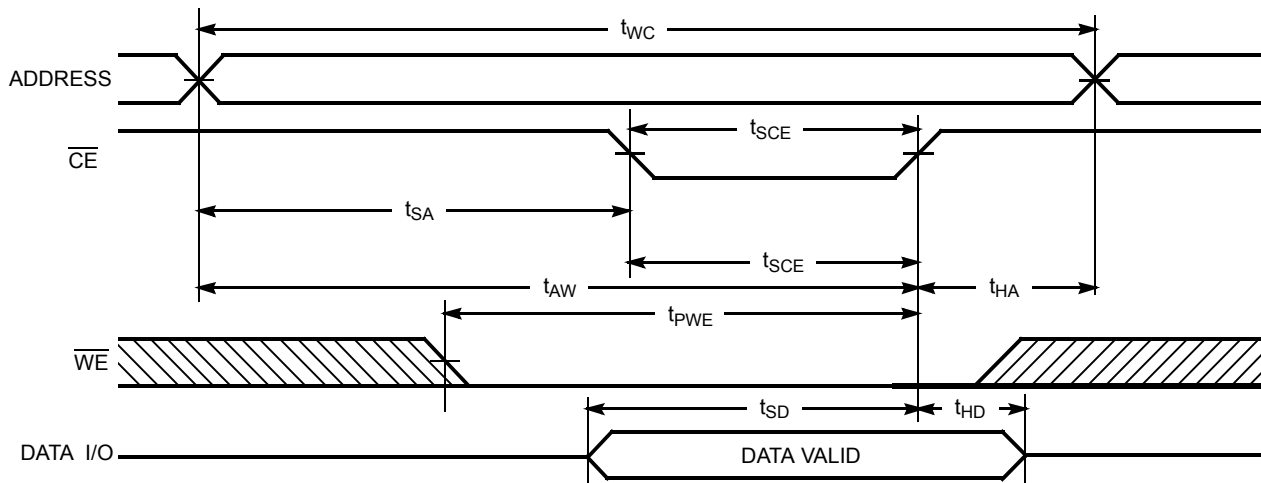


Figure 5. Write Cycle No. 1 (\overline{CE} Controlled) [14, 15]



Notes

11. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
12. \overline{WE} is HIGH for read cycle.
13. Address valid prior to or coincident with \overline{CE} transition LOW.
14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [16, 17]

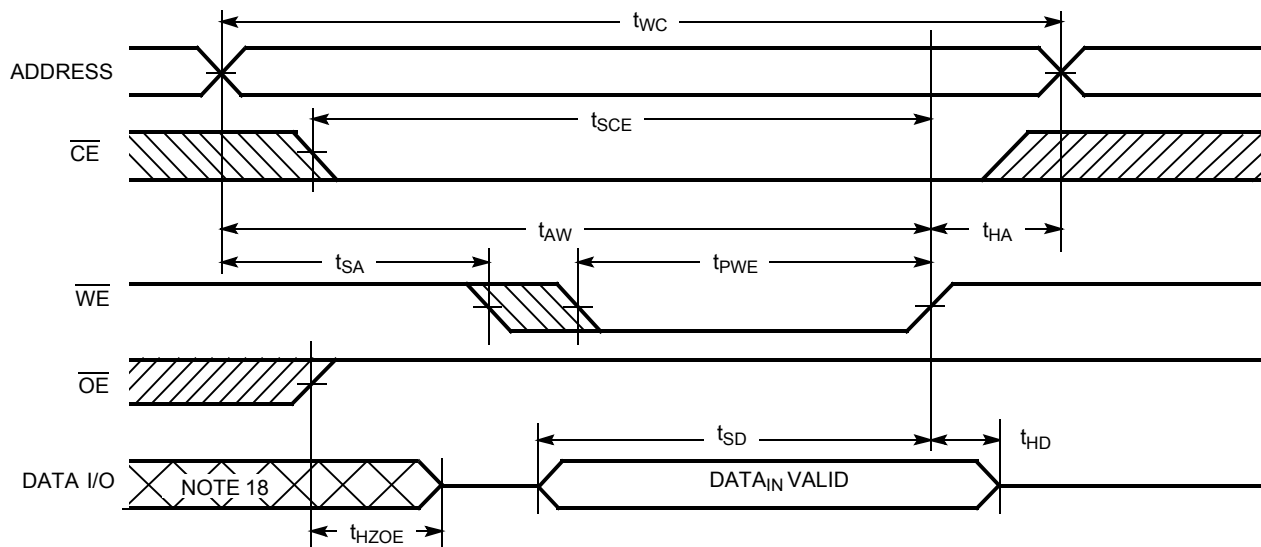
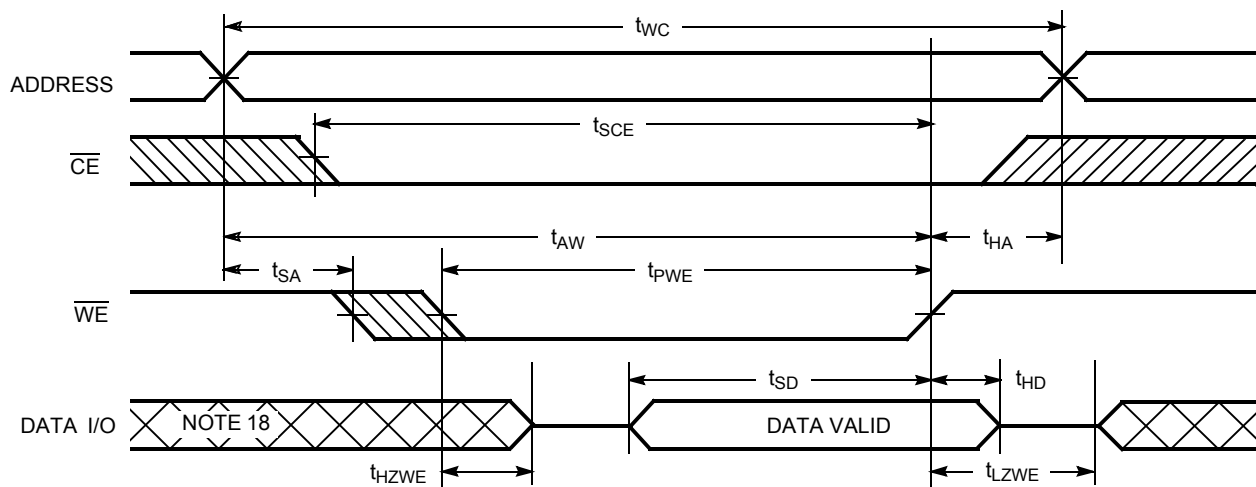


Figure 7. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [17]



Notes

16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
 17. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.
 18. During this period the I/Os are in the output state and input signals should not be applied.

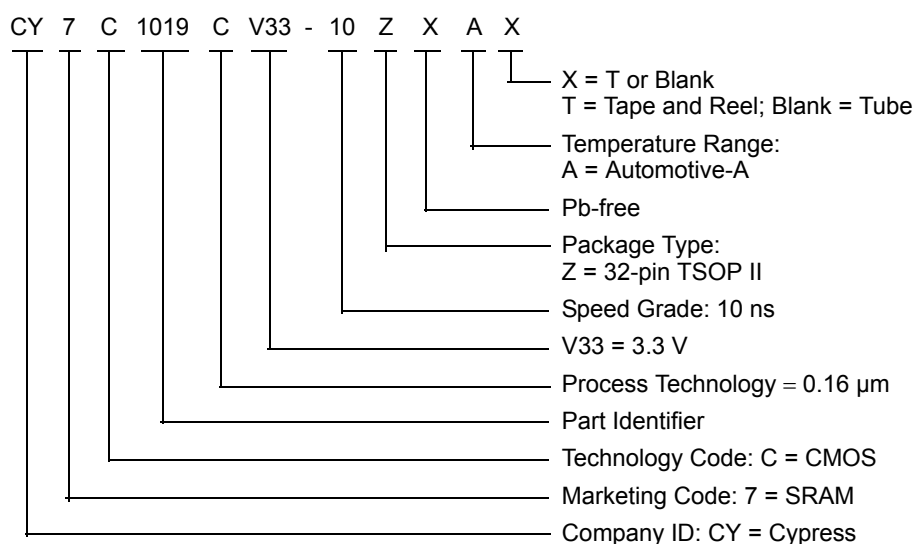
Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ –I/O ₇	Mode	Power
H	X	X	High Z	Power Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

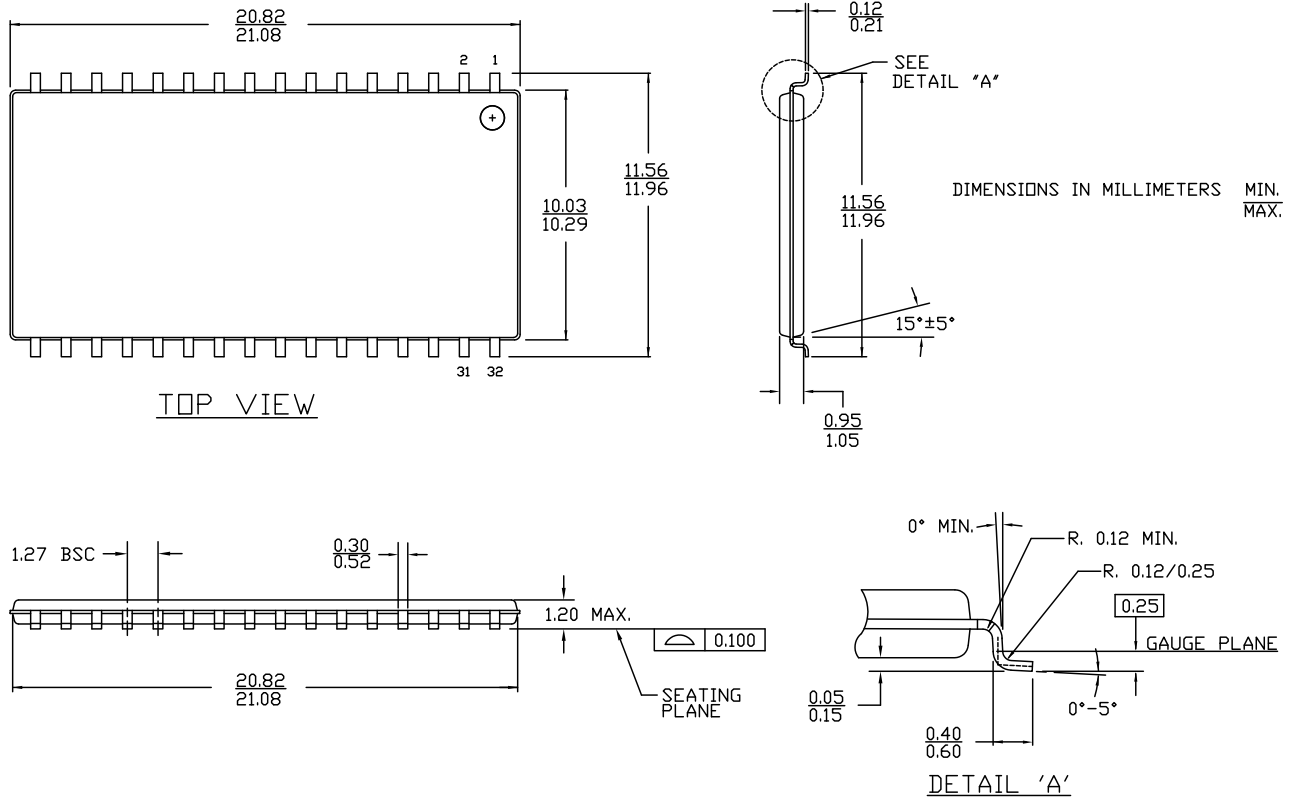
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1019CV33-10ZX A	51-85095	32-pin TSOP II (Pb-free)	Automotive-A
	CY7C1019CV33-10ZXAT	51-85095	32-pin TSOP II (Pb-free)	

Ordering Code Definitions



Package Diagram

Figure 8. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32



51-85095 *B

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
$\overline{\text{CE}}$	chip enable
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
mm	milli meter
ms	milli seconds
ns	nano seconds
%	percent
pF	pico Farad
V	Volts
W	Watts

Document History Page

Document Title: CY7C1019CV33, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05130				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	109245	12/16/01	HGK	New Data Sheet
*A	113431	04/10/02	NSL	AC Test Loads split based on speed
*B	115047	08/01/02	HGK	Added TSOP II Package and I Temp. Improved I _{CC} limits
*C	119796	10/11/02	DFP	Updated standby current from 5 nA to 5 mA
*D	123030	12/17/02	DFP	Updated Truth Table to reflect single Chip Enable option
*E	419983	See ECN	NXR	Added 48-ball VFBGA Package Added lead-free parts in Ordering Information Table Replaced Package Name column with Package Diagram in the Ordering Information Table
*F	493543	See ECN	NXR	Removed 8 ns speed bin from Product offering Added note #1 on page #2 Changed the description of I _{LX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I _{OS} parameter from DC Electrical Characteristics table Updated Ordering Information
*G	2761448	09/09/2009	VKN	Included Automotive-A information
*H	2897691	03/23/2010	RAME	Updated Ordering Information Updated Package Diagrams
*I	3057593	10/13/2010	PRAS	Updated Ordering Information and added Ordering Code Definitions . Updated Package Diagram .
*J	3072834	11/11/2010	PRAS	Removed obsolete parts and package diagrams.
*K	3277371	06/08/2011	AJU	Updated Features . Updated Selection Guide (Removed -12 (Industrial) and -15 (Industrial) columns). Updated Electrical Characteristics (Removed -12 (Industrial) and -15 (Industrial) columns). Updated Switching Characteristics (Removed -12 (Industrial) and -15 (Industrial) columns). Updated Package Diagram . Updated in new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2001-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.