

## Features

- Pin- and function-compatible with CY7C1020CV33
- Temperature Ranges
  - Commercial: 0 °C to 70 °C
  - Industrial: -40 °C to 85 °C
  - Automotive: -40 °C to 125 °C
- High speed
  - $t_{AA} = 10$  ns
- CMOS for optimum speed/power
- Low active power
  - 325 mW (max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin TSOP II package

## Functional Description

The CY7C1020CV33 is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

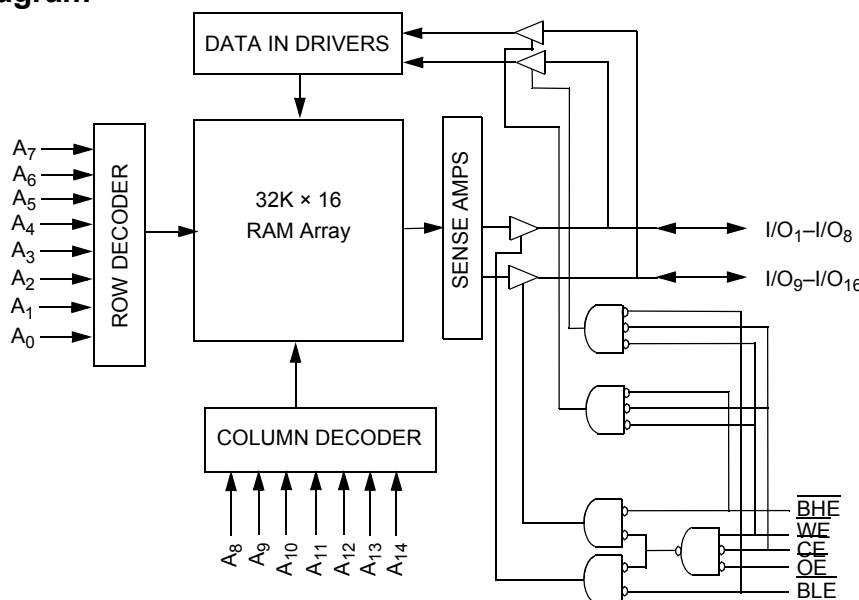
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>1</sub> through I/O<sub>8</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>14</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>9</sub> through I/O<sub>16</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>14</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>1</sub> to I/O<sub>8</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>9</sub> to I/O<sub>16</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O<sub>1</sub> through I/O<sub>16</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}$  LOW, and WE LOW).

The CY7C1020CV33 is available in standard 44-pin TSOP Type II package.

## Logic Block Diagram



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## Selection Guide

		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial/Industrial	90	85	80	mA
	Automotive	—	—	85	mA
Maximum CMOS Standby Current	Commercial/Industrial	5	5	5	mA
	Automotive	—	—	10	mA

## Pin Configuration <sup>[1]</sup>

**TSOP II**  
**Top View**

NC	1	44	A <sub>5</sub>
A <sub>3</sub>	2	43	A <sub>6</sub>
A <sub>2</sub>	3	42	A <sub>7</sub>
A <sub>1</sub>	4	41	OE
A <sub>0</sub>	5	40	BHE
CE	6	39	BLE
I/O <sub>1</sub>	7	38	I/O <sub>16</sub>
I/O <sub>2</sub>	8	37	I/O <sub>15</sub>
I/O <sub>3</sub>	9	36	I/O <sub>14</sub>
I/O <sub>4</sub>	10	35	I/O <sub>13</sub>
V <sub>CC</sub>	11	34	V <sub>SS</sub>
V <sub>SS</sub>	12	33	V <sub>CC</sub>
I/O <sub>5</sub>	13	32	I/O <sub>12</sub>
I/O <sub>6</sub>	14	31	I/O <sub>11</sub>
I/O <sub>7</sub>	15	30	I/O <sub>10</sub>
I/O <sub>8</sub>	16	29	I/O <sub>9</sub>
WE	17	28	NC
A <sub>4</sub>	18	27	A <sub>8</sub>
A <sub>14</sub>	19	26	A <sub>9</sub>
A <sub>13</sub>	20	25	A <sub>10</sub>
A <sub>12</sub>	21	24	A <sub>11</sub>
NC	22	23	NC

### Note

1. NC pins are not connected on the die.

## Pin Definitions

Pin Name	TSOP - Pin Number	I/O Type	Description
A <sub>0</sub> –A <sub>14</sub>	5, 4, 3, 2, 18, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19	Input	<b>Address Inputs used to select one of the address locations.</b>
I/O <sub>1</sub> –I/O <sub>16</sub>	7-10, 13-16, 29-32, 35-38	Input/Output	<b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.
NC	1, 22, 23, 28	No Connect	<b>No Connects.</b> Not connected to the die.
$\overline{\text{WE}}$	17	Input/Control	<b>Write Enable Input, active LOW.</b> When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{\text{CE}}$	6	Input/Control	<b>Chip Enable Input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}$ , $\overline{\text{BLE}}$	40, 39	Input/Control	<b>Byte Write Select Inputs, active LOW.</b> $\overline{\text{BHE}}$ controls I/O <sub>16</sub> –I/O <sub>9</sub> , $\overline{\text{BLE}}$ controls I/O <sub>8</sub> –I/O <sub>1</sub> .
$\overline{\text{OE}}$	41	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V <sub>SS</sub>	12, 34	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	11, 33	Power Supply	<b>Power Supply inputs to the device.</b>

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  to relative GND<sup>[2]</sup> ..... -0.5 V to +4.6 V

DC voltage applied to outputs in high Z State<sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage<sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2001 V (per MIL-STD-883, method 3015)

Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Commercial	0 °C to +70 °C	3.3 V ± 10%
Industrial	-40 °C to +85 °C	3.3 V ± 10%
Automotive	-40 °C to +125 °C	3.3 V ± 10%

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		-15		Unit
				Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = −4.0 mA		2.4	—	2.4	—	2.4	—	V
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA		—	0.4	—	0.4	—	0.4	V
V <sub>IH</sub>	Input HIGH voltage			2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage <sup>[2]</sup>			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Commercial/ Industrial	−1	+1	−1	+1	−1	+1	μA
			Automotive	—	—	—	—	−20	+20	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	Commercial/ Industrial	−1	+1	−1	+1	−1	+1	μA
			Automotive	—	—	—	—	−20	+20	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Commercial/ Industrial	—	90	—	85	—	80	mA
			Automotive	—	—	—	—	—	85	mA
I <sub>SB1</sub>	Automatic CE power-down current —TTL Inputs	Max V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Commercial/ Industrial	—	15	—	15	—	15	mA
			Automotive	—	—	—	—	—	20	mA
I <sub>SB2</sub>	Automatic CE power-down current —CMOS inputs	Max V <sub>CC</sub> , CE ≥ V <sub>CC</sub> − 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0	Commercial/ Industrial	—	5	—	5	—	5	mA
			Automotive	—	—	—	—	—	10	mA

## Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 3.3 \text{ V}$	8	pF
$C_{OUT}$	Output capacitance		8	pF

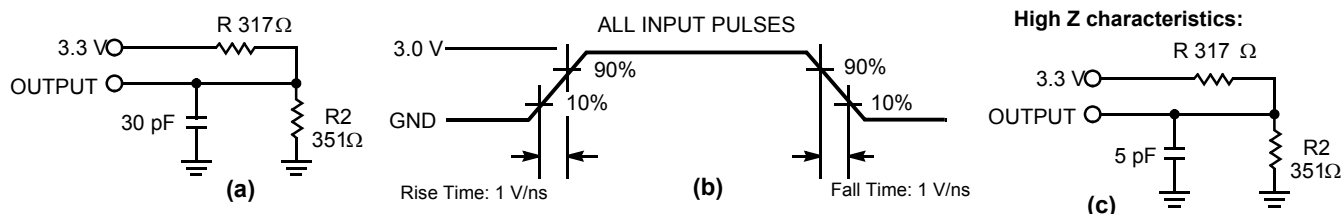
## Thermal Resistance<sup>[3]</sup>

Parameter	Description	Test Conditions	44-pin TSOP-II	Unit
$\Theta_{JA}$	Thermal resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	76.92	°C/W
$\Theta_{JC}$	Thermal resistance (Junction to Case)		15.86	°C/W

### Notes

- $V_{IL}(\text{min}) = -2.0 \text{ V}$  and  $V_{IH}(\text{max}) = V_{CC} + 0.5 \text{ V}$  for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms<sup>[4]</sup>



## Switching Characteristics

Over the Operating Range<sup>[4]</sup>

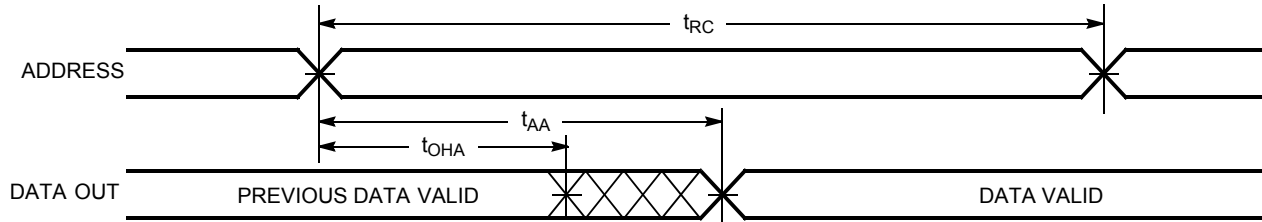
Parameter	Description	−10		−12		−15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t <sub>RC</sub>	Read cycle time	10	–	12	–	15	–	ns
t <sub>AA</sub>	Address to data valid	–	10	–	12	–	15	ns
t <sub>OHA</sub>	Data hold from address change	3	–	3	–	3	–	ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to data valid	–	10	–	12	–	15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	5	–	6	–	7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to low Z <sup>[5]</sup>	0	–	0	–	0	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to high Z <sup>[5, 6]</sup>	–	5	–	6	–	7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to low Z <sup>[5]</sup>	3	–	3	–	3	–	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to high Z <sup>[5, 6]</sup>	–	5	–	6	–	7	ns
t <sub>PU</sub> <sup>[7]</sup>	$\overline{CE}$ LOW to power-up	0	–	0	–	0	–	ns
t <sub>PD</sub> <sup>[7]</sup>	$\overline{CE}$ HIGH to power-down	–	10	–	12	–	15	ns
t <sub>DBE</sub>	Byte enable to data valid	–	5	–	6	–	7	ns
t <sub>LZBE</sub>	Byte enable to low Z	0	–	0	–	0	–	ns
t <sub>HZBE</sub>	Byte disable to high Z	–	5	–	6	–	7	ns
Write Cycle <sup>[8]</sup>								
t <sub>WC</sub>	Write cycle time	10	–	12	–	15	–	ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to write end	8	–	9	–	10	–	ns
t <sub>AW</sub>	Address set-up to write end	7	–	8	–	10	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	0	–	0	–	ns
t <sub>SA</sub>	Address set-up to write start	0	–	0	–	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	7	–	8	–	10	–	ns
t <sub>SD</sub>	Data set-up to write end	5	–	6	–	8	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	0	–	0	–	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to low Z <sup>[5]</sup>	3	–	3	–	3	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to high Z <sup>[5, 6]</sup>	–	5	–	6	–	7	ns
t <sub>BW</sub>	Byte enable to end of write	7	–	8	–	9	–	ns

### Notes

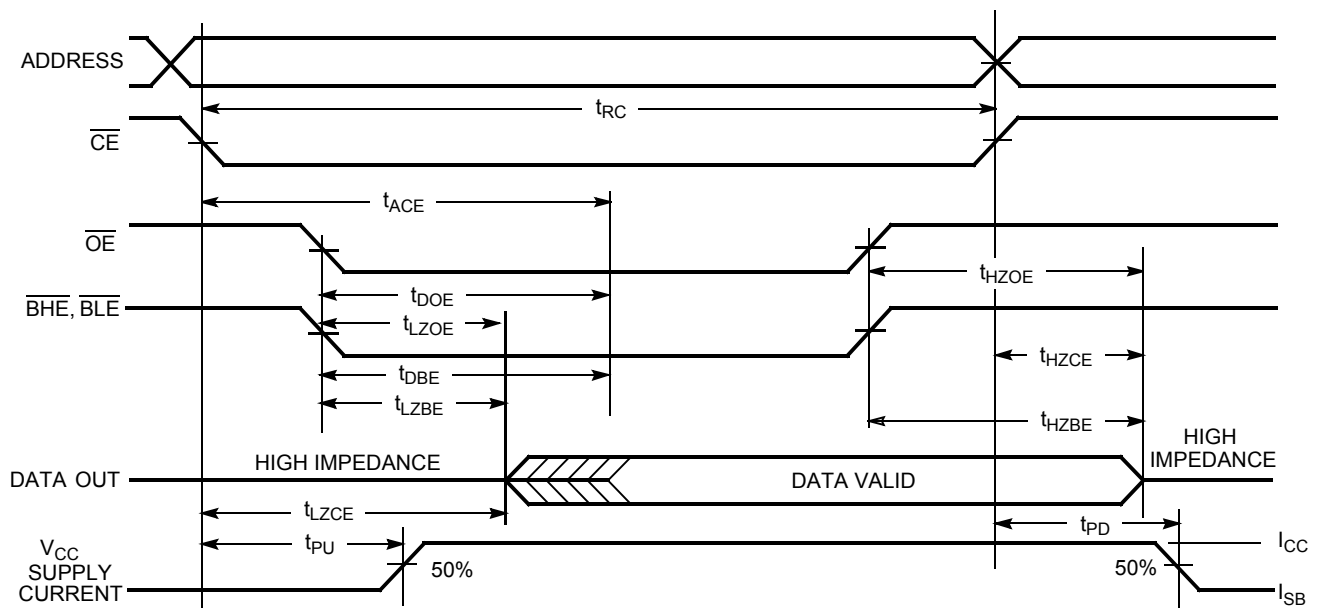
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

## Switching Waveforms

### Read Cycle No. 1<sup>[9, 10]</sup>



### Read Cycle No. 2 ( $\overline{OE}$ Controlled)<sup>[10, 11]</sup>

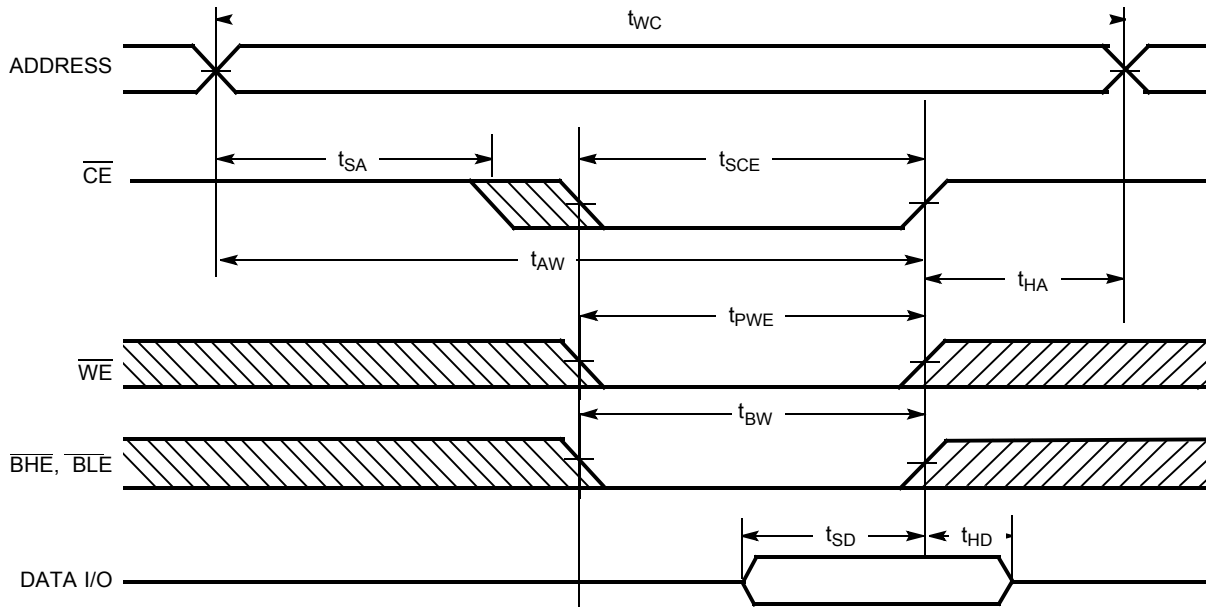


#### Notes

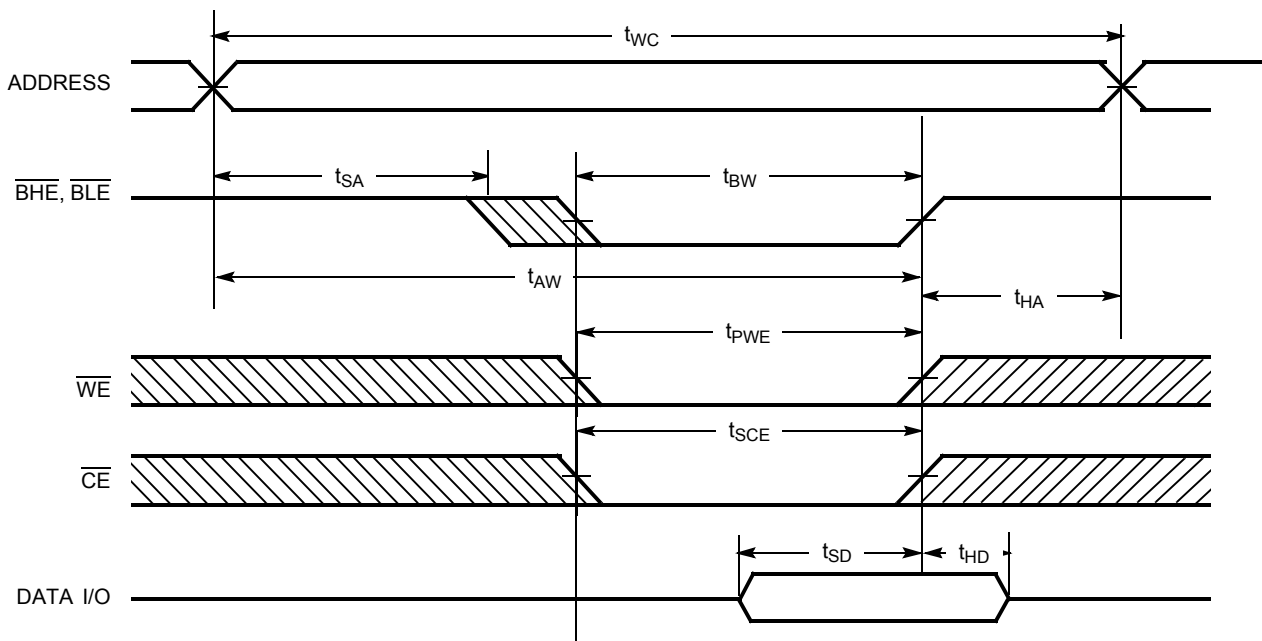
9. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
10.  $\overline{WE}$  is HIGH for Read cycle.
11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms *(continued)*

### Write Cycle No. 1 ( $\overline{\text{CE}}$ Controlled)<sup>[12, 13]</sup>



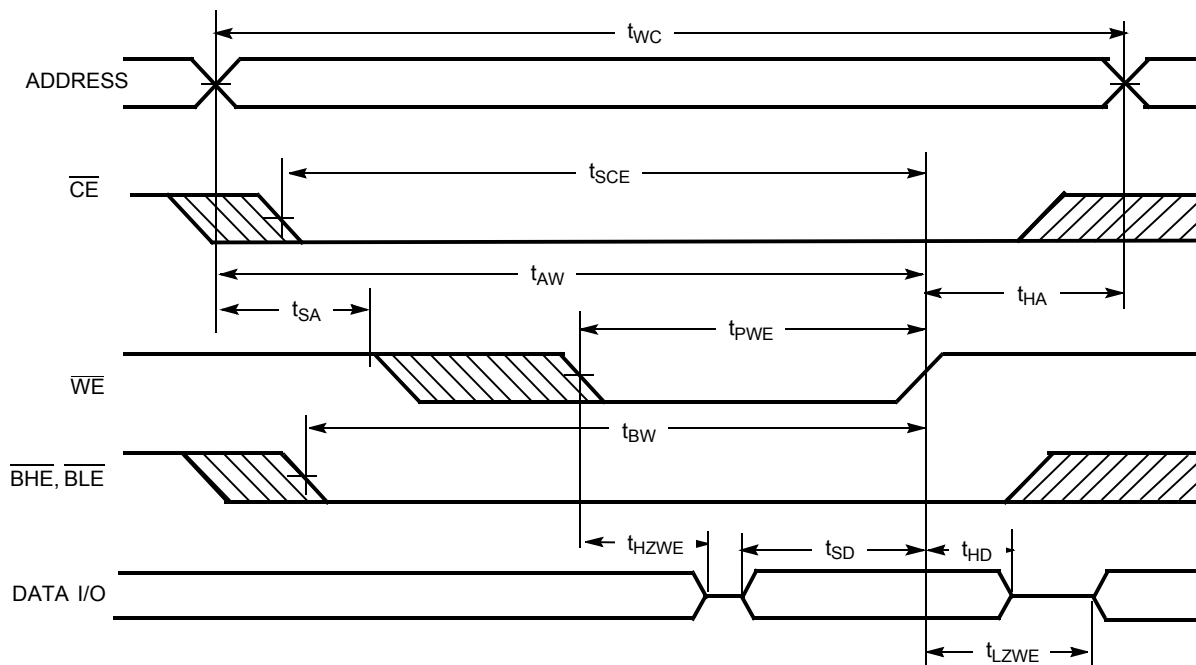
### Write Cycle No. 2 ( $\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



#### Notes

12. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
13. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.



**Switching Waveforms** *(continued)*
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)**

**Truth Table**

CE	OE	WE	BLE	BHE	I/O <sub>1</sub> –I/O <sub>8</sub>	I/O <sub>9</sub> –I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby ( $I_{\text{SB}}$ )
L	L	H	L	L	Data out	Data out	Read—All bits	Active ( $I_{\text{CC}}$ )
			L	H	Data out	High Z	Read—Lower bits only	Active ( $I_{\text{CC}}$ )
			H	L	High Z	Data out	Read—Upper bits only	Active ( $I_{\text{CC}}$ )
L	X	L	L	L	Data in	Data in	Write—All bits	Active ( $I_{\text{CC}}$ )
			L	H	Data in	High Z	Write—Lower bits only	Active ( $I_{\text{CC}}$ )
			H	L	High Z	Data in	Write—Upper bits only	Active ( $I_{\text{CC}}$ )
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active ( $I_{\text{CC}}$ )
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active ( $I_{\text{CC}}$ )

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1020CV33-15ZSX E	51-85087	44-pin TSOP Type II (Pb-free)	Automotive
	CY7C1020CV33-15ZSXET	51-85087	44-pin TSOP Type II (Pb-free)	Automotive

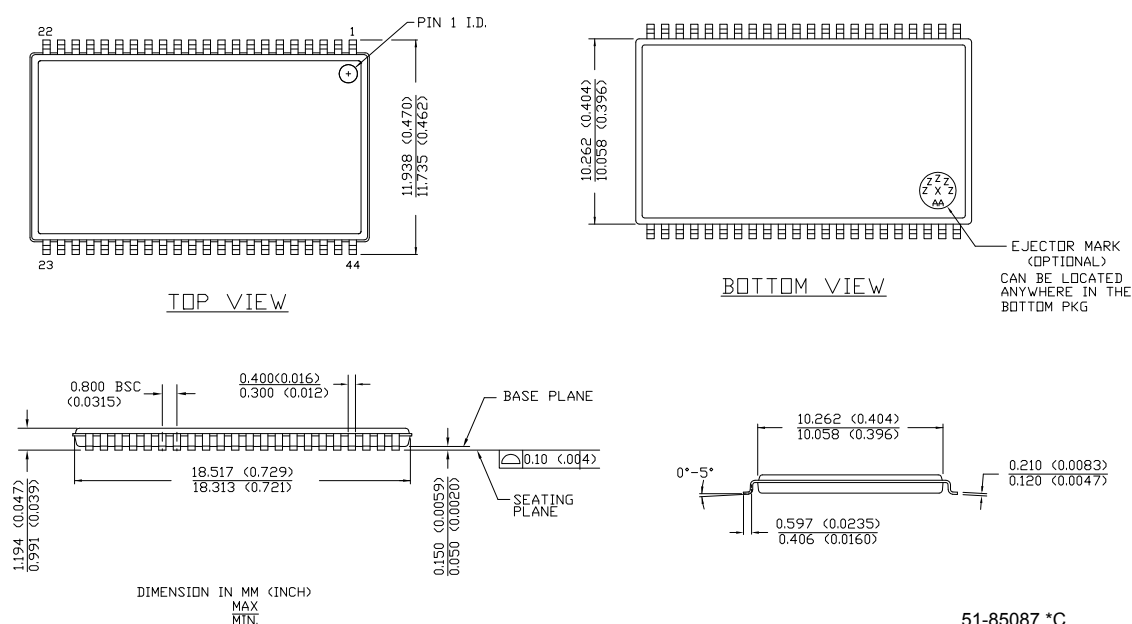
## Ordering Code Definitions

CY7C 1020 C V33 - 15 ZSX E X

X = T or Blank  
T = Tape and Reel; Blank = Tube  
Temperature Range:  
E = Automotive  
Package Type:  
ZSX = 44-pin TSOP Type II (Pb-free)  
Speed Grade = 15 ns  
V33 = 3.3 V  
Process Technology = 0.16  $\mu$ m  
1020 = Part Identifier  
CY7C = Cypress SRAMs

## Package Diagrams

**Figure 1. 44-pin TSOP II, 51-85087**



## Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small-outline package
TTL	transistor-transistor logic
WE	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts
%	percent

## Document History Page

Document Title: CY7C1020CV33 512 K (32 K × 16) Static RAM Document Number: 38-05133				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109428	12/16/01	HGK	New Data Sheet
*A	115045	05/30/02	HGK	I <sub>CC</sub> and I <sub>SB1</sub> data modified
*B	117615	08/14/02	DFP	Pin 1= NC Pin 18 = A4; remove SOJ package option; remove 8ns option.
*C	262949	See ECN	RKF	Added Automotive Specs to Data sheet
*D	334398	See ECN	SYT	Added Lead-Free Product Information
*E	493543	See ECN	NXR	Added note #1 on page #1 Changed the description of I <sub>IX</sub> from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I <sub>OS</sub> parameter from DC Electrical Characteristics table Updated Ordering Information Table
*F	2897691	03/23/2010	RAME	Updated Ordering Information Updated Package Diagram
*G	3057593	10/13/2010	PRAS	Updated <a href="#">Ordering Information</a> and added <a href="#">Ordering Code Definitions</a> .
*H	3100106	12/02/2010	PRAS	Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Minor edits and updated in new template.

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PSoC 1 | PSoC 3 | PSoC 5

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